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18066

Distr.
LIMITED

IPCT.108
9 February 1990

UNITED NATIONS
INDUSTRIAL DEVELOPMENT ORGANIZATION

ORIGINAL: ENGLISH

MICROELECTRONICS - WORLD SCENARIO AND THE INDIAN EXPERIENCE*

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* This study was prepared under the project DP/RLA/86/003 - Regional Project for Strengthening Microelectronics Infrastructure and Capabilities in REMLAC Member Countries - and was presented at the Meeting of the Consultative Group on Informatics Technology for Development, Buenos Aires, Argentina, 11-13 December 1989. The views expressed in this document are those of the author and do not necessarily reflect the views of the Secretariat of UNIDO. This document has not been edited.

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I. BACKGROUND

1. Forty one years ago, Shockley, Bardeen and Brattain at Bell Laboratories, USA invented the point contact transistor leading to the birth of semiconductor industry. In 1955, Texas Instruments, USA began manufacture of silicon transistors on a commercial basis initiating a new era in electronics. In 1958, Jack Kilby of Texas Instruments and Bob Noyce of Fairchild independently invented the Integrated Circuit (IC). The growth of the IC industry, thereafter, has been phenomenal. This period has witnessed the doubling of the integration level every sixteen months while the expenditure for the chip lay-out and chip design has doubled only every thirty two months.

2. Microelectronics - which primarily refers to Integrated Circuits (ICs) ranging from the Small Scale Integration (SSI) to Very Large Scale Integration (VLSI) - is recognised as a vital ingredient of electronics equipment and systems. In fact, the relentless increase in the level of integration is leading to entire sub-systems and even systems being fabricated on chips of few mm square size. Microelectronics is thus making possible the revolution in the management and movement of information. Information and knowledge based

technologies are expected to be the driving engines of national economies in future.

II. WORLD SCENARIO

3. Semiconductors have been called the "crude oil" of the 21st century. In the years to come, the positions of countries would depend strongly on their strengths in electronics and in particular in microelectronics. The thrust in LSI/VLSI has been the corner stone of Japan's strategy and the major factor in its strength in the Organisation for Economic Cooperation and Development (OECD). The importance of this industry has also been recognised by the Newly Industrialised Countries (NICs) such as Korea, Taiwan, Hong Kong, Singapore, India and Thailand. The USA was a major exporter of electronic goods to the rest of the world before 1975. Japan and the NICs have, however, taken away the lead from the USA in some sectors of microelectronics and have become dominant in others. In fact, the scenario in microelectronics became truly international in 1986 when Japan became the largest consumer and producer of microelectronics in the world. The "chip war" between USA and Japan, the creation of SEMATECH in USA to counter the Japanese challenge, the MEGA project between Siemens & Philips, the Alvey programme in UK, the initiatives launched by Europe - the European Strategic Programme for Research and Development in Information Technology (ESPRIT), the Joint European Sub-micron Silicon Initiative (JESSI) - a sequel to the MEGA project - are some recent international

developments which bring out the criticality and imperatives of this industry.

4. World production of semiconductors in 1988 was estimated at US $ 54.72 billion comprising US $ 46.48 billion of ICs and US $ 8.24 billion in discrete semiconductor devices. It is believed that world semiconductor production will continue to grow at a Compound Annual Growth Rate (CAGR) of between 14% to 16% into the 1990s. During the last decade, semiconductor manufacturers have invested heavily in capital equipment to shrink the line geometries and increase capacities with the result that the price per function is semiconductor products has been decreasing at a rate unparalleled in any other industry. Thus, the recent slump in the electronics industry has been felt even more acutely by the semiconductor manufacturers due to the creation of excess capacities.

5. While building a fab in 1980 required a potential market of US $ 35 million, this number is expected to rise to approximately US $ 500 million by 2000. It is expected that the industry would be using 10" wafers by 1995 and 12" wafers by the year 2000. An optimum fab would have an operating level of 14000 wafer starts per month. If a more aggressive operating level of 20000, 12" wafers per month is assumed. the revenue potential of a single fab rises to more than 670 million dollars which is higher than the total semiconductor sales of American Micro Devices in 1985. These fabs will be forced to look not only for clients to buy their standard

products but will have to undertake foundry work as well. A trend could also emerge for colocating a "fab-in-a-box" with the design houses for faster turn around times. LASARRAY, Switzerland and QUDOS, UK are examples of this approach.

III. MODELS FOR GROWTH

6. The semiconductor industry developed in the beginning in the USA followed by Europe. Japan entered in the race much later and recently South Korea, Taiwan, Hong Kong and Singapore have also launched major activities in microelectronics. The development of microelectronics in these countries can provide useful models for planning the growth of microelectronics. The Japanese model is characterised by a strong Government-controlled (Ministry of International Trade and Industry (MITI)), cooperative growth. The success of this model is proven by the fact that 6 Japanese companies figured in the top 10 companies in the world in chip production in 1988 with the first three positions being held by NEC, Toshiba, and Hitachi. The South Korean model is characterised by the emergence of the 4 main chaebols (conglomerates), viz., Samsung, Lucky-Goldstar, Hyundai, Daewoo, which together sold chips worth US $ 1.2 billion in 1988. The South Korean firms cater to the low end of the market vacated by USA and Japan. For example, they are filling the gap for 256 K DRAMs as the Japanese shift to manufacture 1 Mb DRAMs. Taiwan, Hong Kong and Singapore are

relatively new entrants into this arena but are fast making a mark through a mix of liberal policies and incentives.

IV. TECHNOLOGY TRENDS

7. In the area of technology development, DRAMs and SRAMs continue to be the key technology drivers. 1 Mbit DRAMs are now commercially available. 4 Mbit DRAMs and 1 Mbit SRAMs - which employ the same fine line processing technologies as the 4 Mbit DRAMs - are being shipped in prototype quantities. At the 1988 International Solid State Circuits Conference, major semiconductor manufacturers including Toshiba, Hitachi and Matsushita unveiled prototype 16 Mbit DRAMs. Although both making and using mega-bit level memories are still rare skills, a few IC memory suppliers are reported to be readying 16 Mbit DRAMs for sampling before the end of 1989. This trend may also necessitate a change from the conventional 5 volt battery supply to 3.3 volts. The minimum feature size has been shrinking steadily. The cutting edge production technologies of today are around 0.5 micron; 16 Mbit DRAM of Matsushita was manufactured with 0.5 micron design rules. The geometries are expected to shrink to quarter of a micron by the turn of the century. Another development which is close to commercialisation is Gallium Arsenide (GaAs) - on - silicon which unites the high speed and opto-electronic capability of GaAs with the low material cost and superior mechanical and thermal properties of a silicon substrate. The CRAY-3 super-computer is said to use almost all GaAs circuits. Fujitsu is committed to using high electron

mobility transistors in a mostly GaAs computer. In the area of packaging, Tape Automated Bonding (TAB) is fast gaining ground. TAB takes up an area from a third to tenth of the size of most surface mounts while providing lead protection, burn-in and testability.

8. Smart power ICs - analog chips with digital control circuitry - are finding applications ranging from power supplies to automobiles. BiCMOS is emerging as the key to VLSI in the 1990s while the speed improvement in BiCMOS makes it attractive for SRAMs and gate arrays, its usefulness in microprocessors is yet to be established. In the area of Application Specific Integrated Circuits (ASICs), sea-of-gates approach is gaining popularity with the structured array as the logical next step. As the gate count gets pushed to 50,000 - 100,000 level, design systems would need to achieve a thousand fold productivity improvement in the next decade. Object-oriented design systems - which allow concurrent design synthesis to take downstream design constraints into account early in the design cycle - are expected to meet this demand.

9. As the cost of scaling VLSI circuits increases, more attention is being focused on packaging. Multichip modules based on ceramic or silicon motherboards are already common. Mounting silicon chips on silicon motherboards creates a hybrid version of wafer scale integration but lacks the classical test and yield problems of that technology. It

significantly increases wiring density and enhances thermal matching, and also distributes the technology requirements between the VLSI chip and the motherboard. Typical applications of the silicon motherboard increase density seven to ten times, triple performance, and cut power consumption by 30-40 percent. In a different direction, research continues on molecular electronics with efforts to realise the bio-chip. An analogous effort is to use VLSI to generate a neural computer.

V. THE INDIAN EXPERIENCE

10. Production of electronics industry in India 1988-89 was Rupees (Rs) 70,300 million (1 US $ = 16.9 Rs). Anticipated production in 1989-90 is Rs.92,100 million. Sector-wise break-up of the anticipated production in 1989-90 and 1994-95 is given below:

	1989-90	1994-95
	Rs.Million	
Systems	72,500	2,00,000
Components	16,000	65,000
Export-oriented Production	3,600	35,000
	92,100	3,00,000

V.1 IC Manufacturing

11. India has the capability to design, develop and manufacture ICs ranging from SSI to VLSI in both bipolar and MOS technologies. The annual IC production in 1988 was around 11 million numbers valued at Rs.120 million. It is estimated that import of ICs into India in 1988 in various forms viz., chips, chips-on-board and chips as part of sub-systems was around Rs.1,000 million. While the total percentage of semiconductors in the Indian electronic equipment is around 5% as compared to the International average of around 12%, it is to be noted that Indian electronics production constitutes less than 1% of the world electronics production.

12. Manufacture of MOS ICs, till recently, was primarily carried out at the Semiconductor Complex Ltd. (SCL), SAS Nagar - a Public Sector Unit (PSU) under the Department of Electronics (DOE), Government of India - before the device manufacturing and process R&D facilities were destroyed in a fire in February, 1989. Bharat Electronics Ltd. (BEL), Bangalore - another PSU - manufactures bipolar ICs. In the private sector, ICs of the SSI/MSI complexity are manufactured by Hindustan Conductors Ltd. and Greaves Semiconductors. SPIC Electronics Ltd. (SPEL), Madras is essentially an assembly operation based on diffused wafers procured from abroad. SCL was set up with the objective to design, develop and manufacture LSI/VLSI MOS circuits, modules and sub-systems for telecommunication, data

processing, consumer electronics and other applications. SCL obtained process and design knowhow from M/s American Microsystems Inc. (AMI), USA for the manufacture of CMOS and NMOS circuits and started commerical production in 1984. SCL developed the 3 micron CMOS process with in-house R&D ard was in the process of establishing a 2 micron CMOS process in production when fire destroyed their facilities in February, 1989. SCL's corporate turnover in 1987-88 was Rs.115.70 million consisting of 6 million chips valued at Rs.38.70 million and modules, sub-systems and services worth Rs.77 million. The product range included clock chip, pulse dialler, codec, 8 bit microprocessor, etc. The Government has taken steps to ensure continuity of supply of products and services from SCL to various users in the country.

13. Manufacture of bipolar circuits is primarily carried out at BEL which is a vertically integrated systems house manufacturing a wide spectrum of equipment required for broadcasting, telecommunications and defence. BEL manufactures a range of analog and digital bipolar ICs as also CMOS ICs of SSI to MSI complexity for consumer, telecommunication and defence applications using the 7.5 and 5 micron technologies purchased from M/s RCA, USA in the early 70s. Current wafer processing capacity at BEL is 200, 75 mm wafer starts per week. BEL has plans to upgrade its technologies and manufacturing capabilities to include both bipolar and MOS as well as BiCMOS circuits in future to realise an annual production volume of 100 million devices by

1994-95. Indian Telephone Industries (ITI), Bangalore - a PSU under the Department of Telecommunications (DOT), Government of India manufacturing a range of telecommunication equipment - has a small experimental prototyping facility for CMOS ICs and has also developed skills in VLSI design software.

V.2 R&D Laboratories and Universities

14. In addition to the industrial activity at SCL, BEL and ITI, several R&D laboratories are also active in various aspects of microelectronics. The Central Electronics Engineering Research Institute (CEERI), Pilani - a laboratory of the Council of Scientific & Industrial Research (CSIR) - has been working on IC processes and design of ASICs. With UNDP assistance, CEERI has launched a major programme on semiconductor devices and electronic subsystems for electric transportation. In addition to CEERI, other laboratories of the CSIR active in this area include the National Physical Laboratory, New Delhi - unit processes and materials technology, Central Glass and Ceramics Research Institute, Calcutta - ceramic packaging, National Chemical Laboratory, Pune - development of materials, Central Scientific Instruments Organisation, Chandigarh - capital equipment for microelectronics, Centre for Mathematical Modelling and Computer Simulation - software aspects of process modelling.

15. The Indian Institutes of Technology (IITs) at Bombay, Delhi, Kanpur, Kharagpur, Madras and Banaras, the Indian Institute of Science at Bangalore, and Jadavpur University, Calcutta are some of the major academic institutions which are involved in manpower training and R&D on various facets of unit processes, chip design and software tools for microelectronics. Some of these institutions conduct Master of Technology courses on IC technology. The Ministry of Human Resource Development has also identified microelectronics as one of the thrust areas for R&D at academic institutions and has initiated several projects in this area.

16. As part of its sponsored R&D programme, Department of Electronics has initiated several R&D projects at academic institutions, R&D laboratories and industry. As on 31st March, 1989, 25 such projects involving a total outlay of Rs.188 million had been initiated on specific aspects of computer-aids for microelectronics and microelectronics technology. In the area of process technology, projects have been initiated on thin oxides for LSI/VLSI, development of silicon on insulator structures, hybrid microelectronic sensors, development of multi-level interconnect technology for LSI/VLSI, radiation damage in MOS devices, development of process simulator, photo-CVD silicon dioxide and silicon nitride for MNOS devices, LPCVD polycrystalline silicon technology, etc. Three study reports on hybrid circuits, IC testers, and mask making techniques have also been prepared.

In the area of computer-aids for microelectronics, projects have been initiated on design of ASICs, software development for CAD of LSI/VLSI, design and development of codec filter chips, photo-mask information system, integrated design automation language, etc.

V.3 A Blueprint for the Growth of Microelectronics in India

17. Recognising the importance of microelectronics and especially Large Scale and Very Large Scale Integrated Circuits (LSI/VLSI), Government of India had set up the National Microelectronics Council (NMC) in January, 1985. NMC provides an inter-ministerial forum to oversee, coordinate and implement programmes relating to R&D, technology development and manufacture in the area of microelectronics. The Indo-US Joint Scientific Committee on Microelectronics (JSC) was also set up in May, 1986 to provide inputs to the NMC about echnology trends and strategic options for the growth of microelectronics in India. The JSC has submitted its report in June, 1988.

18. The JSC has recommended that India should become a significant force in microelectronics by the turn of the century. The objective is for India to rise to international levels of competitiveness and quality of electronic systems for which microelectronics is the enabling technology. While microelectronics constitutes only 6% to 7% of the equipment cost internationally, it is the "heart" of the product and lends it the vital competitive edge. The JSC has,

accordingly, recommended that India should become a world standard consumer (6-7%) and supplier of microelectronics. The microelectronics production targets defined by the JSC were based on projections of electronics equipment production in 1995 and 2000 provided to the JSC, using International accounting standards. The JSC also noted that investments similar to those for microelectronics would also be necessary in the electronics equipment sector to reach the targetted production levels of electronic systems.

19. The key features of the approach recommended by the JSC are :

(i) that the development should occur in the private sector.

(ii) that a set of policy measures be implemented to attract non-government money into this area from the private sector in India (40%) as also foreign sources (50%).

(iii) that the Government play the role of facilitator and catalyst by providing seed money of around 10% of the cumulative investment.

(iv) that emphasis be placed on export as well as internal market development to earn foreign exchange.

20. The recommendations of the JSC are currently under examination by the Government. On the basis of recent projections covering equipment production, microelectronics consumption, cumulative investment, etc. based on the

prevailing Indian scenario and exports, the following figures emerge :

	1995	2000 AD
	Rs.Million	
i) Electronics Equipment Production	2,00,000	4,00,000
ii) Microelectronics Consumption	10,000	28,000

The suggested values are based on the following:

i) Eighth Plan (1990-95) equipment production targets, and a CAGR of 15% for 1995-2000; CAGR for 1985-90 estimated at 33%.

ii) Microelectronics consumption of 5% of equipment value for 1995, 7% for 2000; current about 2%.

V.4 Microelectronics Production & Export

21. The Indian electronics industry is characterised by a microelectronics demand for a large variety of ICs in small quantities for commonly available diverse circuit designs and equipment as also systems based on imported know-how and components. Economies of scale may rule out meeting the entire demand for ICs through indigenous production. Current consumption and production data for microelectronics indicates that over 80% of the IC demand in 1988 was met through imports. It is, therefore, felt that about 50% of the demand in 1995 as also 2000 AD might still be met through import. It is, however, felt that with appropriate dispensations for the microelectronics industry in India, it may be possible to create an industry with large exports of about Rs.5,000 million in 1995 and Rs.16,000 million in 2000. These figures for export are at much higher levels as

compared to the recommendations of the JSC and might appear over-ambitious but are considered desirable from the viewpoint of economic viability and also in light of the Government's drive to increase exports. This level of export would also balance the foreign exchange drain due to import of ICs. By the turn of the century, the microelectronics industry in India could export more ICs than the import of ICs. The key ingredient for realising this objective would be to provide all inputs to the microelectronics industry at near international levels including interest rates on short-term and long-term loans alongwith preferential access to foreign investors to the Indian market through fiscal incentives. In view of the above, the following production and export figures are projected for the microelectronics industry:

		1995 (Rs.Million)	2000 AD
i)	Microelectronics consumption	10,000	28,000
ii)	Microelectronics production	10,000	30,000
	- domestic consumption	5,000	14,000
	- export	5,000	16,000
iii)	Import	5,000	14,000

V.5 Cumulative Investment

22. The JSC had suggested a cumulative investment to annual turnover ratio of 2:1. The experience at BEL, Bangalore indicates a ratio of 1.1:1. The plans of BEL for expansion of their technology and manufacturing capabilities also show

nearly the same ratio. It is to be noted that this ratio has been reached after several years of operation at BEL. The figures for SCL have been 7:1 for LSI/VLSI devices alone and 3:1 for the total corporate turnover including modules, sub-systems and services. SCL had indicated that with appropriate balancing of equipment capacities leading to increased throughput would enable them to reach a ratio of 1.1:1. This ratio can improve for a predominantly IC design and software-oriented activity. Incidentally, majority of the new start-ups in the USA in recent past have been in the area of ASICs. There are also successful examples of fabless microelectronics industries. In view of the above and keeping in mind the status of the local industry vis-a-vis international standards, a cumulative investment of Rs.20,000 million is likely to be needed till 1995 and Rs.45,000 million till 2000.

23. Insofar as the investment pattern is concerned, there is a view that the private sector in India and foreign investors would invest only when tangible policy measures and procedural modifications are announced and seen to be successfully implemented. It is important to note that the suggested changes in the policies, procedures, financing strategy etc. only address a part of the problems perceived by the private sector in India and expecially foreign investors. The support infrastructure covering peripheral technologies for microelectronics, modern telecommunication facilities, uninterrupted and steady power supply etc. would

have to come up to International standards for attracting foreign capital. Government would have to take a leading role in the beginning with a gradual transition to the role of a catalyst and facilitator.

V.6 Policies

24. The existing policies for electronics components, address the following main elements

- Industrial licensing
- MRTP clearances
- Location
- Foreign equity participation
- Fiscal policies
- Incentives for export

25. The following broad policy objectives are considered desirable for the growth of microelectronics:

i) Increase usage of ICs in the electronics equipment in a phased manner to international levels.

ii) Provide locally manufactured as well as imported ICs to the local electronics equipment industry close to international prices and quality.

iii) Create a business climate for setting up a strongly export-oriented microelectronics industry with investments primarily from non-Government sources.

iv) Provide a long-term, assured non-variable, fiscal regime that will enable local companies to compete with those from the pacific rim countries.

26. The first policy objective would involve promotional and fiscal measures from the Government. It would be necessary to build systems design expertise to increase the volume of electronics business as also the IC content. Microelectronics would have to be driven by market needs. Rationalisation of the IC demand in carefully chosen areas could generate viable volumes for IC manufacture in the country. Induction of ASICs with fabrication preferably in India or even abroad, if necessary, is expected to have a beneficial effect on the quality and cost competitiveness of Indian electronics equipment. Telecommunications, consumer electronics and computers could be the key market segments for fueling the growth of microelectronics. Medical instruments, smart cards, digital radios, digital TVs, card calculators, electronic toys, low-cost PCs, etc. could be some of the products which would serve as vehicles for boosting electronics production by exploiting the price elasticity of the market and, consequently, increasing the microelectronics usage. It would be desirable if ASICs could be developed and standardised for some of the above products to provide viable production volumes for local IC manufacture.

27. It is expected that Semiconductor Complex Ltd. (SCL), SAS Nagar, Bharat Electronics Ltd. (BEL), Bangalore could serve as the nuclei, to start with, for manufacture of microelectronics. It is expected that the private sector in India and foreign investors would be attracted to invest in

this area with the introduction of the proposed policy and related measures. SCL would primarily serve as a silicon foundry for volume requirements of a variety of standard parts and ASICs in NMOS/CMOS technologies. BEL would primarily serve as the bipolar silicon foundry addressing a variety of bipolar products. The distinction of IC industry into bipolar units and MOS units is no longer a technological necessity, expecially with the emergence of the BiCMOS technology. In this context, the above units could be encouraged to have a suitable mix of both bipolar and MOS processes; this would have the added advantage of second sourcing.

28. The private sector has started showing interest in investing in microelectronics. A beginning has been made through the design and software development centre of Texas Instruments at Bangalore with 100% buy-back by the parent company. SPIC electronics has already set up a modern IC packaging plant based on import of diffused wafers at Madras with an investment of approximately Rs. 150 million. With a view to attract capital in this area, it would be desirable to develop one or two demonstration projects involving foreign companies as well as local private industries to serve as role models for attracting further investment. It may be necessary to provide additional incentives/concessions etc. for this purpose based on the interaction with potential investors.

29. In addition to the above, it would be desirable to encourage major equipment houses to diversify into microelectronics to obtain the internationally recognised advantages of vertical integration and/or conglomeration. To enhance local production and to develop exports through world-wide marketing networks, initiation of assembly operations at economic scales could be liberally encouraged based on diffused wafers. Wherever major imports of electronics equipment/technologies are involed local IC manufacturers could be an integral part of the negotiations with a view to gain access to contemporary IC technologies.

VI. APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASICs)

30. The IC industry is currently witnessing the spectacular emergence of Application Specific Integrated Circuits as the fastest growing (25%) segment of the semiconductor industry which is slated to grow at a CAGR of around 15% into the 1990s. Worldwide ASIC consumption in 1988 was estimated at more than US $ 6 billion and is likely to reach over US$ 8.5 billion by 1990. It is interesting to observe that out of the new start-ups in USA over the last 10 years, about a third have been ASIC companies. The worldwide thrust is, therefore, clearly on value-added design rather than low cost manufacturing of commodity products popularly known as "jelly-beans". In fact the industry's changing perceptions have already led to major re-structuring of several US suppliers. Some acquisitions of relevance are: Fairchild Semiconductor Division by National, Monolithic Memory Inc. by

Advanced Microelectronics Devices. Texas Instruments and Intel are also collaborating on the development of cell libraries around successful standard products. VLSI Technology Inc., USA has tied up with Hitachi, NEC - the world leader in the semiconductor industry - is planning to increase the ASIC fraction of its production from 38% to 50%. Another trend is the creation of decentralised design centres by major semiconductor houses all over the world to cater to the diverse systems requirements.

31. ASICs have a special relevance for developing countries since their electronics industries are characterised by the requirement of a large number of different circuits in small quantities. ASICs permit an equipment designer to create an IC to suit his specific needs. This leads to higher reliability, reduction in volume and less cost of the end-product as compared to designing a product non-optimally with standard IC parts. Availability of powerful workstations and a diversity of technology independent CAD tools offer the equipment designer a wide choice of different implementation methodologies and foundries.

VI.1 ASIC Implementation Methodologies

32. ASIC are usually classified into Programmable Logic Devices or Arrays (PLD/PLAs), Semi-custom ICs and full custom ICs. Other user programmable devices such as ROMs and microprocessors are not normally considered as application specific elements since customization does not occur until

the parts have been delivered to the end-user. Semi-custom ICs are either based on gate arrays or standard cells whereas the Full-custom IC implementation can either be totally ab-initio design of all circuit elements or rely on a hybrid approach based on some standard cells. The most popular methodologies at present are based on gate arrays and standard cells.

33. Traditionally, IC design has used an approach where every device and circuit element on the chip is "hand-crafted" for that particular chip. The full-custom approach is suitable only when it is vital to have the minimum possible chip size or when implementing a function that is not available as an IC or cannot be configured optimally with semi-custom or standard ICs. Minimising the chip size reduces the fabrication cost and increases the yield which improves exponentially with reduction in the chip size. The major disadvantage of the full-custom approach is the time taken to complete the design for a highly complex chip, which could run into several hundred man-years of very expensive design effort. Currently, the full-custom design approach is adopted only in cases where the total number of devices per chip does not exceed a few hundred or when the circuit structure is highly repetitive or when the very large potential requirements e.g. for commodity products, justify the expenditure on design.

34. Semi-custom ICs make use of gate arrays and standard cells. The gate arrays consist of a regular array of

transistors and a fixed number of bonding pads each incorporating an I/O buffer. Gate arrays of complexities ranging from a few thousands gates to 100,000 gates are currently available. Customisation requires the designer to generate an interconnect pattern and the corresponding fabrication steps are those of metallisation and bonding. The gate array vendor or a software vendor provides the CAD tools which enable a circuit designer to customise the gate array. Designing on the gate arrays is quite straight forward and is generally favoured by system engineers for prototyping. The design time is short and the fabrication time and costs are also less as compared to the standard cell approach since only the metallisation steps are required to fabricate the circuit. However, the area utilisation is inefficient. This handicap has largely been overcome recently by the sea-of-gates approach.

3. The standard cell approach is based on a comprehensive library of well-characterised building blocks viz. standard cells. The equipment designer uses these cells to implement a circuit. The cells can be analog or digital and can have arbitrary size. The design time is longer than that for gate arrays. The fabrication time and costs are also higher since the full process requiring typically twelve or more masks is needed to fabricate the chip. The advantage is: a more efficient utilisation of the silicon area and realisability of a broad range of circuits as compared to the gate array

approach. A comparison of the different methodologies is given in Table-1.

VI.2 Techno-economics

36. The ASIC approach is adopted to perform a function that cannot be done using standard parts, or to improve the performance of existing circuits based on standard parts. A sizeable portion of the ASIC market is based on the latter. A typical example is replacing glue logic with ASICs. Usually, 7 to 8 PCBs using SSI/MSI level standard parts are replaced by a single PCB using LSI/VLSI level ASICs. A techno-economic comparison of the three implementations viz., standard parts, gate arrays and standard cells is shown in Table-2. The indicative cost comparison is given in Fig.1.

37. While designing new equipment, the designer has to evaluate the standard parts based implementation vis-a-vis the ASIC approach. Clearly, in cases where only 10 or 20 pieces of a circuit are required, an ASIC implementation may prove to be too expensive. ASICs are usually cost effective in the range of 1000 to 100,000 pieces. Each equipment manufacturer has to examine his development schedule, the total cost per gate and the risks involved. Development schedule is the time between specifying a circuit and having fully tested prototypes. This is the most important economic variable since early introduction of even a non-optimally designed product can set standards and capture a large portion of the market. It is estimated that a 10 month delay

in reaching the market place can make a product unprofitable. Total cost refers to the device cost consisting of design and fabrication costs and the systems cost including design PCB assembly, maintenance, power needs, testing etc. and the interest cost. It is necessary to reiterate that cost-benefit analysis has to be done for the product which is sold in the market and not only for ASICs. ASICs are able to compete well with SSI/MSI due to their higher level of integration. The ASIC implementation is able to score over even standard parts of LSI/VLSI complexity since the low integration level peripheral devices can now be integrated into ASICs. It appears that gates per pin is a key determinant of total IC related cost. ASICs raise the number of gates per pin from less than 10 for SSI/MSI implementation to a range of 40-200. The key issue in ASICs is design productivity, especially for complex circuits.

VI.3 Status of ASIC related activities

38. The Department of Electronics, Government of India is giving thrust to proliferating computer-aided design culture in the country to academic institutions, R&D laboratories and electronics equipment manufacturers. This is a recognition of the rapid emergence of ASICs internationally, coupled with their special relevance to the Indian electronics industry. The National Microelectronics Council has approved a 3 level structure for the area of CAD of LSI/VLSI. The structure consists of the Level-I VLSI design centre to be set up by the DOE, Level-II semi-custom design centres at academic

institutions, R&D laboratories and industry and the Level-III personal computer based design awareness activity at the engineering colleges. The DOE centre would act as the nodal resource centre to coordinate and support the activities in this area and also carry out R&D on specific aspects of chip design and software development for LSI/VLSI. The Level-II centres at the major academic institutions and R&D laboratories are expected to serve as "mother" centres for 4 to 5 Level-III centres at the nearby engineering colleges. Projects have been initated for setting up the Level-II design centres at the Indian Institutes of Technology (IITs) at Bombay, Delhi, Madras, Kharagpur, Indian Institute of Science, Bangalore; Jadavpur University, Calcutta and Central Electronics Engineering Research Institute (CEERI) , Pilani. The preliminary phase of activity for the Level-I centre of the DOE is being initiated.

39. With a view to promote and proliferate the usage of ASICs in the indigenous electronics equipment and subsequently upgrade the quality and technology of our electronic products, Department of Electronics has set up 10 VLSI design centres in different parts of the country. A Task Force, set up for this purpose by the DOE has identified the locations as also the hardware and software configurations for these centres. The design centres are located at Bangalore, Electronics R&D Centre (ERDC) - Trivandrum, Madras, Hyderabad, Centre for Development of Advanced Computing (C-DAC) - Pune, Lucknow, Gujarat

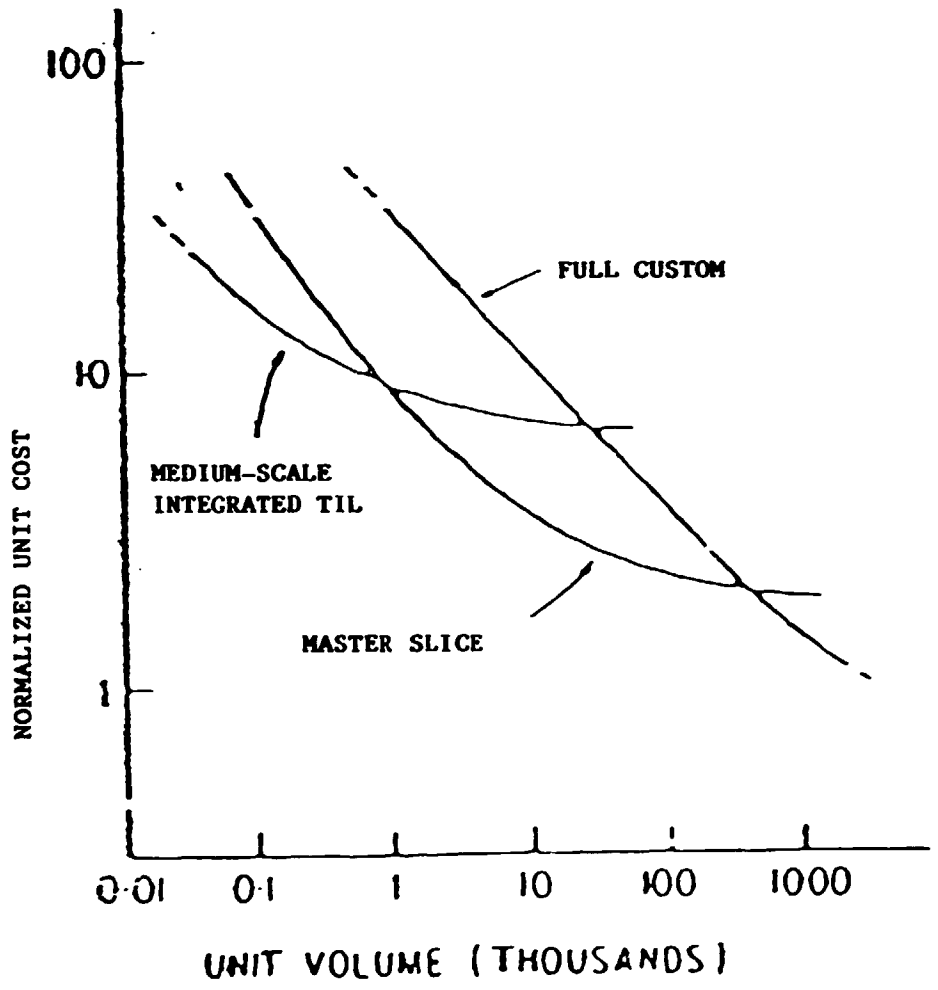
Communications & Electronics Ltd. (GCEL) - Baroda, NOIDA-Delhi, Bhubaneshwar and Calcutta. The design centres at Bangalore, Lucknow, Baroda, NOIDA-Delhi and Bhubaneshwar are being set up on a turn-key basis by Semiconductor Complex Ltd. (SCL), SAS Nagar. The centres at Madras, Hyderabad and Calcutta are being set up on a turn-key basis by ITI-Bangalore. These centres would be operated by the personnel from SCL, ITI, CDAC-Pune and ERDC-Trivandrum, respectively. The hardware and software required for these centres has been procured and the centres are at various stages of commissioning.

40. DOE is also encouraging the private sector to set up design centres. Encouraging by the success of Texas Instruments-Bangalore, other Indian and foreign companies are showing interest in setting up similar, primarily export-oriented, operations.

41. Tha awareness of the advantages to be gained by using ASICs is growing steadily in the country. SCL has already designed and fabricated over 40 ASICs for a variety of applications to cater to the prototyping needs of different users. ITI has developed a standard cell based CAD tool called Vinyas through their in-house R&D. ITI has also designed some chips for telecom applications. CEERI has designed and fabricated a VME-bus compatible controller chip for multiple channel analog data as also an IC of LSI complexity for PWM control in locomotives. TRC has also used

the software tools of M/s Fairchild, USA to design chips for PCM applications. Under the sponsored R&D projects of DOE at academic institutions, the chips designed to so far include communication chip for parallel computer, hardware accelerator for DRC, a music rhythm chip, beam former, correlator chip etc.

42. The Indo-US Joint Scientific Committee on Microelectronics (JSC) in its report entitled "Microelectronics in India - A Blueprint for 2001 AD" has also emphasised the role of ASICs in the development of microelectronics in India. Setting up of the 10 VLSI design centres for the industry by DOE with BEL/SCL/ITI as the foundries and use of foreign foundries, if necessary, is expected to trigger and catalyse the use of ASICs in indigenous electronics equipment.



Source: Sherlekar, Short-term Course on Designing with Semi-Custom ICs, August, 1986. IIT, Bombay

Fig. I

Table-1

	Gate Arrays	Standard Cells	Full-custom
1. Chip density	16-20000 gates	Hundred to many thousand gates	Hundreds to many thousand gates
2. Percent of wafer pre-processed	80-90	0	0
3. Development cost	$ 10,000 to $ 40,000	$ 40,000 to $ 1,00,000	$ 1,00,000 to $ 5,00,000
4. Ability to make design changes/ corrections	Easy, fast and inexpensive	Easy, but somewhat more expensive and slower than gate arrays	Harder, slower and more expensive
5. Unit cost of chip	High	Medium	Low

Source : Sherlekar, Short-term Course on Designing with Semi-custom ICs, August, 1986.

Table-2 : ESTIMATED COMARISON OF VARIOUS SYSTEM DESIGN APPROACHES

	TTL PARTS	GATE ARRAYS	CELL BASED
System complexity	20,000 gates	20,000 gates	20,000 gates
Average gates/IC	12	1,500	3,000
Number of ICs	1,667	13	7
Average Pins/IC	18	68	80
Total IC pins	30,006	884	560
Number of Boards	33	1	1
PCB Cost	$ 165,000	$ 10,000	$ 5,000
IC Development Cost	0	$ 260,000	$ 245,000
Excess Development Cost	0	$ 95,000	$ 80,000
Average Cost/IC	$ 0.50	$ 10.00	$ 15.00
Other cost/IC	$ 2.83	$ 20.00	$ 30.00
Manufacturing Cost/Unit	$ 5,551	$ 390	$ 315
Total Cost (10,000 units)	$ 55.5 M	$ 3.9 M	$ 3.2 M
Cost Saving	0%	93%	94%

Source : Dataquest, February, 1986.