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MICROELECTRONICS TECHNOLOGY : PROBLEMS AND PERSPECTIVES IN COUNTRIES OF WEST ASIA AND NORTH AFRICA.

The paper is a result of a UNIDO sponsored mission in Iraq, Saudi Arabia UAE (Abu Dabi), Tunisia and Morocco. The author wishes to record his appreciation to the sponsors for making his trip possible, UNECWA officials for their assistance and encouragement and UNDP officers i visited countries for their help in administrative matters and for organising certain visits. Finally, the author would like to thank the members of the mission Mr Felix Hinc and Mr Hassan Charif for their excellent cooperation and many valuable discussions. The contribution of the latter deserves special mention due to his profound knowledge of the region and extensive contacts with key people in the field which were invaluable in achieving mission objectives.

The mission was conducted in November-December 1983 and this paper is based on meetings with over a 100 people in 45 organisations spread over 25 days. The organisations covered include government ministries, national computers centres, major oil and mineral companies, investment and planning institutions, academic, R & D and manufacturing organisations. Since such an exercise was being attempted for the first time coverage has been extensive in order to obtain a perspective of the status, problems and potential for microelectronics in the region. However, these notes represent impressions of a 3 week visit only, at a given period in time, with the primary objective of preparing a backgroung paper for the experts meeting in Kuwait in March 1984.

The countries in the UNECWA region and North Africa recognize both the need and potential for the application and development of micro-electronics technology explicity is well ahead of the absorptive capacity of the region both in terms of infrastructure and human resources. Finance clearly is not a constraint, especially, in the oil exporting countries of the region. Consequently, the present situation does not tend toward a stable technological equilibrium and special efforts will be necessary both in terms of infrastructure developement and local manufacture if the present rate of diffusion of the technology, assuming effective utilisation, is to be maintened.

While special efforts to develop applications of this technology have been made in the public domain, as is evident from the chain of national computers centres that have been established, there is a considerable spread in the capabilities of individual countries. Thus, CNI in Tunis and IMEG in Casablanca/Rabat seemed to be considerably ahead of their counterparts in the other countries both in terms of human resources and methodology. Greater regional cooperation with the assistance of UNECWA/UNIDO between these institutions could go a long way in not only rectifying the imbalance but further upgrading capabilities.

In terms of industrial applications, the largest market for microprocessors based control systems was the oil production/exploration and mineral extraction/purification sectors. Thus, while ARAMCO, Saudi Arabia the largest oil exploration/production company was an impenetrable fortress tied to primarily US vendors for the both hardware/software support, the situation in ADNOC, Abu Dabi, and PETROMIN, Saudi Arabia appeared relatively more flexible with greater potential for development of local capabilities to support their future

requirements for microelectronics hardware and software. Similarly, OCP, Casablanca, Morocco and probably the Jordanian Phosphate Company are fare more open and keen to use / develop local capabilities. Another application area of considerable potential for the region was in the generation, transmission and distribution of electricity and the example of STEG, Tunis deserves to be supported and emulated. Finally, the largest potential for the application of microelectronics technology is in the education and office automation sectors as brought out succinctly in the paper of W.M. Turski provided the problem of standardisation of the Arabian character set can be swiftly and unambigously resolved.

Herein also, lies an opportunity of volume manufacture of low cost bilingual terminals and microcomputers. The efforts of Saudi Arabia (Al-Farabi computers), IMEG (low cost micros for schools) and CNI (terminals) need to coalesced and catalysed effectively by UNIDO/ECWA.

The manufacturing base in both the ECWA and North Africa region is presently very limited and would have to be considerably augmented to sustain an autonomous microelectronics industry. Given the gross national product of the region and its continuously increasing requirements for microelectronics products, there is a definite need to evolve a strategy for the development/manufacture of microelectronics products/components for the region. The present efforts at TV assembly at SADA, Morocco, SONELEC, Algeria or in Tunis and Syria nor the offshore assembly of components at SNRF, Morocco of their manufacture to a limited extent at SONELEC, Algeria constitute a viable or effective strategy for the future development. In the experience of the mission, Tunis was the only country where the potential to set up local manufacture on an integrated basis was being seriously examined, primarly, by BDET and API. Thus, BDET was talking to both Jeumont Schneider, France to establish manufacture of EPABXS (10,000 lines per year) and to COMTERM, Canada, to manufacture terminals, while API

wanted to establish of passive components i.e. resistors and capacitors. Both institutions, however, were clearly aware and concerned about the economic viability of these projects and were looking for a wider regional market.

In the author's view, exclusively national strategies cannot be pursued by individual countries in the region since the requisite combination of high per capita income and population does not simultaneously co-exist. On the other hand, the electronics market for the region as a whole is substantial enough to pursue an economically viable developped and growing at a significant rate. Two sectors which need to be singled out are consumer electronics and communications. While it was not possible to obtain any quantitative data on the consumer sector, the fact that production of color TV sets exceeds 100 per day in both Morocco and Algeria, each with a population of 30 millions approximately and 50,000 in Tunisia with a population of 6-7 millions, the color TV market in the ECWA + North Africa region as a whole ought to exceed 1,5 millions sets per annum. If to this is coupled the demand for VCRs, combination sets, calculators, personnal computers and electronic watches, this market is estimated to be in the neighbourhood of $ 2 billions.

An earlier ECWA/UNIDO study shows that the demand for telephone exchange lines is the ECWA regions is projected at 433,000 per annum during the period 1981-85 growing to 796,000 per annum between 1986-1990 with a matching demand for PCM channels. The corresponding demand for telephone sets has been estimated at 563,000 and 1,035,000, respectively. Further, the average annual investment in the regions networks has been estimated at $ 886 millions (1981-85) and $ 1,622 millions (1986-1990).

The estimate is based on a educated conjoncture given the GNP, population, present level of assembly and visibility of these products.

While no accurate estimates exist for the computer market in the region, Saudi Arabia alone has been importing equipment at the rate of $ 100 million/year during 1981 and 1982. Similarly, the requirements for microelectronics, especially, microprocessor based process controls for the oil exploration/production is significant as discussed in the report of the mission. Further, standardisation of the Arabian character set could considerably stimulate the demand for micros and terminals in schools and the office, respectively.

Given the above demand, production of a range of active and passive electronic components clearly appears to be a viable proposition. In the consumer sector for the type of products indicated above, components represent almost 40-50% of the value of these products. Similarly, in the area of switching, the cost of components per line for a system like the E 10 B of CIT-ALCATEL is $ 125/line, namely 50% of the cost per line. While clearly a more detailed study is required to accurately assess present requirements and future demand in these sectors, once this has been done, it would not be too difficult to extract a profile of component requirements both in terms of quantity and value. A priori, it would appear that adequate demand exists for establishing a viable component industry. However, it must be recognized from the outset that such an industry would only be viable if it was established on a regional basis. Consequently, standardisation of hardware must constitute an important element of such a strategy. Clearly, the regional issues involved in an industrial strategy for microelectronics need a closer examination, which is not the purpose of this paper.

Several suggestions have been made in Turski's paper for augmenting the software capabilities in the region. A complementary set of measures to upgrade the regions "hardware" capabilities is essential if a composite and autonomous microelectronics capability is to be established. These are discussed below :

There are 2 major microprocessor families with extensive applications and software currently in vogue, namely, the 8 and 16 bit families of Intel and Motorola. The orientation of the former is primarily towards the personal computer market, and even more so after IBM's entry. Motorola's 6800 and 68 000 series on the other hand are more extensively used for industrial process control applications. The applications coverage and some of the hardware features of these series is summarized in Tables 1 and 2. There are several processor, memory, interface and controller modules together with debugging software packages and development support tools available. Several major semiconductor/system companies have thrown their support behind these series, namely, HITACHI, MOSTEK and THOMSON, thus providing the requisite back up to ensure its continued use. There is a need to establish a regional capability in systems integration around such a concept. In order to ensure effective implementation of such a concept a core group of the more willing users,partly identified above, together with a group of experts from the academic sector needs to be formed with necessary support from ECWA/UNIDO to prepare a feasibility report in terms of the regions requirements in the major application areas,i.e. on exploration/production, mineral extraction/purification and power generation/distribution, etc. Based on these findings a regional centre could be created with appropriate linkages for technology transfer both with OEM suppliers of such components and system suppliers.

The key element in any future strategy to design and build electronic systems is the ability to design the silicon "chip". All IC's technology is built on the foundation of semiconductor device physics which provides the essential knowledge is semiconductor fabrication technology which allows the designed IC's to be physically constructed and above this in turn is the body of circuit and logic design knowledge. Various areas of knowledge in the manufacture of IC's have reached different stages of development, with the higher level design skills being the least highly developed. In fact, all the evidence available strongly suggests that these traditional skills will not enough for VLSI, design methodology is in essence a search for the right approach to built computer-aided engineering systems that will go on to design the IC's semi-automatically. There is a shift from hardware concepts. It appears reasonably certain that the whole area of the design of highly concurrent systems will become one of the most rapidly developing technological fields of the coming year. All these changes are likely to affect the future structure of the industry in terms of being integrated both in terms of design and fabrication as at present.

It is likely that design will become increasingly decentralised and the concept of the "silicon foundry" which does primarily fabrication develop. The emergency of the large custom and semi-custom markets in the eighties is a consequence of this change. Further, design automation systems in terms of both hardware and software in unbundled form are becoming increasingly available. The"work station" which is a low cost design system is becoming increasing viable and several of these systems are being marketed. While the concept of decentralised desgin works quite well in a "foundry" rich environment as has been demonstrated by the sucess of the "multi-project chip", in a developing

country environment it is important that local design capabilities are supported by at least a pilot level "silicon foundry" with the capability to process wafers using at least one stable technology. Obviously, local design centres could still need to have linkages with other silicon foundries in both Europe and the USA. Since the concept of the "silicon foundry" is most prevalent in the USA a list of such foundries is summarized in Table III.

A LSI design centre necessarily has 2 components, namely, hardware and software. In terms of hardware the most extensively used system by far is the VAX II/780. The system has the great advantage that most of the software packages available for LSI design can be directly implemented on it without any modifications. While it is not proposed to go into the details of the hardware configuration, the VAX II/780 uses graphic terminals which constitute the man machine interface. Depending on the configuration the hardware costs for establishing a design centre would be typically S 300,000. The design software could have to include a package for registrer level entry, a logic simulator (TEGAS, SPLICE, EPILOG), a circuit simulator, (SPICE),preferrably a processor simulator (SUPREME), an interactive graphics package (CALMA,GCI, etc...)a package for design rule check, a cell or element extractor from the lay out to verify or resimulate the logic, software for a PG tape output for mask fabrication and cell library with a data basis containing the requisite design rules i.e. layout and electrical. There are several vendors for such packages besides some of them are also available from universities in the USA. However, while integration of unbundled software from multiple sources is more economic it is also that much more difficult to implement.The output of a design centre

is a PG centre from which the mask set for processing the "chip" is fabricated, either using a laser pattern generator or a E-Beam machine. While several mask fabrication shops are available in the USA and Europe, if it is decided to set up a pilot "silicon foundry" for wafer fabrication, then it could also be necessary to set a mask fabrication facility.

As a first step it would be important to establish a regional design centre on a immediate basis for which requisite support should be provided by UNIDO. Such a centre should play a modal role in creating a chain of national design centres in a optimally cost-effective manner i.e. by shar_ the software resources. In order to ensure synergy all national centres and the regional centre should be networked together or at least linked by electronic mail. It would then be possible to rapidly create a corps of designers in the region and thus lead to rapid diffusion of the technology. An important goal of such a programme should be software development, to upgrade the design tools and build the next generation of design automation systems.

The second level of interconnection in a electronics systems is conventionnally provided using printed circuits boards (PCB),and they tend to have 2 or more levels for professional systems. The capability to design and fabricate double sided PCBs with through hole plating was only available at SNRF, Morocco a Thomson subsidiary. Similarly, the mission did not see any evidence of the design and fabrication of hybrid circuits through here again the assembly of thick film hybrids was being done at SNRF based on imported screened substrates and other active/passive components. While the ability to design and fabricate both the above components is a essential prerequisite to built microelectronics sub-systems/systems, equally important is the ability to populate and test these sub-assemblies. A regional centre needs to be

established to fill this gap with additional important function of training personnel in these techniques from the countries of the region. Support for such a concept from existing/potential manufacturers of sub/systems needs to be sought in order to promote the above concept . Further, ECWA/UNIDO could provide the necessary technical inputs needed in planning such a facility.

The region has several excellent schools of which the Technological University,Baghdad, UPM,Saudi Arabia and ENSET and ENIT, Tunisia deserve special mention. In terms of computing capabilities UPM is clearly ahead of all other institutions visited with a VAX II/780, further gives it a head sart to establish a centre for ISI design. However, as been pointed out while considerable emphasis was being placed on the applications and software aspects of microelectronics, there was an definite need to augment the hardware aspects of the technology i.e. materials science, semiconductor device fabrication techniques, CAD for chip design etc...In this context the approach of The Centre for Integrated Systems (CIS), Stanford University is worth emulating. CIS seeks to integrate solid state research and fabrication on the one side with applications on the other. The intention is to merge the three disciplines of the electronics age - computer science, information science and physical science. In order to make the system synergistic it is proposed that the scientists working in solid state physics will investigate the fundamental principles of IC's and pass their results to the IC's engineers. These engineers will use that knowledge to design new devices and fabrication

techniques, and give them to the application engineers, who turn will define new systems and integrate the chips into complete functional systems. Concurrently, the computer and information scientists are developing the tools to design ant test the IC's and so on. The concept brings together all the composite skills and tools to solve the increasingly complex problems of tomorrow.

The communications infrastructure in the ECWA region is being developed at a rapid rate. There is a general trend to shift to electronic switching systems, as witnessed in Morocco and Tunisia. Similarly, Jordan and Egypt have opted for CIT ALCATEL'S E 10 B system which is digital with Saudi Arabia having gone in for ERICSON. The impression gained by the mission was that Saudi Arabia, UAE, Tunisia and Morocco had relatively efficient telephone networks well integrated internationally. The launching of ARABSAT in october 1984 will further augment the region's capability for intra-regional communications. Consequently, the time is ripe to start planning for a multi-service national/regional network which can transmet voice, data and video signals, with the long term goal of establishing an integrated services digital network (ISDN). In particular the development of local area networks, packet switching, electronic mail and teletext/viewdata is of special significance. The need to establish common standards for the systems hardware/software is of crucial importance for the future development of microelectronics in the region and UNIDO with assistance from ITU could assist in commisioning a feasibility study in this area for the region.

The application of microelectronics in the service sectors like education health and transportation is likely to produce the greatest social benefit. The awareness of this potential was highest in Morocco

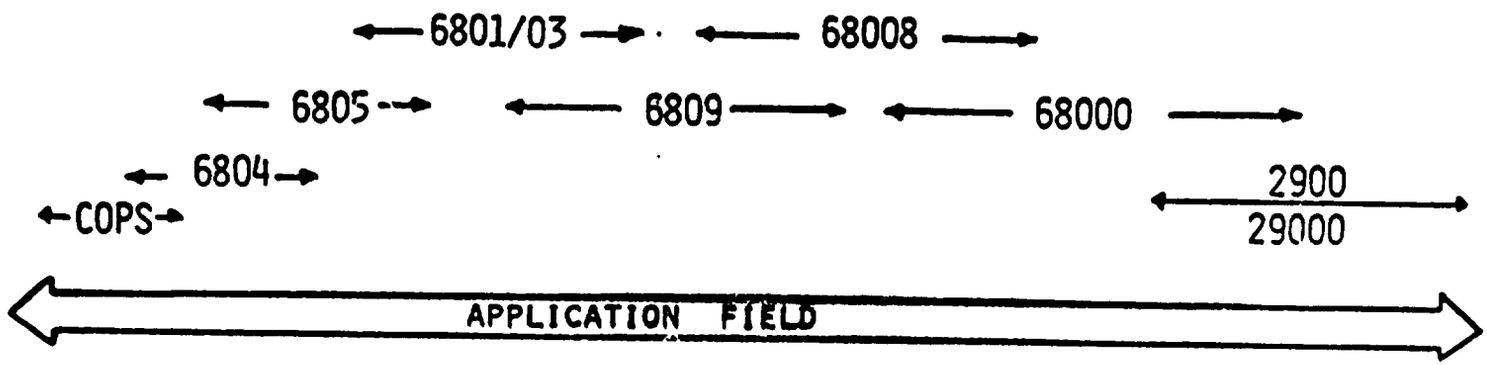
namely, at the Centre for Arabisation, Rabat and ANIT and ENSET in Tunis. There is a need to focus these efforts into a wider regional one and the methodology suggest in Oliphant's paper, "Microprocessor Applications in Developing Countries" (UNIDO, 1982), to establish a hierarchy of microprocessor applications development centres with the requisite hardware/software tools and suitable institutional support could form an useful basis for preparing an implementation plan for the region.

The problems of equipment maintenance and the lack of availability of components spares was pointed out by several organisations. Equipment maintenance can be segregated into two categories, computers and other equipment. A specialised corporation to deal with computer maintenance has been quite successful in the indian context and a modified version of such a concept to meet regional requirements merits a cluser examination. Other electronic equipment covers a wide range and spectrum and includes analytical, measuring and medical instrumentation and its maintenance in view of the large variety of types and vendors is more difficult and no simple solution exists. The programme at ENIT, Tunis to train high level technicians for maintenance needs to be more closely analysed to determine the extent of its sucess and the need for further support and diffusion of the approach. Finally, all development programmes in the region seemed to suffer due to lack of component availability one possible solution to this problem could be to set up a regional component bank which stockpiles a list of priority componentswith support from ECWA/UNIDO.

MICROPROCESSOR AND PERIPHERAL

TABLE 1

MICRO APPLICATION COVERAGE



APPLICATION COMPLEXITY	LOW				MEDIUM		HIGH	
NUMBER OF CIRCUITS	1	1	1-4	1-20	10-50	20-50	> 50	> 100
WORD LENGTH	4	4/8	8	8	8/16	8/16/32	16/32	32

M C U

REFERENCE MANUAL

TABLE 2

MCU DESCRIPTION

MCU = ON-CHIP BOARD

HARDWARE

FEATURES	LOW COST	MID RANGE	HIGH PERF.
CPU	6804	6805	6801
TYP. ROM (Bytes)	1K	2K	4K
TYP. RAM (Bytes)	32	64	128
TYP. TIMER(s)	1 x 8	1 x 8	1 x 16
TYP. I/O NUMBER	20	20 - 30	30
SPEC. PERIPH.	-	. A/D CONV. . PLL . UART	. SCI . MULTIPLIER 8 x 8
NUMBER OF PINS	28	28 - 40	40

SOFTWARE

SPECIFIC APPLICATION

CUSTOMER SELF-DEVELOPMENT

- DEVELOPMENT/EMULATION TOOL
- ROM CODE TRANSMISSION (FSE)
- ROM CODE APPROVAL (CUSTOMER)

CUSTOMER ASSISTANCE

- CUSTOMER NEEDS (FSE)
- CUSTOMER SPEC. ANALYSIS (FAE)
- PRODUCT CHOICE (FAE/LAB)
- APPLICATION DEVELOPMENT (LAB)

- SOFTWARE APPROVAL (CUSTOMER)
- ROM CODE TRANSMISSION (FAE)
- ROM CODE APPROVAL (CUSTOMER)

TABLE 3

Survey of Silicon Foundries

Company Contact Person	Technologies Available Minimum Feature Size/Gate length (minimum metal pitch shown in parentheses) nMOS Me-G	Si-G	p-MOS Me-G	Si-G	CMOS Me-G	Si-G	Bipolar	Prod. Wafer Size	Minimum Production Requirements ($ or wafers per year)	Cost Per Prototype Run (with prod. cost, if available)	Design Format from Customer
Acrian, Inc. 10050 Bubb Road Cupertino, CA 95014 (408) 996-8522 Jim Huskens VP of Mfg.	✓ 6μm (10μm)				✓ 6μm (10μm)		✓	3"	$10,000/yr.	nMOS: $3,000 per 25 wafers CMOS: $4,000 per 25 wafers Bipolar: $25 per wafer, per mask layer	Masks, Calma tape, PG tape
American Microsystems, Inc. 3800 Homestead Road Santa Clara, CA 95051 (408) 246-0330 Jerry Crosby Product Manager, COT Products		✓ 3.5μm (nMOS I) 3μm (nMOS II) 5μm, 6μm	✓ 7.5μm		✓ 7.5μm	✓ 5μm (CMOS I), 3μm (CMOS II) single or double metal		4"	Working plate plate input: $75,000/yr. PG or Calma input: 10 times engineering cost for first year	Development cost: $14,000 to $30,000	Calma tape, PG tape, working plates
ASEA HAFO 66 Bovet Road San Mateo, CA 94402 (415) 574-5400 Anders Dejenfelt Sales Manager					✓ 3μm (8μm)	✓ 2μm (10μm) CMOS/ SOS		3"	One batch (40 me-gate CMOS wafers or 20 CMOS/SOS wafers)	$20,000 (incl. mask and wafer-fab charges)	Masks, PG tape, CIF (PG tape or CIF preferred)
Cherry Semiconductor Corp. 2000 S. County Trail E. Greenwich, RI 02818 (401) 885-3600 David Pryce Marketing Manager							✓ linear, I^2L, optoelect.	3"	100 wafers/month	$3000 per engineering run (10 wafers) Prod. cost: $120 to $160 per wafer (1,000 to 5,000 wafers/mo.)	Applicon tape, Calma tape, masks, scaled drawings
Crtel 3050 Raymond Street Santa Clara, CA 95050 (408) 727-6562 Gary Hess Marketing Director	✓ 5μm (10μm)	✓ 3μm (8μm) 4μm (8μm) 5μm (10μm)	✓ 5μm (10μm)	✓ 5μm (10μm)	✓ 5μm (10μm)	✓ 3μm (8μm) 4μm (8μm) 5μm (10μm) 5μm 2-layer poly	✓ Linear 6μm, I^2L 5μm	3" and 4"	Lot: 25 wafer starts	Variable	Calma tape, masks, PG tape
Comdial Semiconductor Serv. 1230 Bordeaux Drive Sunnyvale, CA 94086 (408) 744-1800 Gary Kennedy VP and General Manager		✓ 3μm (8μm), 4μm (8μm)				✓ 4μm (8μm), 4μm (8μm), 2-layer poly, 5μm (8μm)		4"	25 wafers (Comdial specializes in quick-turnaround prototyping)	$7000 to $8000 for 3μm HMOS (10 or 15 days) $7000 to $9000 for 4μm CMOS (10 or 15 days) Consult factory for other requirements	Calma tape, CIF, masks, e-beam tape
Exar Integrated Systems, Inc. 750 Palomar Avenue Sunnyvale, CA 94088 (408) 732-7970 Tirusion Awar		✓ 5μm			✓ 5μm	✓ 5μm	✓ Linear, I^2L	3"	250 wafers/yr.	Consult factory	Calma tape, masks (preferred)

Post Wafer Processing Services (wafer probing, packaging, testing, etc.)	Normal Turnaround Time	Wafer Acceptable Criteria (std. process control monitor)	Technical Interaction Between Foundry and Customer	Availability of Design Rules for Various Processes	Must Customer Sign Non-disclosure Agreements	Simulator Parameters Available	Second-Source Agreements	Will Foundry Modify Process?	Processes Available Within Next 6 Months
(none)	Masks to wafers: 6 wks. PG tape to wafers: 10 wks.	Test monitors supplied by Actel or by customer	Initial engineering review; updates as required	All	Yes	Process simulation support via PRODEM (similar to SUPREM)	(none)	Yes	Rad-hard megabit CMOS: June 1983 Si-gate CMOS (5μm): Nov. 1983
Probing, packaging, packaged-part testing	PG tape to cut-and-go's: 4 to 5 wks. Database tape to cut-and-go's: 5 to 6 wks. PG tape to packaged parts: 7 to 10 wks.	AMI process control monitor on all wafers; will add customer PCM if requested	Formal review after each phase of AMI development cycle (optional)	Available for all processes	Yes	ASPEC	In negotiation with several companies	Yes (V_T and implants)	nMOS III (2μm): 3083 CMOS I (shrink to 4μm): 3083 CMOS II (10V): 2083 CMOS III (2μm): 1084 EEPROM process: 4084
Probing, packaging, packaged-part testing, burn-in	PG tape to wafers: 6 wks. (CMOS) 7 wks. (CMOS/SOS) Add 3 wks. for packaging/testing	ASEA HAFO-supplied process-param. modules (PPM's) and yield-measurement modules (YMM's)	Initial review	All processes provided	Yes	SPICE 2G4 and SPICE 2G5	Process is RCA-compatible	Yes, (large order)	4-inch process line with dry processing and positive photoresist 4083
Probing, packaging, testing	8 wks. (typical) Design rule check, 1 wk.; Mask generation, 2 wks.; Fabrication, 5 wks.	Chem-supplied PCM	Design reviews to establish circuit, process requirements	All	Maybe	ISPICE (NCSS)	Yes (not specified)	Yes	(none contemplated)
Probing, packaging, packaged-part testing	Masks to packaged parts (production parts, typical) nMOS, pMOS: 6-8 wks. CMOS: 7-9 wks.	Actel- or customer-supplied test circuit	Initial review	All	Yes	Electrical (not simulator) parameters supplied	(not specified)	Depends on individual case	4" bipolar capability. Dec. 31, 1983
Probing, packaging, packaged-part testing	Masks to wafers (prototype): 5 wkg. days (HMOS) 10 wkg. days (CMOS) Masks to tested wafers (Qty.: 500): 15 wkg. days	Combination customer-supplied test device	Initial review	All	No	SPICE	Unofficially, process is compatible with several large semiconductor suppliers	Open, for discussion	3-μm p-well CMOS (6μm metal pitch): 4083 3-μm n-well CMOS process: 4083
Probing, packaging, packaged-part testing	Masks to wafers out: 4 to 6 wks. Add 2 to 4 wks. for tested devices	Example customer-supplied PCM (in-house PCM preferred)	Initial review plus any required process matrices	All	Yes	(not available)	Rohm (parent company in Japan)	Yes (negotiable)	(not specified)

Survey of Silicon Foundries

Company Contact Person	Technologies Available Minimum Feature Size/Gate length (minimum metal pitch shown in parentheses) nMOS Me-G	Si-G	pMOS Me-G	Si-G	CMOS Me-G	Si-G	Bipolar	Prod Wafer Size	Minimum Production Requirements ($ or wafers per year)	Cost Per Prototype Run (with prod. cost, if available)	Design Format from Customer
Four-Phase Systems, Inc. 10700 N. De Anza Blvd Cupertino, CA 95014 (408) 255-0900 Larry Ragle Marketing Manager	✓ 7μm	✓ 5μm	✓ 8μm		✓ 7μm	✓ 4μm		3"	(not disclosed)	Typical engineering qualification run: $5,000	Working plates, PG or database tape
General Instrument Microelectronics Division 600 W. John St., C S 620 Hicksville, NY 11802 (516) 733-3611 J.E. Edwards		✓ 4μm (8μm)				✓ 5μm (10μm)		4"	50 wafers	Prototype run (including mask costs): $8000 (50 tested prototypes or 5 wafers out)	Calma GDSII tape (preferred), PG tape, masks
GTE Microcircuits 2000 W. 14th Street Tempe, AZ 85281 (602) 968-4431 Fred M. McWilliams Sales Manager, Silicon Foundry		✓ 6μm				✓ 4μm, ISO² CMOS, 4μm	✓ Linear	4"	100 wafers/yr. (engineering qual. runs: 25 wafers)	Consult factory	Calma tape, masks, PG tape
Harris Semiconductor P.O. Box 883 Melbourne, FL 32901 (305) 729-5681 Dennis Gaetano Mgr., Mktg. Planning	✓ 5μm (15μm)		✓ 5μm (15μm)	✓ 4μm (10μm)		✓ 3μm (8μm)	✓ STL, 2-layer metal, 14μm metal pitch	4" MOS; 3" bi-polar	$100,000/yr.	Consult factory	PG tape or Calma tape (preferred); masks
Hughes Aircraft Co. Solid State Products Div 500 Superior Avenue Newport Beach, CA 92663 (714) 759-2964 P. Jennifer Hufler Div. Advert. Manager					✓ 4μm	✓ 3μm		3" and 4"	25-wafer lots	Consult factory	Calma tape, PG tape
Intel Corp. 5000 W. Williams Field Road Chandler, AZ 85224 (602) 961-8051 Bob Koehler Marketing Manager		✓ HMOSI 3.5μm*, HMOSII 2μm*				✓ 2μm* CHMOS		4" and 6"	10,000 units/yr. ("classical foundry")	Consult factory	Applicon tape, Calma tape
International Microelectronic Products 2830 N. First Street San Jose, CA 95134 (408) 262-9100 Bob Gardner Marketing Manager		✓ 3μm (8μm), 4μm, 5μm				✓ 3μm (8μm), 4μm, 8μm		4"	$50,000/yr.	Prod. cost (3μm CMOS): $6500 to $8500 plus mask costs	Calma tape or Applicon tape (preferred), masks
Micrel 1235 Midas Way Sunnyvale, CA 94086 (408) 245-2500 Stan Ericsson Director, Sales-Mktg		✓ 4μm (10μm)	✓ 4μm (10μm)	✓ 4μm (10μm)	✓ 4μm (10μm)	✓ 4μm (10μm)	✓ Linear TTL	3"	25 wafer starts	Engineering run, (25 wafer starts): $2500	Database tape, masks, PG tape
Micro-Circuit Engineering, Inc. 1111 Fairfield Drive W. Palm Beach, FL 33407 (305) 845-2837 Dirk Schwebe Marketing Manager					✓ 5μm (10μm)	✓ 5μm (10μm)	✓ bFET and bMOS processes; 20V, 40V, 80V	4"	Order commitment, $100,000	(consult factory)	Calma tape, CIF, masks, PG tape

*Intel uses "effective channel length" which may be a lower number than the equivalent "drawn channel length" specified by other vendors.

Post Wafer-Processing Services (wafer probing, packaging, testing, etc.)	Normal Turnaround Time	Wafer Acceptable Criteria (std process control monitor)	Technical Interaction Between Foundry and Customer	Availability of Design Rules for Various Processes	Must Customer Sign Non-disclosure Agreements	Simulator Parameters Available	Second-Source Agreements	Will Foundry Modify Process?	Processes Available Within Next 6 Months
Probing, packaging, packaged-part testing burn-in	Masks to wafers: 4 wks (typical) Add 1 wk for assembly/test of small lots	Four-Phase or customer-supplied PCM Will also work on a good die-per-wafer basis	"Constant" interaction	All	No	Available (not specified) but "rarely requested"	(no formal agreements)	Yes	Some 4" wafer production by 4Q83 Plans to increase volume in 4μm Si-gate CMOS process by 3Q83
Probing, packaging, packaged-part testing	Calma tape to wafers: 8-10 weeks (typical) Add 2-3 weeks for packaged devices	Electrical parameters measured on GI test structures	Initial review, follow-up reviews as required	All (3μm process specs not final as of 4/25/83)	Yes	(not available)	(no formal agreements)	Yes (within limits)	3μm Si-gate nMOS process avail 4Q83 3μm Si-gate CMOS process avail. 4Q83
Probing, packaging	Masks to wafers: 5-6 weeks (typical)	GTE-supplied PCM	Periodic process and design reviews	All	Yes	SPICE, TEGAS	Mitel	Maybe (depends on size of order)	3μm, 2-layer metal Si-gate CMOS avail. 3Q83
Probing, packaging, packaged-part testing, burn-in	Calma tape to probed wafers: 10-12 weeks (typical) Add 6-12 weeks for packaged, tested parts	(negotiable)	Depends on customer requirements	All	Yes	SLICE (Harris' version of SPICE)	(none)	Yes (if it makes "business sense")	2μm, 2-layer metal CMOS, under development for gate arrays, should be avail. as foundry process by end of 1983
Probing packaging, packaged-part testing	PG tape to masks: 10 days Masks to finished wafers: 25 days	Standard Huges PCM	Periodic process and design reviews	All	Yes	SPICE (worst-case process models)	Yes (not specified)	Yes (if volume warrants it)	(not specified)
Probing, packaging, packaged-part testing, characterization (skew runs)	Database tape to tested wafers (prototype run): 9-12 weeks	Intel PCM always stepped into wafer	Intel prefers to work with customers who design chips chips using the iCEL® standard cell program	All	Yes	ASPEC (usually reqs. non-disclosure agreement)	No	No	(not specified)
Probing, packaging, packaged-part testing, burn-in	Database tape to packaged tested parts: 6 weeks (5μm) 7 weeks (3μm CMOS) (3 weeks cycle avail at added cost)	BMP PCM (preferred) or customer-supplied PCM	Initial review plus any necessary follow-up	All	Yes	Available (not specified)	Comdial (others in negotiation)	Yes (usually for eng prototype run only)	2-layer poly and 15V CMOS processes by 4Q83 2-layer metal by 4Q83
Probing, packaging, packaged-part testing, burn-in	PG tape to wafers 5-7 weeks (typical) Add 3-4 weeks for packaged, tested devices	Micrel- or customer-supplied PCM	Initial review, follow-up reviews as required	All (design rules generally supplied by customer)	No (Micrel will sign non-disct. for cust supplied rules)	(not available)	Will modify process to be mask compatible with prime source	Yes (see left)	4" wafers by 4Q83 Schottky TTL (3-μ epi) by 4Q83
Probing, packaging, packaged-part testing	Calma tape to packaged tested samples: 7-11 weeks	MCE-supplied PCM	Periodic process/design reviews	All	Yes	SPICE, ASPEC-G2	Yes Linear Technology Corp.	Yes	3μm oxide-isolated Si-gate CMOS by 12 83 20V dielectrically isolated bipolar by 12 83 40V dielectrically isolated bipolar by 12 83

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Company Contact Person	Technologies Available Minimum Feature Size Gate length (minimum metal pitch shown in parentheses) nMOS Me-G	 Si-G	pMOS Me-G	 Si-G	CMOS Me-G	 Si-G	Bipolar	Prod. Wafer Size	Minimum Production Requirements (\$ or wafers per year)	Cost Per Prototype Run (with prod. cost, if available)	Design Format from Customer
Mitel Semiconductor 360 Legget Drive P.O. Box 13320 Kanata, Ontario K2K 1X5 Canada (613) 592-5630 Gene Cohen Custom Prod. Line Mgr.					✓	✓ 3μm, 4μm, 5μm		4"	Wafer run: 20 wafers Order: \$10,000	(see left)	Calma tape, PG tape, masks
Mosfet-Micro Labs, Inc. Penn Centre Plaza Quakertown, PA 18951 (215) 536-2104 Robert O. Campbell Marketing Manager	✓ 3μm	✓ 3μm (also tung- sten gate)	✓ 3μm	✓ 3μm	✓ 3μm	✓ 3μm (also tung- sten gate)		3"	Prod. cost: \$2000 (me- gate pMOS, nMOS) to \$3500 (Si- gate CMOS)	(see left)	PG tape, masks
National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051 (408) 737-6055 Richard T. Barck Dir. MOS/LSI Mktg.	✓ 5μm	✓ 3μm, 4μm to 5μm	✓ 8μm		✓ 7μm	✓ 3μm Single and dual poly, 3μm dual metal	✓ FL, 5V Schottky; 5-100V non- Schottky; 5V gold-doped	4" and 5"	Business per family: \$150,000 to \$200,000/yr. (Not inter- ested in prototype business only)	Prototype lot charge (not incl. mask/test charges): \$225/wafer (me-gate) \$350/wafer (Si-gate)	Calma tape (preferred); Applicon tape, masks, PG tape
NCR Corporation Microelectronics Div. 2001 Danfield Court Ft. Collins, CO 80525 (303) 226-9580 Dave Newman Prod. Strategy Mgr.		✓ 3μm Single or dual metal				✓ 3μm (7.5μm) single or dual metal		4"	500 wafers for non-std. processing; 100 wafers otherwise	(consult factory)	Calma tape (preferred), PG tape, masks
Nitron 10420 Bubb Road Cupertino, CA 95014 (408) 255-7550 Robert Miller VP, Mktg. and Sales					✓ 5μm (12μm)	✓ 4μm (12μm)		3" and 4"	\$100,000/yr. (including non-recur- ring costs)	(consult factory)	Calma tape, PG tape, masks, reticles
Plessey 1641 Kaiser Avenue Irvine, CA 92714 (714) 540-9937 Peter Minett Product Mktg. Mgr.		✓ 5μm (10μm), 6μm (12μm)				✓ 2.5μm (8μm); 4μm (9.6μm), 5μm (12μm)	✓ 3μm ECL, 4μm ECL	3" and 4"	\$50,000/yr.	(consult factory)	Calma tape, masks, PG tape
Polycore Electronics, Inc. 1107 Tourmaline Drive Newbury Park, CA 91320 (805) 498-8832 S.K. Leong Vice President					✓ 7μm (>20V process avail.)		✓ Linear, P^2L dielectric isolation combination CMOS/ linear	3"	24 wafer engineering lot	Engineering runs: \$3000 to \$6000 Production costs (avg.): \$100/wafer (CMOS) \$130/wafer (linear)	Working plates
RCA Solid State Div. Rt. 202 Somerville, NJ 08876 (201) 685-6000 Jurgen W. Schmer Mktg. Mgr., Custom Products					✓ 7μm	✓ 3μm, 5μm CMOS/ SOS; 3μm, 4μm, 5μm,		4" (3" for CMOS/ SOS)	(consult factory) (RCA offers foundry services on selected basis only)	Evaluation- lot costs \$20,000-\$30,000 Tooling costs \$10,000-\$20,000	Calma tape
Semi Processes, Inc. 1971 N. Capital Ave. San Jose, CA 95132 (408) 945-1500 C.D. Detrick Wafer Service Mgr.					✓ 4.5μm	✓ 4.5μm		3"	(not specified)	Typical cost for evaluation run (CMOS me- gate): \$2500	Masks

Post Wafer Processing Services (wafer probing, packaging, testing, etc.)	Normal Turnaround Time	Wafer Acceptable Criteria (std process control monitor)	Technical Interaction Between Foundry and Customer	Availability of Design Rules for Various Processes	Must Customer Sign Non-disclosure Agreements	Simulator Parameters Available	Second-Source Agreements	Will Foundry Mostly Process?	Processes Available Within Next 6 Months
Probing, packaging, packaged-part testing	Masks to wafers: 6 weeks (typical) Add 4 weeks from PG tape, add 2 weeks to packaged parts	Motel PCM	Technical review meetings possible	All	Yes	SPICE	GTE Microcircuits	Yes (negotiable)	(not specified)
(services available locally elsewhere)	Masks to test circuits 3 to 4 weeks	(flexible)	Interaction with MML's engineers/ technicians as required	Sells layout rules for $250	—	(not available)	(sometimes)	Yes	High-voltage MOS, also working with V-groove MOS
Probing, packaging, packaged-part testing, reliability processing	Database tape to PCM-tested wafers: 6 to 10 weeks (depending on process) For packaged parts, add 4 to 6 weeks	Standard National PCM	Initial and follow-up process/design reviews as required	All	Yes	SNAP (NSC internal)	Yes (not specified)	Yes (minor)	2μm double-metal n-well CMOS: mid 84
Probing, packaging, packaged-part testing, burn-in	Calma tape to tested wafers: 6 weeks (typical)	Prefers to step-in NCR PCM	Initial review Follow-up reviews as necessary	Negotiable		SPICE	Not yet (in negotiation with 3 large companies)	Yes (depends on volume)	Will be able to manufacture devices (with poly-to-substrate capacitors) for analog functions in CMOS circuits by end of 1983
Probing, packaging, packaged-part testing, burn-in	Masks to tested wafers 4 to 6 weeks From PG tape add 2 weeks, to packaged/tested parts: add 4 weeks	Nitron PCM (preferred) or customer-supplied PCM	Initial and follow-up process/design reviews	For older processes	Yes	(not available)	Universal Semiconductor (Si-gate)	Yes (within limits)	3μm Si-gate CMOS available by 1084
Probing, packaging, packaged-part testing	Masks to wafers: 2 wks PG tape to tested devices: 6 wks	Plessey PCM	Initial review	All	Yes	SPICE	Yes (not specified)	No	2.5-μm CMOS by end of 1983
Probing, (packaging in far East and testing can be arranged)	Fast-turnaround engineering runs, masks to wafers 2 wks (CMOS) 3 wks (linear) Add 2 to 3 days for sample packaging	Polycore-supplied PCM	Initial review	All	No	(not available)	(no formal agreements)	Yes	(not disclosed)
Probing, packaging, packaged-part testing, burn-in	(not specified)	RCA's Wafer Acceptance Test (WAT) criterion	Initial formal design reviews (required)	All	Yes	R-CAP	(no formal agreements)	No	(none)
Basic testing	Masks to wafers 4 wks (me gate CMOS) 6 to 8 wks (Si-gate CMOS)	Mutually agreed-upon PCM	Periodic interaction	All	For Si-gate CMOS process only		(not specified)	Yes	5" wafer production by end of 1983

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Company Contact Person	Technologies Available Minimum Feature Size/Gate length (minimum metal pitch shown in parentheses) nMOS Me-G	Si-G	pMOS Me-G	Si-G	CMOS Me-G	Si-G	Bipolar	Prod Wafer Size	Minimum Production Requirements ($ or wafers per year)	Cost Per Prototype Run (with prod. cost, if available)	Design Format from Customer
Silicon Systems, Inc. 14351 Myford Road Tustin, CA 92680 (714) 731-7110 Bob Schultz Director, Customer Servs					✓ 7μm (12μm)	✓ 3μm (8μm)	✓ Junction-isolated (12V V_{CEO}), 14μm	4"	$20,000/yr.	(consult factory)	Calma tape, CIF, masks, PG tape
Solid State Scientific, Inc. 3990 Welsh Road Willow Grove, PA 19090 (215) 657-8400 John J. Wunner Director of Mktg		✓ 7μm			✓ 6μm	✓ 3μm		4"	$250,000 over first year	$15,000 to $30,000 to produce packaged prototypes from PG tape	Applicon tape, PG tape
STC Microtechnology 2270 S. 88th St., MD G1 Louisville, CO 80027 (303) 673-4307 Lori Hiatt		✓ 3μm (1- or 2-layer metal)		✓ 3μm (1- or 2-layer metal)		✓ 3μm (1- or 2-layer metal)		4"	500 wafers or $250,000/yr.	$10,000 for first 20 wafers	Calma tape, Applicon tape, CIF, PG tape, masks
Supertex, Inc. 1225 Bordeaux Drive Sunnyvale, CA 94086 (408) 744-0100 Richard Siegel Vice President Sales					✓ 5μm (10μm)	✓ 5μm (10μm)		4"	Lot 24 wafers	Engineering lots: $4800 to $8400	Masks
Synertek (a subsidiary of Honeywell) 3001 Stender Way Santa Clara, CA 95054 (408) 748-7045 Dan Carlson COT Marketing		✓ 2μm (6.5μm), 3μm (9μm), 5μm (10 and 11.5μm) single & double poly				✓ 2μm double poly (6.5μm), 3μm (9μm) single & double poly		4"	5 wafer runs per year (20 wafers out per run)	Production cost: $250 to $400 per wafer	Calma GDSII (preferred), PG tape, masks
United Microelectronics Corp. 3065A Scott Boulevard Santa Clara, CA 95050 (408) 727-9239 Troy Speers Marketing Manager		✓ 3μm (7μm)			✓ 5μm (10μm)	✓ 3μm (8μm)		4"	Production run: 24 wafers (engineering prototype run: 10 wafers)	Engineering wafers $200 each (minimum 10)	Calma tape, PG tape, masks
Universal Semiconductor, Inc. 1925 Zanker Road San Jose, CA 95112 (408) 279-2830 Barry Boulton Sales Manager		✓ 5μm (10μm				✓ single and double poly 3μm (10μm), 5μm (10μm)		4"	500 wafers (engineering run: 50 wafer starts)	Engineering run: $15,000 plus tooling ($25,000 plus tooling without product commitment)	Calma tape, Applicon tape, PG tape, masks
VLSI Technology, Inc. 1101 McKay Drive San Jose, CA 95131 (408) 942-1810 Tony Valentino Marketing Manager,		✓ 3μm (7.0μm) HMOSI, 5μm				✓ 3μm n-well process via Japan source		4"	Production lots: 10 wafers Prototype runs: 5 wafers Multi-product wafers (MPW) 20 packaged, unlested devices	MPW run $5000-$7500 Typical wafer charges: (4 wks. turnaround) $400/wafer (5μm nMOS) to $700/wafer (4μm CMOS)	CIF, PG tape, Calma tape, (also masks for standard processing)
ZyMOS Corp P.O. Box 62379 Sunnyvale, CA 94088 (408) 730-8800 Cliff Vaughn COT Mktg. Manager					✓ 5μm (10μm)	✓ 5μm (9μm), 3μm (8μm) in devel		4"	6-wafer prototype run plus 50 wafers/yr (eng. proto-type run 10 wafers)	6-wafer proto-type run $4800 to $5300 Production volume costs $240 to $260 per wafer	Database tape, PG tape, masks

Post Wafer Processing Services (after probing (packaging testing etc.)	Normal Turnaround Time	Wafer Acceptable Criteria (test process control monitor)	Technical Interaction Between Foundry and Customer	Availability of Design Rules for Various Processes	Must Customer Sign Non-disclosure Agreements	Simulator Parameters Available	Second-Source Agreements	Will Foundry Modify Process?	Processes Available Within Next 6 Months
Probing, packaging, packaged-part testing, high-reliability back-end screening	Masks to tested wafers: 6 to 8 wks.	SSI or customer-supplied PCM	Initial design review	All	No	SPICE	(no formal agreements)	Yes (depends on volume)	Washed emitter bipolar process available 4Q83
Probing, packaging, packaged-part testing, qualification/screening	PG tape to tested wafers: 10 to 12 wks.	Stepped-in test sites (source not specified)	Initial process/design reviews, further assistance as required	All	Yes	MSINC (SPICE available soon)	nMOS process compatible with Standard Microsystems	Yes (depends on circumstances)	(none)
Probing, packaging, packaged-part testing, characterization	Masks to tested wafers: 2 wks. From PG tape: add 1 wk. From CIF or CAD database tape: add 2 wks. To tested pkg. parts: add 2 wks.	STC PCM	Various process/layout/design reviews available	All	Yes	SPICE MOS2 model parameters	(available but not specified)	Yes	2μm Si-gate CMOS and nMOS processes, 1- or 2-layer metal by 4Q83
Custom handling	Masks to tested wafers: 4 to 6 wks. (me-gate) 5 to 8 wks. (Si-gate)	Supertex-supplied PCM	Process parameter reviews	All	Yes	(not available)	No formal agreements (claims to be mask compatible with Mitel, GTE, and AMI)	Yes	4μm Si-gate CMOS by 4Q83
Probing, packaging, packaged-part testing, burn-in	Cetma tape to wafers: 10 wks. From PG tape: 8 wks. From masks: 3 to 5 wks.	Synertek PCM required on at least 3 of 5 test sites	Depends on customer requirements	All	Required for 2μm and 3μm processes	Provide SPICE simulation (but not actual SPICE model)	Some (not specified)	Yes (implant levels only)	5" wafer processing capability by 1Q84
Probing, packaging, packaged-part testing	Masks to wafers: 3 wks. From PG tape: add 1.5 wks. To packaged parts: add 1.5 wks.	PCM (source not specified)	Initial design rule exchange/review	All	Yes	Some SPICE and ASPEC parameters available; not complete for 3μm process	Mask compatible with AMI Si-gate CMOS	Yes	3μm 2-layer metal and 3μm 2-layer poly CMOS process available by 4Q83
Probing, packaging, packaged-part testing	Masks to probed wafers: 5 wks. From PG tape add 2 wks.; to packaged samples: add 1 wk.	Prefers Universal PCM stepped in, but will accept customer PCM	Initial review, circuit design and CAD support	All	Yes	SPICE2G	Silicon++ and Nitron (others in negotiation)	No	2μm oxide-isolated CMOS by Dec. 1983
Probing, packaging, packaged-part testing	Database merge to packaged parts (MPW), 4 wks. Masks to wafers (stand-alone product) 2.5 wks.	VTI-supplied PCM	Process compatibility and prototype verification reviews	All	Yes	SPICE, ASPEC	Ricoh Corp. (Japan)	Yes (VT only for low volume)	2.5μm HMOSII available by 3Q83 3μm n-well CMOS in August 1983 3μm twin-tub CMOS 4Q83 2-layer metal CMOS available by end of 1983
Probing, packaging, packaged-part testing, high-temp and mil-std testing	Masks to wafers: 3 to 4 wks. PG tape to wafers 5 to 6 wks. Add 1 wk. for tested prototypes	ZyMOS-supplied PCM (not proprietary, available to other IC makers)	Initial and follow-on reviews as required	All	No	Most SPICE parameters available	Intel (3-μ HCMOS) Calls other processes "industry standard"	Slight adjustments only	3 μHCMOS available in 2nd half of 1983