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SEMICONDUCTOR DEVICES AND ELECTRONIC

SUB-SYSTEMS FOR TRANSPORTATION

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INDIA

Technical Report: Development of Custom Designed Monolithic Integrated Circuits

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of P. Jespers
Expert in Monolithic Integrated Circuits

United Nations Industrial Development Organization
Vienna

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PROJECT TITLE — Semiconductor Devices and Electronic Sub-Systems for Transportation

Development Objective

To promote utilization of electronic systems for transportation by:

i) increasing the operational efficiency of electric vehicles;

ii) achieve a self-reliant product development capacity;

The immediate objectives being:

i) development of power semiconductor for control in electric drives;

ii) development of custom ICs;

iii) development of hybrid integrated modules;

iv) development of system drive packages

12 April, 1985

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2. Synopsis

A global approach of PWM (Pulse-Width-Modulation) drive was undertaken in order to identify candidates for custom integrated circuit design and fabrication. Two potential circuits were defined and their specifications laid down. A work program is proposed under item 7.

Technical information about design tools, software, circuit examples as well as technology were provided.

3. Table of Contents

1. Introduction

Electronic control systems for power electric drives are of considerable interest in transportation applications such as mining locomotives, railways, trolley buses and electric vehicles. Particularly, variable frequency solid state AC drives based on pulse width modulation (PWM) offer interesting capabilities, especially with the added flexibility of microprocessors providing the software capabilities for intelligent control strategies. Typical examples are real time optimisation of efficiency, torque versus max horse power control, etc. The steady growth of interest for MPW drives results from the availability of an increasing number of hardware devices:

i) fast power semiconductors: Thyristors, GTOs as well as bipolar and MOS power transistor and Darlingtons.

ii) standard Integrated Circuits (ICs) offering a wide range of switching strategies for power semiconductors.

Hence an increasing number of hardware-based implementations have been introduced during the last ten years. Hardware implementations, however, suffer from a severe drawback. They do not allow easily changes of switching sequences such as one would require in order to optimize harmonic content, maximum voltage, carrier frequency, while providing in the same time protection against accidental short circuits of the power supply.

With the advent of microprocessors, programmability becomes possible. A microprocessor-based PWM development system offering a large flexibility to investigate the transient behaviour of drive systems is described in (1). Such a system is under development at CEERI-Pilani.

Whereas development systems make almost exclusive use of software, electrical drives must meet requirements which plead for a combination of hardware and software in order to fulfil proper noise immunity, power supply rejection, cost and volume reduction.

Custom integrated circuits offer a good compromise in this respect. They may substantially enhance the computation speed of microprocessors, implementing some of the repetitive low level algorithms, hence releasing the microprocessor from those tasks, so that more refined high level algorithms can be handled in real time. They also help to reduce the volume and power requirements replacing many standard ICs by a single one. Moreover, they enhance the overall reliability for less soldering is required.

Integrated Circuit design and fabrication, however, introduces large cost penalties which can be justified only with sufficient quantities to be manufactured. This is still a controversial matter, for semiconductor manufacturers claim usually that numbers below 100,000 are not interesting while custom design houses and silicon foundries do accept quantities as low as 10,000 and even less. Actually, 30 to 40% of the total semiconductor business already is related to customisation and higher figures are predicted within the coming 5 years. Indeed, gate-arrays with their short turn around times, relatively low cost, and complexities of more than 10,000 transistors, may substantially help to increase the share of semi-custom ICs. Similarly, standard cells, combined with an ever increasing number of software tools helping to cut design time and improve layout correctness, are attractive for complex printed circuit board(PCB) implementations. They are commonly available in design houses and silicon foundries. Combined with full custom parts, they can meet both layout efficiency and cost minimisation.

PWM systems for transportation should offer a reasonable market for ICs insofar the choices of the functions to implement are made with care. Moreover, they meet some of the points mentioned earlier, like better system performances, increased speed, smaller size and higher reliability.

A global approach of the problem, however, is absolutely necessary first. It was the cornerstone of our approach and a lot of time was devoted to this.

5. Preliminary Section

In the block diagram of the PWM development system represented at Fig. 1 of Annexure-1, power from a DC source is switched by power semiconductors, represented by block (3), themselves controlled by a pulse width modulation - PW - block (2). By repetitively switching the power "on" and "of" on to the windings of the motor during short durations and by modifying the ratio of "On" and "Off" times, one is able to control the shape of the current fed to the motor windings. Hence, current sine waves with proper phase shift can be produced.

Input signal "f" of block (1) is called the angular frequency. It controls the rotation speed of the motor. Other inputs are the feedback signals delivered by block (4) such as, Voltage and Current, Torque. They are used in order to determine the control strategy of block 1 and define the variables M (modulation index) and R (ratio of carrier frequency to angular frequency) which in turn determine the "on" and "off" times of the power semiconductors block (3).

A simple interpretation of Fig.1 may lead to the conclusion that block (1) contains the intelligence of the system, while block (2) interprets the order and executes them at the required pace. Hence, block (2) does a lot of repetetive tasks at a relatively high frequency, while block (1) controls the settings of block (2) in an adaptive manner whenever changes in the motor speed or torque are being required.

In the past, such a system was implemented at CEERI in a hardware version. Presently 40 KW drives are being developed at CEERI for mining locomotives. With the advent of microprocessors, a new dimension to adaptive variable frequency drives has been added. The word "Adaptive" should be understood time-wise as well as machinewise. In the first case, one is concerned with real time control strategies which strive to higher efficiencies for energy conservation. In the second, one considers different types of motors, all connected to the same microprocessor-based control unit, the parameters and control strategies of which are adjusted by means of proper software. In such systems, all the functions carried out by blocks (1) and (2) are taken over by the microprocessor at the expense, of course, of increased computational power requirements. Powerful microprocessor such as the 68,000 may be required therefore (Ref. 2, 3, 4, 5, 6).

In actual drives, the full flexibility of the microprocessor-based development systems is not required. Torque information, moreover, is not available. The block diagram consequently resumes to the one shown in Fig.2 of Annexure-1. The power consumption is evaluated on the basis of voltage and current data fed from 2 phases. Phase shift between voltage and current is estimated either in the filtering module or in microprocessor strategy module (1).

6. Choice of Customisable Parts

A survey of the parts of the system shown in Fig.2 which could be implemented as custom chips was carried out. The following considerations were taken in account:

- Customisation should result in enhanced performance.
- Size of equipment should be reduced.
- In the first run, digital ICs should be preferred to analog ones. This is justified by the fact that prototypes must be fabricated at CEERI. Analog MOS ICs require preferably double poly (for switched capacitors implementations) and C-MOS (for operational amplifiers). Since those technologies will be available only after some time, it was felt that any chip which could be made with the existing N-MOS, single poly technology, should be preferred.

- Programmability should be introduced in the design in order to enhance the adaptive character of the chip as much as it is possible.

During the first and partly second week, the following conclusions were gathered.

i) Implementation of the filter section of block (4) should be postponed since it is an analog IC. Presently, the filter is made by means of two cascaded low-pass second order switched capacitor filters in order to obtain a 4th order Butterworth filter. The bandwidth can be adjusted by changing the clock frequency in order to provide tracking with the actual angular frequency. The two second order sections are available as standard ICs. The remaining part of block (4) is considered hereafter.

ii) The four-channel data acquisition system which combines some standard ICs such as an analog multiplexer (MUX), a sample and hold circuit (SH) and a 12 bit analog to digital converter (A/D) was split in its analog and digital control parts. The latter is controlled by the microprocessors, to select appropriate analog channels. It sequences the analog signal through the MUX, S-H and A to D converter before sending the digital data to the microprocessor.

Standard hybrid circuits combining those analog functions and the microprocessor driven control signals do exist. They are usually designed in order to interface one or another standard bus.

It was felt that a modest implementation of the control part only of the present system would provide an opportunity to rapidly design a chip which could replace several standard ICs of one of the actual PCB boards. This circuit could be a stepping stone to later more elaborated implementations combining perhaps some of the analog functions and digital control. Eventually, filtering could be added to the chip, whether in switched capacitors form or in digital implementation.

iii) A new circuit implementing the fast repetitive tasks of the PWM algorithm was identified. It is supposed to generate appropriate timing signals for block n°3 of fig.2 at the carrier frequency f_c and with the modulation index determined by the microprocessor. It corresponds to block n°2 of the same figure. The coupling between the circuit and block n°3 should be provided by means of opto couplers.

Among additional features, pulse dropping should be mentioned. The purpose is to avoid too short extinction time of the thyristors (less than 50 micro seconds) which otherwise could damage the power semiconductors. Whenever pulse dropping is likely to occur, the circuit ideally should inform the microprocessor which then takes appropriate measures in order to avoid power transient. Whenever pulse dropping must occur, then new circuit takes the initiative and keeps the microprocessor informed for further action.

Changing of the ratio P between carrier frequency "f_c" and angular frequency "f" also must be possible. The circuit consequently must accept modifications of both R and the modulation index M, without changing the angular frequency. Means to achieve such a goal were found.

A block diagram was elaborated. It is not yet possible to evaluate the actual floor-plan. Possibly, it could require a max. 5000 transistors, which is higher than what is expected in the case of the second circuit. Its fabrication certainly represents a major step. It was one of the reasons to consider fabrication of the second circuit as well as the third. The availability of chip No.3, however would substantially improve the control strategies of PWM systems by freeing the microprocessor from time consuming repetitive computations. It could move CEERI in the forefront of electric drives, at a moment where some new IC controlled drives are just appearing on IC market (Ref. 7, 8).

7. IC Design Strategies

After several discussions about advantages and disadvantages of the circuits described above, the following conclusions were reached:

- Circuit n°2 will be designed first at CEERI keeping in mind that it should be simple enough in order to reach completion in the shortest possible period, typically 6 months.

- Mask fabrication and processing consequently could start within this year.

- Upon completion of the layout of circuit n°2, the design team should immediately start with circuit n°3, so that a successful implementation could be available for testing with the actual PWM system well before the end of the UNIDO contract.

This supposes a very tight time schedule. In order to reach max. chances of success, the following proposals were added:

- The design of the 3d (and if necessary second) circuit could benefit from computer aided design tools available at U.C.L. in Belgium, if required by CEERI. Besides, a number of existing design tools, UCL is likely to acquire commercial software packages within the coming months which substantially reduce the design effort and minimimize layout errors. In practice, a stay at UCL-Belgium of one CEERI designer during 6 months would be sufficient for complete layout of circuit $n^{o}3$.

- As soon as the layout is achieved, a trial run based on the N-MOS technology of UCL could be undertaken (6 or 3.5 micron). It would normally require 2 months, Min. 1 month, after mask fabrication.

- After successful completion of the technology, a few ICs would be delivered to the CEERI power electrical engineering group, who then could start testing the new circuit in an actual drive system. This will enable the users to ascertain proper functioning of the circuit and evaluate the value of the new global approach. New algorithms for drive control will be required to provide an objective measure for comparison between the fully microprocessor approach and the custom IC assisted one.

- CEERI then, would fabricate the same chip in its own facilities, using the same masks, or new ones in case minor modification would be required.

- Mask fabrication could proceed along different lines. In the first one, fabrication of the masks by E-beam in the frame of a multiproject chip program running at UCL is possible. It would require, however, some financial participation since masks are made outside the university.

  For the silicon-foundry of UCL, no financial participation is necessary as a contribution to the UNIDO program. In the second scenario, masks would be fabricated at CEERI, sent to UCL for IC fabrication and then returned. This second solution may be somewhat more difficult to implement because it requires clear interfaces between UCL and CEERI's Electromask machine. The distance and difficulties to establish fast contacts between Lauvain-la-Neuve and Pilani may lead to unacceptable delays. However, the second solution would provide a better entry to CEERI's fab. line.

A third possibility which was introduced recently consists to work out a co-operation between CEERI and SCL-Chandigarh's Semiconductor Complex. Not only would it provide a fast turn around time, but it would establish a very useful co-operation in the same time. Mask making would require 4 - 6 weeks and a trial run could be achieved in 3 months according to a SCL's management recent statement while visiting CEERI.

A tentative bar chart was designed. We also suggest a visit at CEERI of the chief engineer of the microelectronics facility at UCL, Mr. M. Lobet. The purpose of this visit is to help CEERI's solid state group to run the IC fab. equipment in a pilot line mode, so that fabrication of the previously described circuit could successfully be accomplished at CEERI with a fast turn around. For getting max. benefit from this visit, a number of spare parts should be purchases, however, such as mass flow meters for LPCVD system. Some consumables also should be duplicated in order to avoid exaggerated delay time.

The following steps already were taken:

a) The design rules of UCL and N-MOS 6 and 3.5 micron technologies were given as well as those for C-MOS and double poly N-MOS in 6 microns.

b) The architecture of several circuits was reviewed:

- In the frame of three lectures (see list of lectures at Annexure-2).

- Copies of UCL cell library examples were given, namely an add subcontract bit slice ALU, input and output buffers, as well as protection circuits. All circuits may enter in the design of circuit n°3 and some in circuit n°2.

- Copies of a UCL research report on a signal processing chip were given which complete the information previously made available to CEERI on a parallel multiplier IC. Besides layout, a comparative study of multiplication schemes is presented in this report. It may be helpful for the 3rd circuit.

Before closing this section, it is appropriate to stress the spirit of collaboration which evolved from joint meetings with design and power electrical scientists. Their interest has greatly contributed to useful discussions which helped to define the specifications of the third circuit. One of the assets of the UNIDO project is to have contributed to establish closer relations between solid state and power systems scientists.

We express the hope that more such examples of collaborative effort evolve in the future. Undoubtedly, the strength of CEERI lies in its interdisciplinary character. Whereas semiconductor houses such as SCL are geared rather on the production of high volume ICs, CEERI may exploit its expertise for the benefit of companies producing goods in which the added value of custom ICs opens new markets, like in transportation, industrial electronics, and some telecommunication problems (teletext). CEERI, therefore, should try to invite scientists from other sections, like industrial electronics and telecommunications, to learn design custom ICs. An appropriate internal education program should be started soon. The actual design team should be substantially increased also, in order to assist new-comers. The present inbalance between the number of technologies and designers should be reduced.

In order to successfully bridge the gap between IC designers and system scientists,it may be highly desirable furthermore to enhance CEERI's CAD tools rapidly. A number or work-stations are being developed presently which could fill the gap, the most typical one is the DAISY logician. Acquisition of design software packages, such as those from VII, Phoenix data systems, or ECAD offers a more general solution implementable on the VAX VMS 750 computer. Those programes are in fact integrated hierarchycal design tools, which combine a set of software packages, behavioural, logical, switch-level and circuit simulation tools, combined with graphical editor, design verification, compaction software, etc. They provide the user with the capability to go from any level of the design procedure to another without the need for tedious time consuming transcriptions.

Information on those software packages was provided during the stay and discussions were carried out in order to evaluate the benefits CEERI would gain therefrom in the frame of its interdisciplinary character for the design of specific ICs.

8. Other Contributions

After selection of those system parts which provide interesting opportunities for integration, more contacts with the scientists of the Solid State Technology group were established. A number of documents and information was given.

- Computer printouts describing step by step the UCL technologies for silicon gate N-MOS (single, poly, double poly) and C-MOS (6 and 3.5 micron).

- Layout rules for Si gate N-MOS 6 micron.

- Layout rules for Si gate C-MOS 6 micron, P-well C-MOS technology.

- Development of N-well, 3 micron technology (internal report UCL).

- List of procedures for cleaning, dry and wet oxidation, photoresist deposition, promotion adhesion techniques, wet and dry etching, etc.

- Report "Architecture Adaptable Pour des Processeurs Integres de traitement Numerique du Signal" - Ph.D. Theseis by Abdelhamid Maraghni.

- Report "Implementation des circuits Fandamentaux de processeurs integres de traitement numerique des Signaux" - Ph.D. Thesis by Youcel Bouterfa.

- "Layout examples" for Adder, A_bU pads, etc., description of bit slice architecture, layouts, status.

- Chapters 2-8 of the book by Prof. Jespers (pre-publication material).

- Analysis, including SPICE simulation of a clock buffer circuit used in a well known microprocessor. Discussion and synthesis. Examples of layout.

- Copy of SPICE program on VAX VMS.

Copies of papers published by Prof. F. Van De Wiele (UCL) on MOS modelling, 2D simulation, Finite element methods, solar cells, etc.