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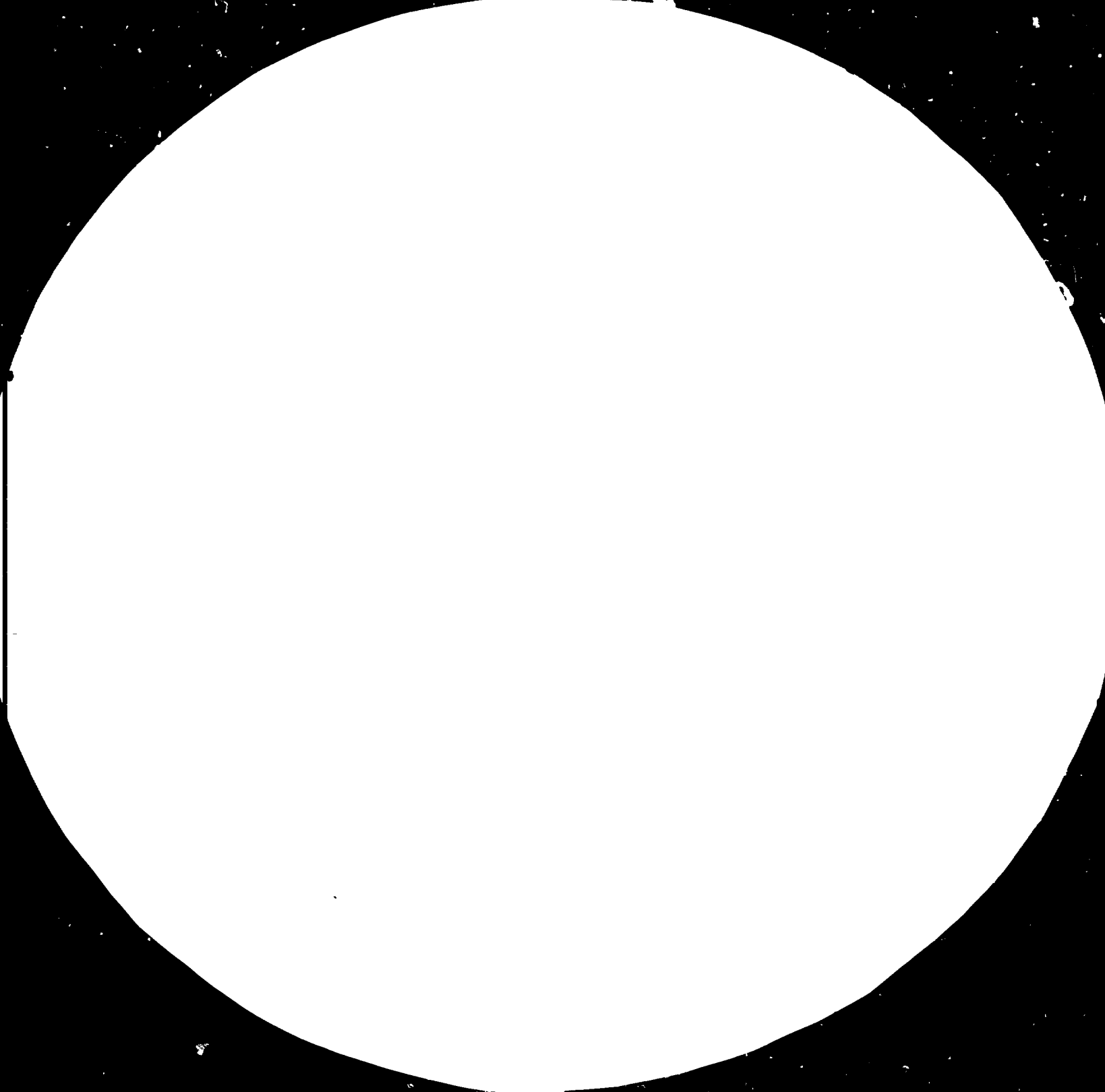

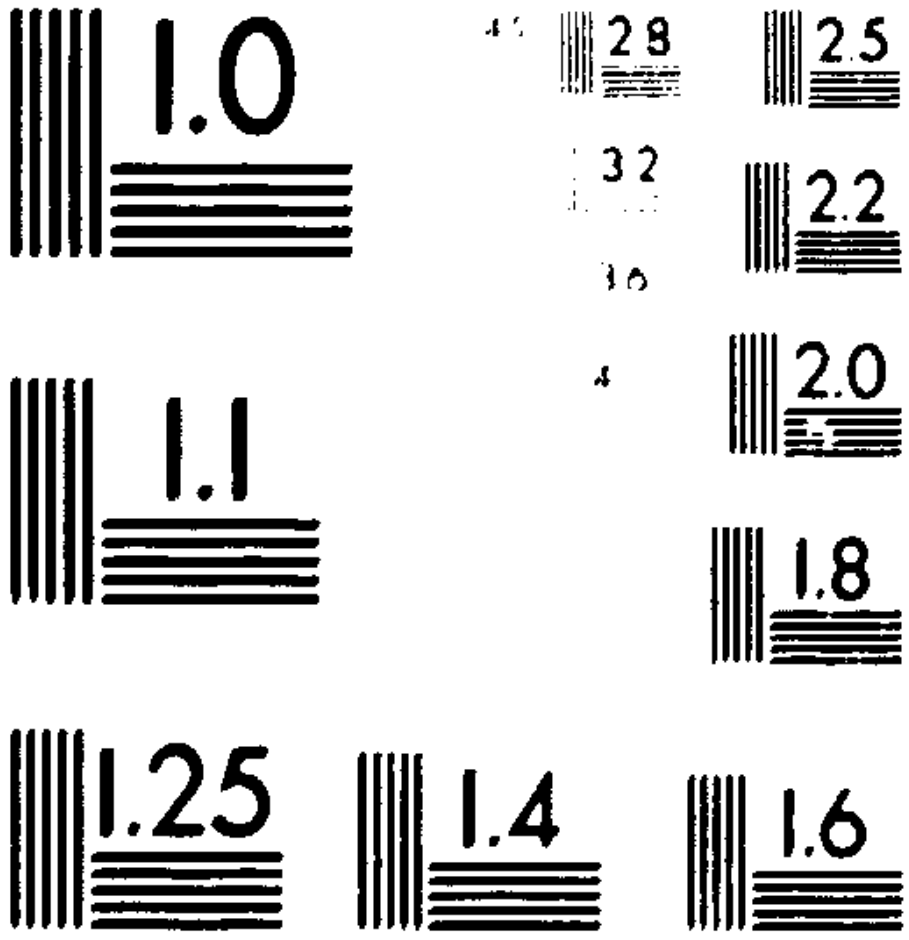

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SEMICONDUCTOR DEVICES AND ELECTRONIC
SUB-SYSTEMS FOR TRANSPORTATION

DP/IND/84/015

INDIA

Technical Report: Monolithic Integrated Circuits*

Prepared for the Government of India
by the United Nations Industrial Development Organization
acting as executing agency for the United Nations Development Programme

Based on the work of P. Rai-Choudhry,
Expert in Monolithic Integrated Circuits

United Nations Industrial Development Organization
Vienna

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Report of progress on Project - Semiconductor Devices and Electronic Sub-systems for Transportation - DP/IND/84/015 during the visit of Dr. P. Rai-Choudhury, Consultant (October 27 to November 30, 1984

Dr. P. Rai-Choudhury arrived at CEERI,* Pilani on October 28 1984. A series of discussions were held with CEERI management on various aspects of the project. The areas of materials requirement, equipment identification, training programmes, study tours, and consultants identification were discussed. Regular detailed discussions were also held with the technical staff along with follow-up experiments. The results of discussions are summarised below.

1. Materials procurement status:

   Some gaps have been identified for power devices and these are as follows:

   Pb-Ag-Sb foils: The quotation for this has been obtained and indent will be placed soon.

   Transistor packages: The package design has to be discussed by the Transistor Group with Dr. Rai-Choudhury. After finalisation of the design, a drawing will be given to Dr. Rai-Choudhury for discussions with the suppliers and for obtaining a quotation from them.

   Ag Wire:10 mil dia., nail head wire of Ag, packaged parts such as washer, phosphor bronze spring wire etc. These can be obtained only after quotations have been obtained.

   Indents, which have been submitted were also gone through. These contain: (i) spare parts for Abrasive Trimmer - for Hybrid circuits and power devices;
   (ii) spares for ion - implantation. These include a 4" baffle combination valve, which is no longer available off the shelf. The Company had informed Dr. Rai-Choudhury that they will supply a minimum of 4 numbers which is not needed by CEERI in 4 numbers. CEERI may probably skip this item.
   (iii) spares for Spray Developer.

* Central Electronics Engineering Research Institute

2. Equipment procurement status

The situation regarding the non-expendable equipment to be supplied by UNIDO was examined. Out of 13 items, 10 items have been indented. Out of 10 items, Quartz tube baking and sealing equipment (item 4), Microprocessor development system (item no.5), Bevelling contouring machines (item no.7) and Variable Frequency 3 Phase Ac Motors (item no.12) have been ordered and the rest are in the process of being ordered. Spin Etcher (item no.8) is needed urgently and as it is a custom built equipment, an order should be placed as soon as possible. For Epitaxial Reactor (item no.9), no suitable commercial model of equipment has been identified for low volume or R and D work. The existing equipment is being modified to meet current requirements.

The following software packages are identified for purchase: SUPRA-two dimensional semiconductor process simulator; GEMINI-two dimensional MOS device simulator; CAD software for Applicon AGS 861 User Programming Package for AGS 860; AGS 867- Designer Logic Package.

Due to potential export difficulty from U.S. on some of these items alternate sources from Europe and Canada will be explored by Dr. P. Rai-Choudhury. Also an assessment of the existing two dimensional device modelling programmes will be provided by Dr. P. Rai-Choudhury.

Information about small proper Wafer Scrubber suitable for R and D operation and the possibility of installation and operation without on-site training by the manufacturer for Nanospec Measuring equipment has been requested from Dr. P. Rai-Choudhury.

3. Training and Study Tours:

In discussions with Dr. P. Rai-Choudhury, it emerged that it would be desirable to have a cushion of a few months for adjusting the duration of training of some of the colleagues. It was also

suggested that the study tour under serial number 3 for power devices of 1.5 months may be combined with a saving of 2 months already effected from training on dry processing technique, as a result of training available from the manufacturers of dry processing equipment from Government funds, with another one month from the cushion mentioned above for a study tour by a senior scientist for power transistor for 4.5 months proposed to be placed at Westinghouse.

The placement of individual scientists preferably in an industrial organization is desirable. For this purpose, CEERI is preparing a resumé of individual scientists along with the description of the nature of training desired. This list will be handed over to Dr. P. Rai-Choudhury to assist with suitable placement of the individual scientists.

Study tours of senior scientists should be separated to maximise the benefit of visiting as many technical institutions and industries as possible, as well as to attend important relevant conferences. In addition, scientists during their training period should attend the important conferences on their area of specialisation.

Identification of Consultants:

Dr. P. Rai-Choudhury provided additional names of consultants from which the following have responded positively:

1. Dr. M.D. John Murphy — Solid State AC Drives
   University College,
   Cork
   Ireland

2. Prof. R.G. Hoft, — " " "
   College of Eng.,
   Department of Elect. and Comp
   Engineering,
   Columbia
   Missouri
   USA

3. Dr. Fred C. Lee, — " " "
   Virginia Polytechnic Inst.,
   and University,
   Virginia.

He will be contacting additional consultants, especially in the area of power semiconductor devices.

Technical Progress Summary:

4. Integrated Circuits

4.1 Initial Status:

Working Si gate binary counter Chips containing test structures have been fabricated. Test structures containing geometrics up to 3 µ have been fabricated. As anticipated, features below 5 µ were not satisfactory.

Problems:

1. In the processing area, Al metal step coverage problems on some wafers were encountered due to thick poly resulting from a problem in the atmospheric CVD system. Although this has been corrected, it is difficult to obtain thickness uniformity with atmospheric CVD system.

2. EB evaporation of Al also resulted in threshold voltage shifts. This is probably due to X-ray damage of the gate oxide. Because of Al penetration into Si, Al-Si alloy has been used for source drain contacts. These led to a problem of etching of the metal which tends to leave Si particles behind.

3. Another problem area is the relatively large number of printable defects due to mask defects and particulates.

Action Plan:

1. In order to have suitable control over Poly thickness, LPCVD reactor is being used which uses $SiCl_2H_2$. This reactor was originally connected for SiH_4 and was not used due to non-availability of silane. This should eliminate the step coverage problem.

2. The problem of threshold voltage shift has been resolved by using the sputtered Al-Si alloy, and modifications of sintering procedure. The damage induced by EB evaporation is further being characterised through junction leakage and MOS characteristics. It is anticipated that

the voltage of the evaporator may have to be reduced from 10 kv. In addition use of wet nitrogen for sintering to remove interface state is being attempted. Etching for Al-Si is being modified to effect complete removal of Si particles.

3. Mask defects can be reduced by a number of steps. One method will be to use two identical masks requiring double exposure. Use of this approach will result in some penalty in resolution. Second approach would be to maintain low level of defects in the mask through suitable cleaning, storage and use of proximity printing.

Additional points in Action Plan:

In order to plan work for finer geometry, use of projection printing double and triple layer resist techniques and planarisation techniques and AR cotatins were discussed. The existing mask aligner will be improved to provide proximity printing.

4.2 Power Devices:

Initial status:

Design of 100 A Darlington was completed. Masks were made. Process layout and verification were completed. 3 Runs of wafers were completed. Three fusions were completed with thin Al metallisation and Al alloying back contact on Moly. Low current up to 20 A transistor characteristics were observed.

Problems:

1. Al thickness required is about 10 micron.
2. Alloying to n^+ back should be done with Lead-Silver-Antimony for which process development is required.
3. Suitable high current d.c. and pulse testing together with dynamic testing are to be carried out for which new set-up is required.

Action Plan:

1. Sloan EB evaporator was used for depositing 5/u Al on test wafers. Thickness of the film is being checked. This will be followed by evaporation on 19 transistor fusions waiting for metallisation. In parallel Varian EB UHV System is being used to establish a thick Al evaporation capability as a back up. Both the above units require minor modifications for 10 /u Al.

2. Pb-Ag-Sb alloying process was defined. Crucibles, spacers and associated jigs were fabricated and number of alloying runs have been attempted. Results to date indicate some non-uniform wetting of the brazing alloy. A series of experiments have been planned to overcome this problem. In the meantime, additional 4 Al alloyed fusions were carried out.

3. High current d.c. testing capability was verified. On the first transistor fusion, current gain of 120 at a collector current of 120 Amp. and VCE of 1.8 V was measured. Additional circuits needed for dynamic testing are being built.

Additional points in action plan:

Thick Al evaporation will allow satisfactory contact to the emitter and the base, together with ultrasonic bonding for the base lead. Package specifications and requirements were discussed. Dimensions of the proposed package will be discussed by Dr. Rai-Choudhury with the manufacturer to initiate a quotation.

The design features of the 100 A and 300 A Darlingtons were discussed. Verification of the 100 A Dalrington characteristics using theory and experimental data is in progress. This will allow us to scale up to 300 A device.

A batch of fast switching thyristors has been fabricated by BHEL using CEERI initial design. Results of these devices were discussed, and design modifications to affect proper turn-on of the device have been proposed.

The material used for the transistor project is epitaxial silicon purchased from a vendor. In order to develop an inhouse capability experiments have been initiated to grow thick epitaxial silicon. The reactor is being modified to incorporate a 40 kw R.F. generator and provision for in-situ HCl etching.