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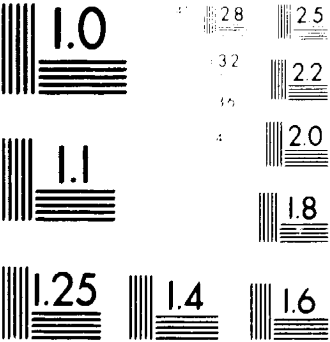

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Iraq.

A Techno-economic Study on a 'Silicon Foundry' in the Western Asia Region,

by Stephen L. Gilbert,

UNIDO consultant

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The joint UNIDO/ECWA mission to Iraq in late November-early December of 1984 was helped greatly by the excellent planning performed by ECWA personnel Dr. Hassan Charif and Dr. Ribhi Abu El-Haj. Visits with the principals in local industry and government sectors were most informative and the persons contacted were most eager and willing to discuss in detail the special problems that this issue addresses . Special mention must also be accorded the able assistance of the UNDP office in Baghdad for their assistance in logistical matters.

Two members of a French delegation from DIELI, Dr. Gerard Matheron of the Ministere du Redeploiement Industriel et du Commerce Exterieur and Dr. Rene Micolet of the Laboratoire d'Electronique et de Technologie de l'Informatique, Grenoble, joined the mission and contributed both to the discussions and to an addendum included in this report.

Introduction

The silicon foundry approach to integrated circuit design is aimed at completely restructuring the semiconductor industry in such a way that anyone with a design idea can get that idea cast in silicon at a reasonable cost. To achieve this end, "thought stages" associated with design are separated from the "mechanical stages" associated with fabrication. (2)

This inovation requires comprehensive organization to establish such a new `foundry' approach to semiconductor manufacturing. Many diverse skills are required in a complex orchestration extending over many months of constant effort to realise a finished product. Each and every step must be performed precisely and in harmony, both with the step preceeding and the one following, to yield the desired results. The technology necessary to produce microelectronic devices, such as have been created within the last decade, can, at first contact, appear awesome.

It is necessary to pursue this technology slowly and purposefully with a careful eye to precisely what benefits are desired. The nature of the technology is such that half-measures generally produce little or no results; a critial mass of resources are necessary to initiate the creative process and produce results, as resources expended at the wrong time or in the wrong areas could be entirely wasted. The competition in microelectronics in `developed' countries has shown the technology to be quite a risk; albeit a necessary and profitable one. The learning experience necessary to create a sucessful indigenous microelectronics technology requires time to mature. The establishment of a regional `silicon foundry' capability will accelerate the achievement of that maturity.

A. Assessment of Current Microelectronic Technology Base in Iraq

Throughout the mission to Iraq particular attention was paid to the operations level of semiconductor technology being performed at the various installations. It is possible to assess the level of technology in a quantitative manner by dividing along the skill levels necessary to implement a particular semiconductor operation. This is not to say that this represents a QUALITY distinction, but rather that differing skills are required to perform at each operational level.

Such a division of operations would resemble the following functional operations:

A) Assembly of complete electronic products from vendor supplied electronic subassemblies and component parts.

B) Design and production of printed circuit boards and subassemblies

C) Production of simple passive component parts, i.e. resistors, capacitors, etc.

D) Design and production of Solid State discrete active components

E) Design and production of simple linear IC's & Gate Array customization

F) Design and production of Semicustom IC's..bipolar/MOS

G) Design and production of Custom IC's..bipolar/MOS/CMOS

As one proceeds down the list, the operational level of technology necessary to successfully perform the next level is cumulative. That is to say the previous step must be performed with precision and efficiency before the next operational level can be successfully undertaken. Each successive level is dependent on the completion of the proper prior level for successful product completion.

It becomes apparent that the highest skill levels are required for design and production of fully custom IC's while minimal skill levels are required to successfully perform the assembly operations that yield a completed product. It is obvious that the initial operations attempted by developing nations concentrate on the most productive and easily achieved operational level: that of assembly operations.

More ambitious SOLID STATE operation levels require first developing a mastery of technology levels A through C before products can be achieved with any degree of success. It was with some pleasure that an assessment of the Mansour facility in Baghdad, Iraq indicated an operational technology level of E; quite an advanced level.

a) Mansour Facility, Baghdad

The mission visited the Bipolar production facility and had discussions concerning the operational capability of the facility with Dr. Adib Nu'man Abdul Aziz, Assistant Manager, Dr. Munim D. Salim, Production Engineering Manager, and other staff members.

The Mansour Semiconductor facility has been very intelligently planned to take advantage of several factors:

: The facility support functions, such as deionized water purification and air liquification, have been established as separate economic operations and provide service not only for the semiconductor facility but also serve as a central source of supply for all such high quality materials in the country. This allows the cost of the installation to be shared among other consumers of these materials such as a battery plant (uses DI water as electrolyte) and welding suppliers (use hydrogen and inert gasses from air liquification plant).

: The buildings have been designed to allow additional expansion within the complex for higher level operations without having to redesign distribution systems for most facilities. The HVAC (heating, ventilation, and air conditioning) system is configured to allow adequate environmental control for existing operations and quite possibly could form the basis for a more sophisticated system in the future. The facility was designed with the intention of continuing operations at the same site for the more difficult technical operational levels. (PMOS,NMOS,CMOS)

: The facility is quite remarkable in overcoming the rather severe environmental constraints; airborn particulate contamination during summer dust storms, waterborn contamination of silt from the Tigres River, and the great extremes of temperature experienced during Baghdad summers. Higher level operations that produce very small device features (high density devices) require very tight control of environmental conditions.

The Mansour facility functions at the level of discrete devices and although it produces linear bipolar devices (Simple Linear IC's) it has been hampered by the inability to design IC's within the facility. The original patterns for mask making are not only still `laid out' or drafted by hand but are also transfered to the final optical lithography bench by painstakingly cutting the pattern by HAND into Rubylith. It is currently functioning at an operations level of between D & E. With the addition of a suitable pattern generator to transfer designs electronically to the mask and by eliminating the hand operation steps, Mansour could be operational at level F.

b) National Research Council, Electronics Section

The mission had the opportunity to discuss the organization and direction of researches of the National Research Council with its Director, Dr. Monther Takriti, who invited the mission to visit the electronics and architecture sections.

The mission was given a tour of the Electronics Section by Dr. M.S. Abdulwahab, the head of the section.

The electronics section has been in existance for one and one half years. It is currently developing applications using discrete purchased components. These applications are directed at regional and national problems, such as electric motor power-factor controllers to conserve electrical power, and robotic controls for industrial manufacturing.

The electronics section has the potential to evaluate specific design applications by building feasibility circuits. Application specific designs are currently being evaluated by breadboarding the circuits with discrete IC's purchased from foreign vendors. Availability of the more sophisticated devices is poor and the small quantities required for feasibility studies do not provide a sufficient profit incentive to ensure adequate supply. Delays in procurement also result from restrictions on importation of electronic materials. This is due in part to local political and/or military expediencies.

The lack of a local manufacturing capability for microelectronics custom chips hinders the transfer of technical applications from the research stage to the manufacturing evaluation stage. This lack of manufacturing outlets for production of completed application designs produces a sense of frustration. This institution would be a major source of semicustom designs for regional applications should a regional `silicon foundry' come into existance.

As is common at all electrical technical institutions, in Iraq efforts are hampered by a lack of trained personnel; particularly experienced engineers at senior levels. Dr. Abdulwahab expressed a desire to have increased professional contact with electronic specialists in other Universities and institutions.

c) National Research Council, Architectural Section

The mission held discussions with Dr. R.Tabuni, Head of the Architecture Section and staff members.

The architectural section uses two-dimensional computer aided design tools (CAD) primarily as automated drafting devices. This department expects delivery of high quality Hewlett Packard computers specifically configured for drafting work along with the necessary software programs to efficiently use them. The CAD programs that perform architectural drafting are quite similar to those used to design masks for IC's and both can conveniently be run on the same equipment with little or no modifications.

Hewlett Packard also sells specific CAD programs to design masks for IC customization if it is desired not to adapt the architectural drafting program for IC design use. The computer system purchased by the architectural section is quite adequate to perform design mask customization for use in semicustom GATE ARRAY TECHNOLOGY.

d) University of Baghdad, Electrical Engineering

This department is currently teaching general engineering skills necessary to form a background level of expertise. It is not, however, producing chip level design expertise rather, teaching applications of existing chip designs, and designs involving discrete devices. The programs offered should produce competent junior engineers, talent that could perform more sophisticated work in microelectronics fabrication (Foundry) if given proper direction and leadership. It is my understanding that graduates are being further trained ON-THE-JOB at the Mansour facility to improve their skills in the fabrication techniques. This is a very valuable method for increasing the level of education and extending the technology. It is not adequate however, to educate design engineers as the Mansour facility does not currently support a design function.

e) University of Baghdad, Computer Center

A very helpful discussion was held with Dr. Salam N. Salloum, Director, Computer Science Department in regards to the computational facilities available at the University and the educational programs offered there. During the discussion it was revealed that Dr. Salloum had studied aspects of 'routing' theory used to shorten lead lengths on a silicon chip to increase the signal speed.

The Computer Center at the University of Baghdad is typical of many large university centers in that there are sufficient users to support efficiently a large mainframe computer system. This type of system lends itself well to modeling studies and theoretical analysis of many aspects of microelectronic processing. However, the state-of-the-art in process simulation does not yet allow sufficiently accurate modeling of process variables. In addition to simulation modeling it is still a necessary requirement to empirically determine the values for each process step to optimize a process technology.

The most effective computer systems for design are ones that have dedicated interactive graphics capability, similar to the small stand-alone minicomputers used by the architecture section at the National Research Council. The most powerful of these mini's, the super-mini's, are generally true 32 bit machines with dedicated microprocessors for CPU, I/O, and interactive graphics display. While the systems purchased by the architecture section are suitable for design, the main-frame computer in the University center is not and I am unaware of any super-mini's in Iraq. (CPU = central processing unit; I/O = input/ output functions)

f) National Iraqi Electronics Co.

A meeting and informative discussion with Dr. Ahmed Rafe'h, Director, preceded a visit of the factory. The Company is a mix-sector effort, 50% public..50% private shareholders.

The company is primarily an assembly operation producing one quarter million telephones, radios, and fifty thousand televisons per year. The company employs 1500 people and provides 60 % of the passive components necessary for assembly. The existing technology and designs are provided via contract with offshore vendors. A small capability to modify existing designs and/or operations to account for local conditions of temperature and voltage variations has been developed at the facility. The facility operates at levels A, B, & C

g) Ministry of Industry and Minerals

An overview of the regions data processing capability was presented to the mission by Dr. Abdulilah Dewachi, Executive Director, Information Processing Center.

The Information Processing Centre serves as a central computational facility that connects all sectors of industry and government. As a central facility it can more easily access the kinds of support necessary for specific projects. The center employs twenty programers to provide service in using the systems. The purchase of all computer systems in Iraq is coordinated through the government and one vendor's equipment predominates. This makes for good compatibility between systems and facilitates the exchange of data throughout the country. A new Hewlett Packard Model 9000 system has been purchased with software support capability suitable for two and three dimensional design. Such programs could be applied to customization layouts for mask making at the Mansour facility. The prime users at this time for such software programs are mechanical engineering designers. The capability at the Center is similar to that purchased by the Architecture section of the National Research Council.

B. Technology Strengths

A) Iraq Semiconductor manufacturing facility (Mansour Unit Operations) is suitable for addition of MOS processing IF suitable volumes of product dictate the sizable capital investment required; the facility is immediately suitable to increase the level of technology and complexity in the fabrication/design of Bipolar Linear IC's. (Note: See addendum for further details to achieve this increase)
This improvement would raise the operational level to E & F, and also allowing semicustom GATE ARRAY TECHNOLOGY to be processed at the plant.

B) Due to the selection of one vendor's computer equipment there is compatability of computer systems nation-wide which enables educational resources in design methodology to be shared in every area of the country. All sectors of the industry are connected by the central computational facility AND can communicate design informations through this network.

C) Well established University programs exist with excellent support provided at the national level of funding to educate and train new junior engineers locally, ensuring a continuing supply of indigenous engineers.

D) There are technically educated administrators in many sectors of the industry. It is evident that strong prioritys are given to technological considerations in deciding which directions to take in all technology sectors, education, research, and manufacturing.

E) Programmers are trained locally, and receive on-the-job training at the Information Processing Center or the University Computer Center. It is essential that such a cadre of programmers be developed to assist in transfering applications into silicon designs.

F) Future missions to other regional semiconductor installations will identify other strengths which could be incorporated into a regional semiconductor resource plan.

C. Technology Weaknesses

The current state-of-the-art in microelectronic technology in Iraq shows great promise and considerable expertise, however the indigenous technology effort suffers from the following problems;

A) The current production mix was not designed within the region. It was a purchased expertise which did not lead to the development of design capability locally. Tools that are supplied are used well, but the process of creating tools remains with foreign vendors. There is an attitude, apparent even to a non-native, of a certain lack of respect for locally developed products; a concern that offshore vendors products are, and will remain, superior in quality.

B) There is no in-place procedure to maintain an up-to-date technical community by continuous training and contact with state-of-the-art institutions and industry. Current process expertise is approximately 10 years out of date AND rather than catching up, is instead falling behind more rapidly. Communication with the cutting edge of the technology is a vital necessity to retain and keep the technical skills of the individual engineer at a current level of technology.

In this high technology enviornment it is not unusual for the technical staff to require about 15% to 20% of their work time during a year to be devoted to training.'(3)

C) When a contract is let to a foreign vendor to provide the tools to manufacture a semiconductor product the foreign vendor provides the design and the organization. The specifications may be provided by local engineers, but the bulk of the technical expertise is involved in the design and organization of the product. It is in this manner that the technilogical expertise of the foreign vendor is enhanced. By relegating the major elements of the process to foreign expertise, no local indigenous expertise is developed. A simplified approach to viewing this problem would be to equate the risk involved to the benefit realised. Thus if a foreign company/industry typically supplies design and guarantees the product feasibility...the local expertise;

experiences & gains
----

no risk = no ingenuity necessary to solve problem
no risk = no incentive (professional pride)
no risk = no product advantage in market
no risk = no profitability in world market

This is not a foolproof technology; learning is accompanied by mistakes and risks must be taken to develope technical expertise.

D. Regional Needs and Goals

'Many enterprises in both the public and private sectors can be expected to have a good grasp of fundamental knowledge required to have THOUGHT of the application in the first place, but not have the technical base to complete the entire application design.' (3)

It was a common complaint heard throughout the mission that efforts in several areas progressed to a certain point and then were forced to stop because the necessary connections to the next logical step did not exist. There is no continuity between research and development institutions and a distributors shelves in the marketplace. Several institutions are actively investigating state-of-the-art designs for microelectronic applications and have proceeded successfully to the feasibility stage. What remains to achieve usefulness is to link the feasibility stage with a manufacturing and distribution/service step. The region needs to make use of the potential bottled up within the research and development function without an outlet to the public sector. The region does not benefit from applications that remain only potentials.

It is desireable to create an entrepreneurial atmosphere within the technical community. This inovative spirit is directly responsible for the tremendous expansion in developed countries microelectronics capabilities. Many developing countries loose their most talented engineers to countries that provide "perks" highly rewarding that talent. Each developing country should consider what indigenous "perks" could be used to retain these talented engineers.

The path to success in applying microelectronics technology within the region will make demands on the technical commumity as a whole. The acceptance of `traditional' methods of achieving certain ends must give way and yield to new techniques. The microelectronics applications are most likely to manifest themselves in areas where the information processed is not conveniently verified by any individual, (as in the case of mask layout designs) producing a doubt in the minds of many as to the accuracy of the results. This inability to verify, to confirm the results is a condition that must be accepted to enable the valuable conclusions to be applied with confidence.

A decentralized design philosophy is appropriate for the region. The designer needs only the application design criteria and the design rules for the particular technological process to perform his task. It is not necessary for the design center to be located in close proximity to the fabrication area. It is necessary , however, for the design center to be staffed by a technical staff of sufficient `technical mass' to handle any applicatons that might be encountered at the particular location. The nature of the design function is special in that solutions to individual design applications can be applied in whole or part to many other applications. This indicates that the maximum interaction between designers would accelerate their learning and efficiency. Designers are creative elements within the microelectronics field and require a certain level of interaction among their collegues to maintain a level of "mental health". Accordingly while it is feasible to locate design installations remotely from the fabrication facility it is imperative that good comunications be maintained between design facilities and the fabrication facility. By dispersing design centers throughout the region a closer contact can be maintained between the designers and the users of applications.

E. Plan of Action:

A successful plan of action in applying microelectronics technology could be organized along lines consisting of functional divisions and implemented by programs designed to achieve specific goals independently o lines consisting of functional divisions and implemented by programs designed to achieve specific goals independently of each other. Such programs can pursue several activities in parallel when organized and executed with close coordination. To be successful it is necessary to identify quite precisely the specific goals that are desired and set priorities to control the timing and use of generally scarce resources; both technical and economic.

Let us assume a list of desireable goals that could be attained from those proposed in conversations held with industry principals throughout the mission:

1) technical proficiency of regional applicions
2) economic viability of regional application
3) regional selfsufficiency in microelectronics
4) ecomonic viability on a world scale in microelectonics

In order to achieve these identified goals one must set priorities, consider which goals have common elements among them, and then organize a program of action to achieve the common elements; thereby securing the maximum value from expended resources.

One can now consider a three fold approach in developing an action plan:

1............ Define priorities;

a) To aquire advanced technology in microelectronics to intelligently direct and guide the technology applications to extract the maximum benefit from the technology for the region.

....meets goal 1

b) To develope regional self-sufficency in ALL aspects of microelectronics technology; i.e. microprocessor design and manufacturing; microcomputer design and manufacturing; assembly of region-specific applications, etc.

....meets goals 1,2,3

c) To compete on an international scale to preserve foreign capital and reduce balance of payments due to importation of electronics, both components and assemblies in the commercial and consumer sectors

....meets goals 1,2,3,4

At the present technical level of operation, attempting to achieve goals 3 and 4 would be very expensive and in my opinion totally inappropriate for the developing microelectronics industry of the region. Rather, the strengths identified previously should be built on and enhanced, while improvements made in the areas' considered shortcomings. This emphasis applies to BOTH the "hardware" aspects of the technology and the "applications/design...or software" aspects.

"In the inexperienced hand any tool reverts to a hammer" (7) The microprocessor and other microelectronics "hardware" need appropriate programs and applications to fashion the technology into something more than just an expensive hammer. A demonstration project is necessary to achieve credability and show a positive benefit from the technology. Even if offshore hardware capabilities are used to achieve results, it would prove a valuable example throughout the region and serve as a model to emulate.

A particularly interesting evaluation can be made utilizing an "Added Value" concept (3) as applied to growth in engineering capability, in that if considered the primary yardstick for evaluating microelectronics progress due to an activity, then the process becomes straightforward and successfully integrates the quite diverse factors of economics and regional selfsufficiency.

The main advantage to microelectronic technology for developing countries is that a single program can sucessfully handle many simultaneous similar applications even where only unskilled personnel are available. With the aid of such a programmed calculating device the expertise of the programmer is extended and reproduced at every location where the program is utilized. It is then obvious that the most capable and appropriate programs need be developed.

'By putting the computing power of a large main-frame computer on a chip costing just a few dollars, by making these chips cheap and easy to use, and with skill requirements predominantly in software programming capability, microprocessor utilization comes well within the reach of developing countries.'(5)

2.............Identify Program Elements

1) MARKET SURVEY to determine what specific applications need be addressed, and what quantity of devices are required to satisfy the need. Reference (3) will provide details and important insights into required informations "Product Marketing"

2) Initial DESIGN SPECIFICATIONS GROUP, reduces applications to semicustom gate array logical design functionality

3) Offshore supplied GATE ARRAY MASTERSLICE customized locally for the application design to gain experience in semicustom fabrication

4) SILICON FOUNDRY developes REGIONAL capability to produce PMOS/NMOS/CMOS masterslices achieving regional independence in GATE ARRAY technology.

5) Improve/establish LINKAGES between the regions Universities and industry.

6) Consideration must be made to the DISTRIBUTION, SERVICE, AND MAINTENANCE networks for products see (3)

Product Marketing Concepts are at the crux of the current consideration, where to go after preliminary engineering feasibility, what scale manufacturing is necessary to meet future demands for the product? What price should be charged to make manufacturing feasible? All these questions demand answers before a silicon foundry can be justified. 'It is important to recognize that Product Marketing is responsible of IDENTIFYING the correct market conditions.'(3)

It is very important to realise that education in this field is not and cannot be stagnant. In other engineering fields you would not hesitate to reject outmoded techniques of construction, architecture, or transportation 30 years out of date. In the semiconductor field 5 years is equivalent to 30 in more traditional engineering fields. Design engineers must constantly improve their skills by working on successful applications, it is a learning experience necessary to retain competence.

It is essential that appropriate linkages are created between University workers and the developing industry. One must realise that the designers trained within the university system are the CONSUMERS of microelectronic technology. It is these engineers that will choose the particular microelectronic device used to accomplish the application. It is unreasonable to expect local engineers trained to use foreign products exclusively throughout their education, and taught that these devices are superior, to adapt locally produced devices into their application designs. If one were to use the same mindset within another industry, say chemical refining, and asked engineers to change their choice of equipment manufacturer to one they had no experience with, you would have a sizable argument!

3...............Recommendations

Planning for a regional 'silicon foundry' must provide a global viewpoint which connects the entire process of utilization of microelectronic technology; inception/design/inplementation /manufacturing/distribution/maintenance should all be considered in both a local and regional perspective. It may be productive to combine functions in certain geographic areas and separate them in others. Careful consideration should be paid to the possiblity of dividing technologies, such as bipolar and MOS operations between different member states to avoid redundancy of effort.

I recommend accelerating the development of application programming and design development expertise by utilizing offshore vendor-supplied GATE ARRAY MASTERSLICE TECHNOLOGY, utilizing a SINGLE LAYER CUSTOMIZING STEP, METALIZATION, to produce semicustom logic schemes dedicated to applications indigeous to the region.

The fabrication process at a US silicon foundry, MOSTEK, was simplified to one product, an MOS GATE ARRAY MASTER SLICE. MOSTEK had produced a variety of MOS products prior to takeover of the company by UNITED TECHNOLOGIES. After the takeover a new philosophy was imposed on the fabrication process to produce a single product suitable for almost all applications in the company. MOSTEK choose NMOS technology as its single process standard and proceeded to adapt its production to that single technology.

In order to produce the wide variety of applications necessary for such a large company, the fabrication processing of the silicon wafers is halted just before the final interconnections of transistors is performed by etching the metal interconnect layer. At this stage a special semicustom mask is used to apply the custom design pattern from the design section computer by means of a photolithography procedure. The final metal interconnections are then formed by etching metal lines between each transistor necesssary in the applied pattern, producing a semicustom device. The GATE ARRAY approach has the highest flexability in product applications primarily because changes from application to application are made only in one process step, the metal level mask, and the rest of the fabrication process remains unchanged. This approach makes minimal changes in the more difficult steps of the fabrication process and results in an optimal yield.

'The METALIZATION step is the process where all the individual transistor on the chip are interconnected into an "integrated circuit". A thin metal layer is evaporated onto the silicon wager under vacuum conditions. A photoresist step exposes a semicustom mask whose pattern defines the specific application the device will serve. The metal is etched away leaving interconnections to satisfy the logical requirements of the design engineer. It is this step in the process that differentiates gate array devices into the different applications.' (6)

This GATE ARRAY approach is viable for PMOS, NMOS, and CMOS masterslice technologies as suitable design software is developed. Logical design software can be written such that the applications designer is unaware of the particular technology actually used to construct his device.

The GATE ARRAY approach is also viable from a hardware perspective. Since the design methodology is independent from the process technology, a simpler process can initially suffice to begin indigenous production via a regional foundry such as Mansour. This would enable a PMOS masterslice process to satisfy the starting requirments for product, allow changeover to NMOS masterslice production when it becomes a viable process, and ultimately permit utilization of a CMOS masterslice process when it is supportable at a regional facility. It should be pointed out that this sequence of processes corresponds to the historical development of the technology AND reasonably expresses the relative degree of difficulty in implementing the repective technologies. I do not believe it adviseable to attempt to circumvent these process learning steps by leaping into a more advanced technology before perfecting the predecessors.

At the present time a GATE ARRAY approach could be started with no in-house masterslice processing at the Mansour facility. Mansour has the capability to utilize vendor-supplied masterslices and also to manufacture the metal level customizing mask. What would be required is an optical pattern generator to transfer applications designs from computer tapes into processing masks to customize the purchased masterslice into a finished product.

The etching and mask processes are currently supported in the bipolar lines and would need minor changes to implement this step for GATE ARRAY masterslice customizing. An interactive graphics mini-computer system, possibly a HP 9000, would also be required to complete the automatic handling of design data and could also serve to make minor corrections as very few designs are totally error free.

It is imperative to share the scarce resource of technically trained personnel within the region. Currently technically trained persons are lost to the technical community by vertical mobility. The trained people are successful and rapidly advance to the administrative levels where there exists a great need for their talent. This advancement, while necessary, contributes a significant drain on scarce technical resources. Concurrently, the administrators find little opportunity within their administrative functions to retain their technical expertise and become 'obsolete' in their fields within a short span of years.

UNIDO/ECWA could serve as a coordinating organization to initiate regional information exchange via lectures and symposia. They could also organize a series of short courses presented by experts from outside the region and attended by WORKING engineers to accelerate learning in state-of-the-art technologies. It was suggested at the University of Baghdad that some form of faculty exchange between Universities both within and from outside the region would enhance the flow of new technology into the educational sector. Included in the appendix are brochures illustrating the nature of activities currently being pursued in developed countries to achieve this technology transfer.

It would be advisable to consider the experience of the French in creating a design capability. The creation of such an infrastructure as a result of government policy does not parallel the path followed by most developed countries, where a strong profit motive and abundant venture capital provided motivation. Their experience may provide addition insight into other possible alternatives.

The capital investment required both in personnel and monies would be reduced by approximately 15 % over what had previously proposed, $ 50,000,00 US.(6), if the silicon foundry was incorporated into the Mansour site. The savings would be due primarily to the sharing of existing support facilities, namely the Deionized water supply and the Air liquification plant. The personnel could also share management structure and administraive support functions.

It is feasible to share costs of such a facility by the formation of a syndicate of investors, quite similar to the approach in developed countries, that would limit the financial exposure experienced by each individual member, and would distribute income and products within the syndicated area. Several regional financial groups have expressed interest in the microelectronics technologies supported by such a silicon foundry approach. (1)

`Developing countries should not set up plants to manufacture products that must be manufactured in "high level" technical operations to meet the cost and quality standards needed for international competitiveness, where the constant rate of change of technology is discouraging to newcommers, and entrenched competitors enjoy substantial marketing and production advantages.'(5)

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Addendum

Special Addendum in reference to Mansour Unit Production

by Dr. Rene Micolet

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The Mansour Unit has been implemented for the production of Silicon Bipolar Transistors (NPN,PNP) and linear int

The Mansour Unit has been implemented for the production of Silicon Bipolar Transistors (NPN,PNP) and linear integrated circuits. The IC's produced by this plant are based on SGS-ATES technologies, and for applications in the field of professional (operational amplifier) and entertainment equipment (radio, TV).

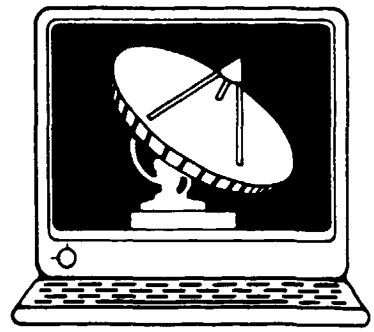
In fact, the field of applications of such processors is much larger than those corresponding to the present production, and there would certainly be good opportunities to satisfy other needs of the market with the same family of processes. Potentially, these processes may be used to produce perhaps nearly all circuits working with a voltage supply 1 to 45 V (depending on the characteristics of the epitaxial layer) and operating frequency approximately equal to 50 MHz and a power dissipation 0.5 to 5 Watts (depending on the package chosen). Moreover, one process could be adapted to integrate mixed linear and logic functions, the latter being based on I"Squared"L structures with bipolar transistors.

Generally speaking, it is probably not worth to continue in the area of standard ICs whose market prices are very low due to strong competition. It seems rather more promising in the future to develop original ICs for special purposes (the so-called ASIC: Application Special ICs): CMOS is, of course, the dominant technology for ASIC, but there is a niche for the bipolar ICs whose processes have been experimented in Iraq. This niche exists for example, when there is a need for low noise at the imput (to amplify small signal delivered by sensors with possibly added logic) and/or high power at the output (to drive lamp relay, motor), or relatively high frequencies. These new trends would certainly imply the implementation of design centers with trained people, aimed at developing the creativity of engineers in close contact with the equipment manufacturers.

Appendix

Electronics

In Minnesota, high tech begets high tech. With homegrown titans such as Control Data, Honeywell and Minnesota Mining & Manufacturing (3M) nurturing new enterprises, developing new products, providing executive talent, venture capital and exchange of ideas.



From the small job center started a generation ago by Engineering Research Associates in St. Paul came Sperry's Computer Systems Division (then called Univac) and Control Data, which in turn, have launched more than 60 other high tech companies. At this same time in 1956, IBM chose Rochester as a manufacturing site. Today, the IBM Rochester facility employs 7,100 people in manufacturing and development on 593 acres, while Sperry has recently opened a $175 million semiconductor facility and moved six of its ten corporate technology research centers to Minnesota. Combined, all of these companies produce a diversity of electronic products including computers, hardware, software, semiconductors, manufacturing and testing, measuring and controlling devices, communications equipment and robotics.

Fast-growing small and medium size high tech firms have enjoyed explosive growth here. CPT grew 14 times larger in one decade. Data Card expanded seven times larger during the same period. Cray Research grew from 21 employees to 1,336. Control Data doubled its home state work force to nearly 23,000. Honeywell increased its headquarters employment by 13% and is spending $43 million on buildings and additions. And on northern Minnesota's Iron Range, noted for its gigantic taconite processing plants, Hibbing Electronics has expanded five times in 10 years, from a handful of employees to more than 400.

Minnesota ranks third in the nation in the dollar volume of electronic computer equipment sold by United States companies. Minnesota computer, peripheral equipment and related parts manufacturing plants total over $3.4 billion annually.

Much of Minnesota's success in capturing such a large share of high tech industry is attributed to its founders and leaders who are native Minnesotans. They know the state, its values, its benefits. And they are eager to attract new high tech ventures to Minnesota.

Education: high standards, high goals.

Minnesotans are keenly aware of the relationship between the quality of the state's education system and the technological progress vital to the state's economy. Governor Rudy Perpich has expressed his intent to make Minnesota "the brain power state in the nation" recognizing that an investment in education is an investment in Minnesota's economic stability and quality of life.

In 1983 the Minnesota Legislature passed the Minnesota Education Technology and School Improvement Act for K-12 public education. Its total approach to the use of technology in the classroom is heralded as one of the best in the country. Continuing innovations include the Talented Youth Math Program (where gifted secondary students move on to study in collegiate programs) and teacher upgrading programs with special motivations for further study and assignments.

Minnesota's commitment to quality post-secondary education is broad-based, including the humanities and arts, and extends across the full spectrum of educational opportunities. The state has 33 Area Vocational-Technological Institutes, 22 public and private community colleges, 24 private liberal arts colleges, 7 state universities, and 5 University of Minnesota campuses. Four-year engineering programs are now offered at Mankato and St. Cloud State Universities as well as at the Duluth and Twin Cities campuses of the University of Minnesota.

Minnesota's public and private colleges and universities offer education in computer-related fields, such as aerospace studies, computer science and microcomputer studies, data processing, nuclear medical technology, pre-engineering and mechanical and electrical engineering technology as well as in other professions and the liberal arts. In fact, Minnesota's private colleges and universities account for as much as 50 percent of the state's Baccalaureate Degrees in physics, chemistry and mathematics.

The University of Minnesota offers high tech excellence in many areas. The Twin Cities campus is the largest urban campus in the country, and one of the nation's major research universities located in a metropolitan area. Within the University's Institute of Technology, the Department of Chemical Engineering ranks first and the Department of Mechanical Engineering ranks fifth nationally.

The University of Minnesota is working hard to put Minnesota among the top eight graduate schools in the country by 1991, seeking more research support and academic chair endowment from state and private sector partnerships.

Similarly, the goal of the University's new Super Computer Institute is to retain Minnesota's worldwide super computer leadership, a role coveted by Japan.

R&D funding will rise to $110 billion in 1985

Our annual forecast finds planned funding going up by 13.4% overall. Federal funding increase leads the way, but industry still is major source of dollars.

C.J. Mosbacher
Executive editor, *R&D*

NO RECESSION FOR R&D. That's the 1985 scenario based on the studies leading to our forecast of $110 billion total funding for this year.

Compare that to the total United States economy. The consensus of economic studies in late November called for real growth in the gross national product (GNP) of 3 to 5% in 1985. Inflation is expected to stay low at 4 to 5%. Thus total growth of 7 to 10% is foreseen in the year ahead, barring calamity.

But, again barring calamity and using a revision of our 1984 forecast as a base, R&D funding should rise 13.4%. The implication is that the proportion of GNP spent on R&D will continue to increase, as it has each year since 1978. In 1984, 2.7% of GNP was spent on R&D in the United States.

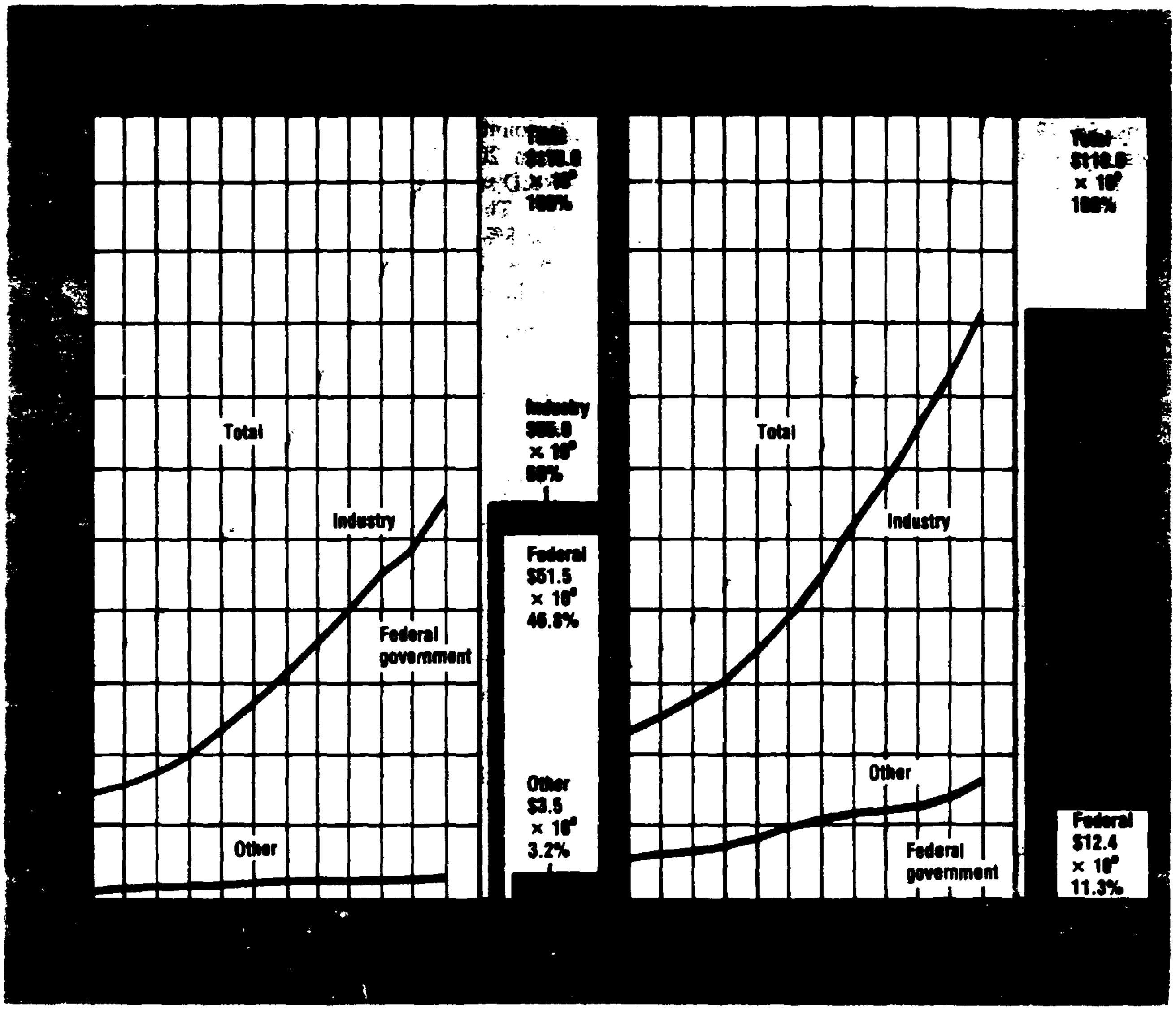
That percentage comes from "National patterns of science and technology resources 1984," NSF 84-311, the latest overall data on R&D funding from the National Science Foundation. While distributed last fall, its foreword is dated February 1984. According to this document, total R&D funds for 1984 were estimated at $96.975 billion, with the Federal government providing $44.270 billion, industry $49.375 billion, and universities and nonprofit organizations $3.330 billion.

The performance profile, or who spent these 1984 funds, is given as $10.800 billion in Federal government laboratories and R&D centers, $72.000 billion by industry in its own facilities, and $11.375 billion by universities and their associated research centers and $2.800 billion by other nonprofit institutions, giving a total of $14.175 billion.

NSF also estimated that 12% would be spent in 1984 on basic research, 22% on applied research, and 66% on development.

In our January 1984 forecast, we projected total funding for 1984 as $97.8 billion, with $50.5 billion provided by industry, $44.5 billion by the Federal government, and $2.8 billion by other sectors including academic and nonprofit organizations. Our performance projections were expenditures in industry of $73.9 billion, in Federal facilities of $10.5 billion, and in other sectors of $13.4 billion.

In addition to NSF 84-311, we also considered later data in revising our 1984 forecast to provide a basis for this 1985 forecast. We checked changes in Federal funding as monies appropriated by the Congress were obligated to specific projects and then were actually spent. We monitored changes in plans made by industry as revealed in financial reports and other documents and in conversations with executives in a number of companies. And we also monitored and checked leaders in academic and other nonprofit organizations. These procedures lead not only to the revised 1984 base but also give insights that aid our forecast.



Our revised base for 1984 gives a total of $97.0 billion for R&D funding. Industry provided $49.0 billion, the Federal government $44.7 billion, and other sectors $3.3 billion. Thus industry provided 50.5% of 1984 funds, the Federal government 46.1%, and other sectors 3.4%.

Revised performance data for 1984 are $72.0 billion for industry, $10.8 billion for Federal facilities, and $14.2 billion for other sectors. Thus industry spent 74.2% of available funds, Federal facilities 11.1%, and other sectors 14.6%.

While the revision in total funds is less than 1%, changes in the categories range from 2.5% to more than 21% in the smaller funding and performance levels for the academic and nonprofit sectors. What caused these changes from our earlier view and how we arrived at the sector levels of expenditures and performance forecast for 1985 that are shown graphically at the beginning of this article will be discussed sector by sector in the following paragraphs.

Incidentally, had we not revised our 1984 data, we would show a 12.47% increase in 1985 funding.

Industry spreads its support

By last June, NSF had received replies from 87 companies representing an estimated 53% of all R&D industrial funding in the United States. Projections based on data received were $49 billion of company funds to be spent in 1984 and $55 billion in 1985. (These data are reported in "Science resources studies highlights," NSF 84-329.)

Our discussions with executives in a somewhat smaller group of companies chosen to balance those that fund R&D cyclically with the economy against the countercyclical segment provided similar data—so close, in fact, that our industry figures round to the same as NSF's. An increase of 12.3% in funding and 12.8% in expenditure levels from 1984 to 1985 is indicated.

However, that does not mean that industry is putting more funds into its own facilities than into other sectors. The opposite is true. Late in 1983 the law was changed to remove major restrictions on cooperative R&D, allowing industry to form such new groups as the Semiconductor Research Foundation. This change also allowed nonprofit organizations such as Battelle to seek wider support for cooperative projects.

Industry also is expanding its funding of R&D in the academic area, continuing a trend from 1983.

NSF 84-329 also provides breakdowns of company funds to be spent in 1984 and 1985. For 1985, chemicals and allied products account for $9 billion, machinery (including computers) $10 billion, electrical equipment $11 billion, motor vehicles and their equipment $6 billion, aircraft and missiles $5 billion, professional and scientific instruments $5 billion, and all other segments $9 billion.

For 1984, the comparable estimates are, in billions, $8, $9, $10, $5, $4, $4, and $9. The largest increase, 17%, is in the professional and scientific instruments sector.

To summarize, we expect industry funding to rise from $49 billion in 1984 to $55 billion in 1985, with industry providing 50% of all R&D funds in 1985. Industry performance will rise from $72.0 billion to $81.2 billion so that industry will spend 73.8% of all R&D funds in 1985, down slightly from 74.2% in 1984.

Federal funding up significantly

Our forecast is that actual Federal funding for 1985 will increase 15.2% from 1984 to $51.5 billion. Performance in Federal facilities will rise 14.8% to $12.4 billion.

Such a large increase was not evident early last fall as the Congress and the Administration battled over acceptable levels for appropriations. NSF was the beneficiary of an early budget decision and appropriation with a significant increase. The National Institutes of Health benefitted from an appropriations bill that significantly increased funding, primarily because a companion piece of legislation provided for expansion of the number of NIH institutes. While President Reagan vetoed the expansion, he approved the appropriations measure, thus giving NIH more money for grants and other programs. For example, money for AIDs research was increased significantly.

But most government funding was provided by an omnibus appropriations bill at the last minute that gave the Administration much of what it had asked for in its original requests for R&D funding, plus additional amounts that the Congress tacked on. Thus a more than 20% increase in Dept. of Defense-sponsored R&D survived, for example.

Thus, the Federal government will account for $46.8% of total funding in 1985, somewhat more than the 46.1% in 1984. In performance, the Federal share of the total rises from 11.1% to 11.3%.

Universities and nonprofits gain

Funds provided by other sectors rise only 6.1%, from $3.3 billion in 1984 to $3.5 billion in 1985. However, performance in these sectors really jumps, from $14.2 billion in 1984 to $16.4 billion in 1985. That is a 15.4% increase, leading to these sectors rising to 14.9% of performance in 1985 from 14.6% in 1984 while their actual contributions fall from 3.4% to 3.2% of total funding.

As noted earlier in the industry section, transfers of funds to cooperative R&D projects are creating more activity in the academic and nonprofit sectors. When Federal funding increases are added, the effect is a significant jump in performance levels.

The overall result? No recession for R&D. It would take a significant slowdown in industrial activity coupled with a virtual elimination of R&D funding by the Federal government in its fiscal 1986 budget to make R&D funds decrease in 1985. The probability of that, in our opinion, is zero. R&D

EDITORIAL

U.S., JAPAN, AND THE REST

THE UNITED STATES and Japan are entering 1985 with courage and optimism. The other countries of the world also are entering 1985. In the U.S. and Japan, strong technology drives strong economies. In the other countries, weak technology is accompanied by faltering or even foundering economies, rampant inflation, poor exchange rates, high unemployment, and/or declining productivity. Says *The Economist* in reference to the nations of Western Europe, "[This] problem has outgrown its economic dimensions and now has political consequences. . . . few doubt that Europe is in real trouble."

To some it might seem that nations other than the U.S. and Japan are in a desperate search for a perpetual motion machine. They are trying to find an economic unit that produces more energy than is put into it. For example, the U.S. staffs its industrial firms with some 32 R&D scientists and engineers per 1,000 industrial workers, slightly above Japan's ratio. And Japan exceeds all other national ratios by 25% or more, with nearly double that of France.

The same situation applies when it comes to funding research and development. Europe's two leaders, West Germany and the UK, together spend an amount approximately equal to Japan's. With France and Italy included, the total for Europe's four big spenders on research and development is well under half of that for the United States.

R&D funding in the U.S. should increase by 13.4% during 1985 to hit an annual rate of $110 billion. Such an increase is detailed in our annual R&D forecast, elsewhere in this issue. This prediction assumes the operation of a major philosophical difference between U.S. and Japanese businessmen, on the one hand, and European planners on the other. Our projection assumes that the proportion of the gross national product that is spent for research and development in the United States will continue to increase, as it has in each of the preceding six years. In nations where this is not the case, technology inevitably lags, then the economy lags.

For the U.S., this is a notable landmark. It is the first year that R&D funding has topped $100 billion. And it continues the recent trend with industry controlling more of the funds for R&D than government does ($55 billion *vs* $51.5 billion), a fact we applauded when it first occurred several years ago.

It is good to see the strength and economic health of the U.S. and Japan, but Western Europe and the Third World countries also occupy portions of Spaceship Earth. There is no room for vast disparities of employment, of inflation, and of other important economic factors. We echo the sentiments of *The Economist* when it concluded its appraisal by saying, "The new technologies . . . are taking the drags off the wheel of human activity and letting it move as fast as human imagination can spin it. Won't Europe jump on board?"

Robert L. Jones
editor

SPIE—The Society of Photo-Optical Instrumentation Engineers
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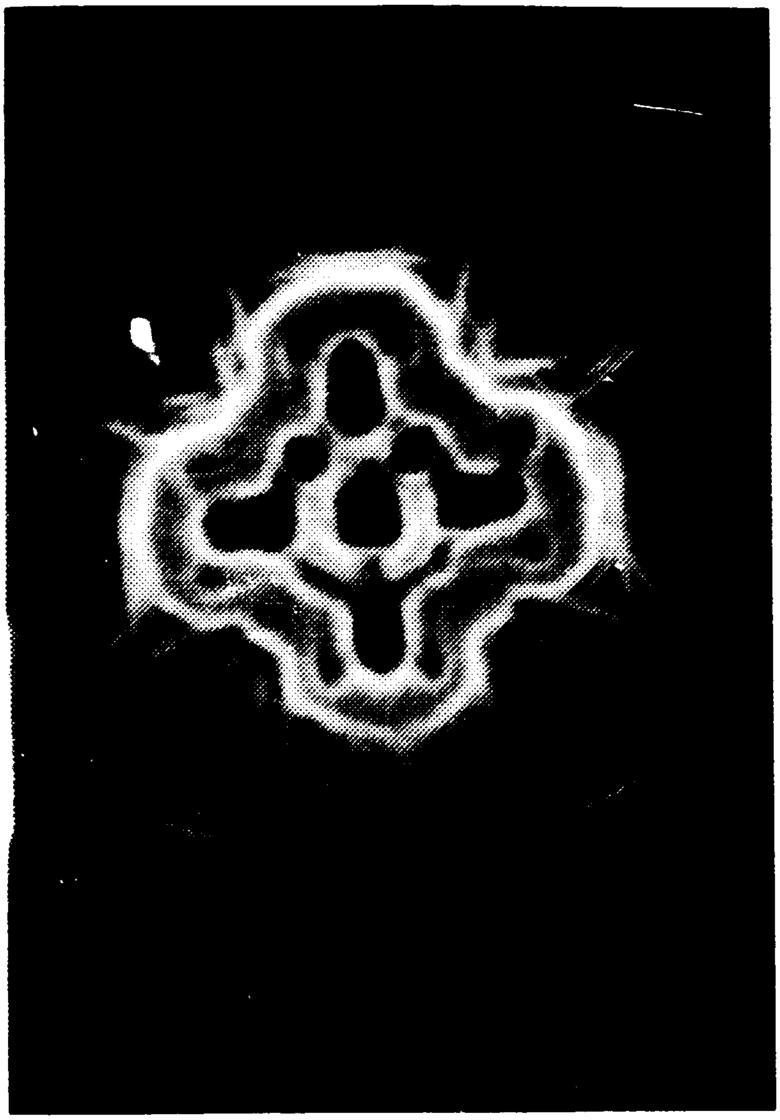
Advance Program



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COURSE DIRECTOR

Dr. Robert G. Hunsperger is Professor of Electrical Engineering at the University of Delaware. Prior to this he spent ten years in semiconductor and optical device research as a member of the technical staff of Hughes Research Laboratories in Malibu, California. He has taught at the University of Southern California and at UCLA, as well as serving as a Consultant in the fields of semiconductor and optical devices and systems. Organizations that have called upon Dr. Hunsperger's expertise in this area include Hughes Aircraft Co., Martin Marietta Laboratories, E.I. du Pont Co., and the U.S. Army (AMCCOM). He has over 70 publications and holds 14 patents. These include patents for devices fabricated in gallium arsenide by ion implantation doping, such as optical waveguides, a monolithically coupled integral waveguide/detector, a junction laser, and a microwave field effect transistor, as well as a patent on a system for optical injection locking of microwave oscillators.

Dr. Hunsperger is a member of the IEEE, AAAS, SPIE, OSA, IPA, Eta Kappa Nu, Tau Beta Pi and Phi Kappa Phi. He received the Ph.D. in Applied Physics from Cornell University, the M.S.E. from Princeton University and the B.S.E.E. from Drexel University.

ADDITIONAL FACULTY

Dr. John M. Zavada is with the Electronics Division at the Army Research Office in Durham, N.C., where he is managing an extramural research program in electro-optics devices, sensors, and materials. Previously, he was a research physicist with the Army Armament R&D Center in Dover, N.J. working on optical properties of semiconductors. He has over 30 publications in the areas of optical characterization of materials, effects of ion-implantation, and scattering of EM waves. He has taught at Drexel University and has served on national review committees for electronics research.

Dr. Zavada is a member of the APS, OSA, SPIE, and Sigma XI. He received the Ph.D. and the M.S. in physics from New York University and the B.A. from Catholic University of America.

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Course Director

R. Michael Carrell is a robot user. A Member of the Technical Staff at RCA's David Sarnoff Research Center in Princeton, New Jersey, he has consulted with the operating divisions on mechanization and robotics projects for over five years. Other projects have included computer based factory data collection systems, high performance photocomposition systems for the graphic arts industry, wideband magnetic recording systems, and intercommunication systems for use in high intensity noise. He holds a number of patents and is author or co-author of over thirty technical papers. He received the BSEE degree from Iowa State University.

Additional Faculty

Michael J. McCraley is Project Manager, Robotics, for the Panasonic Industrial Company. He was formerly Director of Marketing for Central Automation, and PUMA Product Manager at Unimation. He received his undergraduate degree in Industrial Management from Purdue University and his M.B.A. from Xavier University.

Dr. Henry Baird, a software specialist, is a Member of the Technical Staff at AT&T Bell Laboratories at Murray Hill, New Jersey. His previous work at RCA Laboratories included integration of diverse robots and vision systems. He received his Ph.D. in Computer Science from Princeton University.

Mitchell Weiss is a robot designer and co-founder of US Robots. He received the BS and MS degrees from the Massachusetts Institute of Technology where, as an undergraduate, he designed swimming and walking machines. Previous industry assignments included application engineering at Unimation and work on the Space Shuttle manipulator arm at Spar Aerospace.

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* Prices are subject to change to conform with current publisher's price. Please check appropriate box of the application form to order text.

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Course Director

Dr. Charles L. Croskey is an Instructor at Pennsylvania State University and has taught courses in solid state design, network analysis, communications, logic design, and electronics for engineers other than electronics engineers. He is also a Research Associate in the Communications and Space Sciences Laboratory.

His current engineering assignments concern the development of instrumentation for sounding rocket payloads for measurements of the lower ionosphere. He has supported field expeditions to Wallops Island, Virginia; White Sands, New Mexico; Fairbanks, Alaska; Canada; Kenya and Norway, for various coordinated research programs.

Dr. Croskey received the BSEE, MSEE and PhD degrees from the Pennsylvania State University.

Additional Faculty

Joel Balogh is Director of Instrumentation in the College of Engineering at the University of Delaware. He is responsible for the design of specialized electronic instrumentation for research laboratories at the University. Prior to this he was employed in an instrumentation group at the Pennsylvania State University and was also part of a receiving system group at HRB Singer, Inc.

Mr. Balogh received the BS in physics, MS in astronomy, and MSEE degrees from the Pennsylvania State University where he was also a part-time instructor of Solid State Electronics.

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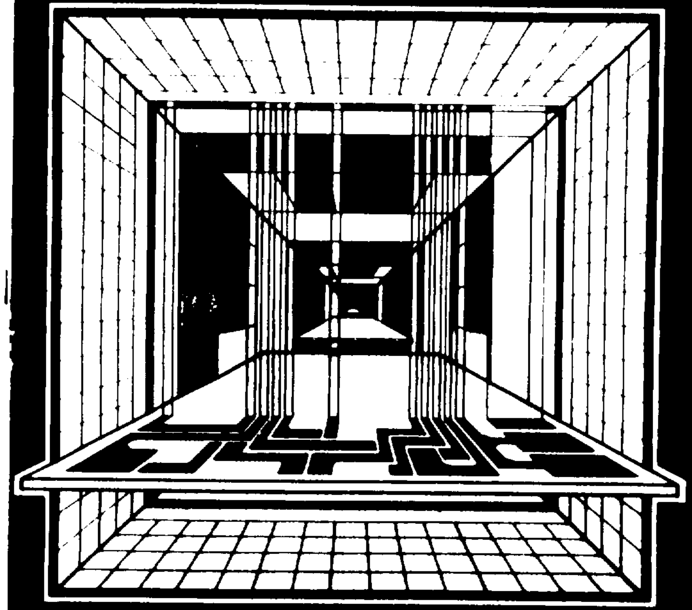

G. E. McGuire · Manager
Materials Development and Characterization Laboratory
Tektronix, Inc. · Beaverton, Oregon

Instructors

Dr. Tim J. Anderson · University of Florida
Dr. John R. Arthur, Jr. · Oregon State University
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Continuing Education Institute

Focus

The explosive growth of the semiconductor industry has resulted in the rapid evolution of materials and processing techniques that are compatible with state-of-the-art device requirements. At the same time, device geometries have decreased while device performance has increased. The practicing engineer has little time to keep abreast of the changing technology except in the areas of his immediate interest. Many professionals enter the semiconductor industry with little formal training in the process technologies and materials to which they will be exposed. This course is addressed to them and may be considered as a vehicle to acquaint them with a broad spectrum of topics in the field. This course will be taught by a carefully selected group of practicing experts in their respective fields. Since this is an overview, the subjects cannot be examined in great depth, although every attempt will be made to present current and future directions of the technology.

Course Overview

The core subjects to be covered are the basic materials and processing technologies of compound semiconductors. The primary emphasis will be devoted to III-V compound semiconductors, however, other compound semiconductor materials will be discussed. The topics that will be covered include crystal growth, wafer preparation, process induced defects, epitaxial growth techniques, implantation, dielectrics, metallization systems, device modeling, characterization techniques and solid state devices. In each of the areas the scientific background, basic technology, advantages, limitations and applications will be discussed.

Course Summary Information

Date	February 4-7, 1985
Days	Monday-Thursday
Time	8:30 a.m. to 5:00 p.m. (Thursday ½ day)
Fee	$895
Units	3.0 CEU
Number	Engr. 150.01
Hotel	Holiday Inn
City	Monterey, California

Course Materials

Participants will receive an extensive set of lecture notes.

Course Director and Instructor

Dr. Gary E. McGuire, Manager, Materials Development and Characterization Laboratory, Tektronix, Inc. His current responsibilities include the development of new display and hardcopy materials, and the introduction and application of new analytical techniques at Tektronix. Previously with Texas Instruments, he did research on surface characterization techniques investigating thin films and metallization systems used in the microelectronics industry. He is a member of the editorial board of the *Journal of Electron Spectroscopy, Scanning Electron Microscopy, Surface and Interface Analysis* and Series Editor for Noyes Publications on Semiconductor Materials. He is a Trustee of the American Vacuum Society, he serves on both the program committee of the International Conference on Metallurgical Coatings and the Publication Committee of the Electrochemical Society.

Instructors

Dr. Tim J. Anderson is an Associate Professor of Chemical Engineering at the University of Florida. His research interests include the study of solid-liquid and solid-liquid-vapor phase equilibria in multicomponent III-V semiconductor materials. His studies include investigating the heat, momentum and mass transfer and homogeneous and heterogeneous kinetic processes which occur during epitaxial processes. Dr. Anderson was previously on the staff at the Air Force [illegible] Energy Commission, Ames Lab, and served as a summer [illegible] research associate at Hanscom Air Force Base. Dr. Anderson [illegible] award [illegible]

Mail Form: Enrollment and Information

Mail to: Continuing Education Institute, 10889 Wilshire Blvd., Los Angeles, CA 90024

Application for Enrollment

☐ ***Please enroll me in the following course:***
Compound Semiconductor Materials and Process Technology
☐ **February 4-7, 1985**
Engr. 150.01
Monterey, CA
Fee: $895

☐ Check enclosed payable to: *Continuing Education Institute*
☐ Purchase order enclosed
☐ Reservation tentative pending authorization

Information Request

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Name ______ · [illegible] ______
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ELECT ENG.
UNIVERSITY OF MINNESOTA
MINNEAPOLIS MN 55455

Instructors
(Cont'd)

Dr. John R. Arthur Jr., [illegible] Engineering [illegible] the [illegible] Engineering [illegible] epitaxy [illegible] the [illegible] Dr. Arthur was the [illegible] scientist at [illegible] Physical Electronics [illegible] responsible for the [illegible] molecular beam epitaxy [illegible] molecular beam epitaxy process while at Bell Laboratories in Murray Hill, New Jersey. He began his career at the [illegible] Research at Iowa State University where he [illegible] emission from metal surfaces and heterogeneous [illegible] metals. He has held numerous offices in the American Vacuum Society including President in 1983, Chairman of the [illegible] Division and Founder and Chairman of the Electronic Materials and Processing Division. He has received numerous awards including the Morris N. Liebmann Award in 1982 from the IEEE and the American Physical Society IBM Award for New Materials in 1982.

Dr. H. C. Casey, Jr., Professor and Chairman, Department of Electrical Engineering, Duke University. His current professional interests involve the study of the optical properties of InP, the temperature dependence of the threshold current density of $Ga_xIn_{1-x}As_yP_{1-y}$-InP double heterostructure lasers, visible heterostructure lasers and bipolar heterojunction transistors. Prior to joining Duke University he was a member of the Technical Staff at Bell Telephone Laboratories in the Solid State Electronics Laboratory which he joined after a period at Hewlett Packard, Inc. Dr. Casey is a [illegible] member of the Microelectronics Center of North Carolina, member of the Executive Committee of the Electronic Materials and Processing Division of the AVS, Chairman of the 1983 IEEE Device Research Conference and member of the Electron Devices Society Administrative Committee. He has published numerous articles, book chapters, and a two-volume book *Heterostructure Lasers*. He also served as Guest Editor for the IEEE Centennial issue on *Transactions on Electron Devices*.

Dr. Gary Y. Robinson, is Professor of Electrical Engineering, Colorado State University. His current research interests include metal-semiconductor interfaces, heterojunction, ohmic contacts, molecular beam epitaxy and characterization of deep levels in III-V semiconductor devices. Before joining the faculty at Colorado State University he was Professor of Electrical Engineering and Chairman of the Microelectronics Research Group at the University of Minnesota. He has also served as a staff scientist for Hewlett Packard, Perkin Elmer and the Naval Research Laboratory. He has served on the Executive Committee of the Electronic Materials and Processing Division of the American Vacuum Society and is the Program Chairman of the [illegible] Annual Molecular Beam Epitaxy Workshop.

Dr. Ben G. Streetman, Professor of Electrical Engineering, University of Texas at Austin, [illegible] the [illegible] Centennial Chair in Engineering. His research interests include radiation damage and ion implantation, transient annealing and deep-level impurities and defects in semiconductors. Prior to joining the faculty at the University of Texas, Dr. Streetman was Professor of Electrical Engineering at the University of Illinois. He is a Fellow of the Institute of Electrical and Electronic Engineers. He serves on the Program Committee of the IEEE Device Research Conference and is a member of the Executive Committee of the Electronics Division, the Electrochemical Society. He serves on the University Advisory Committee of the Semiconductor Research Corporation and on the Advisory Committee on Solid State and Microstructures Engineering, National Science Foundation. He is author of numerous articles and the book *Solid State Electronic Devices*. In 1981 he received the Frederick Emmons Terman Award of the American Society for Engineering Education for outstanding contributions to engineering education.

Daily Schedule

Monday, February 4
I. Overview. Bulk and Epitaxial Crystal Growth

Introduction and Overview *(McGuire)*
An overview of the topics to be covered and their interrelationships and common concepts.

Bulk Crystal Growth and Wafer Preparation *(Anderson)*
An introduction to crystal growth techniques: thermodynamics, heat and mass transfer, impurity incorporation, slicing, etching and polishing. The critical crystallographic, mechanical, and electrical properties will be discussed.

Liquid and Vapor Phase Epitaxial Growth *(Anderson)*
The practical and fundamental aspects of epitaxial growth of compound semiconductors via liquid phase epitaxy and chemical vapor deposition will be discussed. Included in the discussion is an overview of equipment design and capabilities, thermodynamics and kinetic effects.

Molecular Beam Epitaxy Basics *(Arthur)*
The basic aspects of molecular beam epitaxy will be discussed including the preparation and characterization of the substrate and starting conditions of the effusion cells.

Molecular Beam Epitaxy Capabilities *(Arthur)*
An overview of MBE capabilities will be given including surface reaction kinetics, molecular beam interactions with surfaces and thin film growth of compound semiconductors.

Tuesday, February 5
II. Doping Techniques. Dielectrics. Recrystallization. Metallization Systems

Doping Techniques *(Streetman)*
The basic concepts of diffusion and ion implantation processes for introducing a dopant into the semiconducting substrate will be reviewed.

Dielectrics and Recrystallization *(Streetman)*
The methods of dealing with radiation damage and recrystallization and the selection and deposition techniques for dielectric films will be presented.

Metallization Systems *(Robinson)*
The basic requirements of Ohmic and Schottky barrier metallization systems will be presented. Processing requirements and degradation mechanisms of both single and multilevel metallization systems will be reviewed.

Wednesday, February 6
III. Device Modeling. Integrated Optics

Device Modeling *(Robinson)*
The methods of device modeling and system configuration will be described. Relevant device performance, material requirements and process parameters will be reviewed.

Integrated Optics *(Casey)*
Heterostructural materials and material systems for optoelectronic devices will be described. The optical and physical properties of GaAs, $Al_xGa_{1-x}As$, $Ga_xIn_{1-x}As_yP_{1-y}$, InP and selected wide bandgap heterojunctions will be discussed.

Thursday, February 7
IV. Materials Characterization

Materials Characterization *(McGuire)*
The techniques for characterizing the electrical, mechanical, structural and elemental composition of thin film structures and the semiconducting substrate will be discussed. Both trace elemental analysis and bulk characterization techniques will be described.

General Information

Continuing Education Institute
[illegible] development in engineering and applied science [illegible] in the areas of technology that are [illegible] rapid change. These dynamic educational programs are [illegible] by CEI and outstanding experts in their related fields. These experts have demonstrated a working knowledge and expertise of the subject matter and an ability to present the material in a clear manner to a professional audience. The Continuing Education Institute is helping to shape the world of tomorrow by providing short courses which challenge the mind today.

New Course Development
For information regarding New Program Development, contact:

Dr. Jon R. Mancé
Executive Director
10889 Wilshire Blvd.
Los Angeles, CA 90024
(213) 824-9545

Dr. Birgit Jacobson
European Director
Roerstorpsvaegen 5
S-61200 Finspong, Sweden
46 (0122) 175 70

On-Site Programs
For information about on-site programs, hybrid programs, and custom programs contact Helen Hegnsdal, Associate Director, On-Site Programs at (213) 824-9545.

Hotel/Setting
Monterey, California
The West Coast offering of this course will be held at the Holiday Inn Monterey located on the beach just minutes from Carmel, Cannery Row, the Naval Postgraduate School and the Monterey Peninsula Airport. For hotel reservations, please call (408) 394-3321 and request the Continuing Education Institute's group rate at least three weeks prior to the beginning of the course. The hotel address is 2600 Sand Dunes Drive, Monterey, CA 93940.

Course Fee
The course fee includes tuition, course materials, and refreshments. Faculty, student, and group discounts are available. Checks and purchase orders should be made payable to the Continuing Education Institute and are due one week prior to the course. Refund of fee (less 10% processing charge) is granted if cancellation is received before the first day of the course. The Course Director and CEI reserve the right to cancel, reschedule or change instructors.

Registration/Information Requests
You may register by calling any of the following Registration Centers or by mailing the registration form on the back panel of this brochure. Do not mail a registration form if you register by phone. A confirmation letter will be mailed to each registrant. You may also use the registration form for requesting other information, i.e., brochures, on-site course proposals, etc.

	TELEPHONE	TELEX
Los Angeles	(213) 824-9545	704789 CEI LA
Washington, DC	(301) 596-0111	886776 CEI DC
Finspong, Sweden	46 (0122) 175 70	64471 CEI EUR

Films and Coatings for Technology

April 8-12 198[illegible]
Los Angeles, California

An Annual International Short Course

Technologies		General Topics: Plasmas in Deposition Processes	Structure and Properties	Analytical Techniques	Cleaning and Adhesion
Physical Vapor Deposition (PVD) Processes	*Evaporation*	●	●	●	●
	Sputtering	●	●	●	●
	Ion Plating	●	●	●	●
Chemical Vapor Deposition (CVD) Processes	*CVD*		●	●	●
	Plasma Assisted CVD	●	●	●	●
Electrodeposition			●	●	●
Plasma Spraying and Detonation Gun Coatings		●	●	●	●
Polymeric Coating Processes		●	●	●	●

Applications Optical/Microelectronics/Mechanical/
Chemical Corrosion/High Temperature Corrosion/Decorative

Rointan F. Bunshah

Rointan Bunshah
Jan-Otto Carlsson
John Fish
Birgit Jacobson
Donald W. Mattox
Gary McGuire
Morton Schwartz
John Thornton
Robert Tucker

Continuing Education Institute

Films and Coatings for Technology

Intent

Films and coatings are applied in a very broad spectrum of applications, which can be subdivided into five generic areas

- *optically functional*
- *mechanically functional*
- *electronically functional*
- *chemically functional*
- *decorative*

Knowledge of the underlying sciences, developments in technology and applications are growing at an exponential rate. Engineers, scientists and managers working in most areas of high technology have to deal with coated materials. This course is addressed to them and may be considered as a vehicle to acquaint them with the wide spectrum of coating technologies and their applications. Such knowledge is essential in arriving at the correct decisions on technical and economic grounds. This course will be taught by a carefully selected group of practicing experts in their fields. Since this is an overview, the subjects cannot be examined in great depth although every attempt will be made to present the material at the cutting edge of technology. This is also not a conference where the latest research and development material is presented exclusively. General discussion sessions are scheduled each day.

This will be the 11th offering of this course, which was offered for the first time in 1978, under the coordination of Dr. Rointan Bunshah of UCLA. This course has been offered in Los Angeles, California; Soderkoping, Sweden; Davos, Switzerland; and Zandvoort, Holland.

Course Content

As the cover shows, the **core subjects** to be covered are the basic technologies for the deposition of films and coatings. These are the Physical Vapor Deposition (PVD) Processes consisting of Evaporation, Sputtering and Ion Plating; Chemical Vapor Deposition (CVD) and Plasma Assisted Chemical Vapor Deposition (PACVD); Electrodeposition and Electroless Plating; Thermal Spraying, Plasma Spraying and Detonation Gun Technologies; and Polymeric film deposition technologies. In each of these, the scientific background, basic technology, advantages, limitations, structural/property relationships and applications are discussed. Supportive to this basic theme are lectures on subjects of common interest to several technologies. These are: Adhesion of Coatings, Surface Preparation, Role of Plasmas in Deposition Processes, Structure of PVD Deposits, Microstructure of Films as Revealed by TEM and SEM Techniques, Mechanical and Tribological Properties of PVD Deposits, Elemental and structural characterization techniques, and Non Elemental coating characterization techniques. Examples of applications will be covered by the various lecturers throughout the course. Two major areas of applications — Electronic Materials and High Temperature Coatings — are treated in separate CEI short courses.

New Feature

A book *Deposition Technologies for Films and Coatings*, Noyes Publications, coauthored by the present lecturers will be provided to each attendee in addition to supplementary notes.

Biographies

Course Director **Rointan F. Bunshah D.Sc.**, Professor, Materials Department, School of Engineering and Applied Science, UCLA. His activities include materials synthesis, vacuum metallurgy, structure/property relationships, biomaterials, nuclear reactor materials, space processing of materials. Dr. Bunshah is internationally known as an expert in vacuum metallurgy and materials synthesis. He has been a pioneer in physical vapor deposition, especially in evaporation technology for metals, alloys and refractory compounds. He has carried out and published much of the basic structure/property relationship work for such coatings. He developed and chaired the International Conference on Metallurgical Coatings, which has become an annual event for the past seven years. Dr. Bunshah has been developing short course in metallurgy since 1957. He was the co-founder and first chairman of the Vacuum Metallurgy Division of the American Vacuum Society and in 1971 the President of AVS. He is the editor of ***Techniques in Metals Research***, a 17 volume reference set. He is on the Editorial Board of Thin Solid Films, Series Coordinator for Materials and Processes Short Course Series, and member of the Academic Advisory Council for the Continuing Education Institute.

Instructors:

Jan-Otto Carlsson, Ph.D., Docent, Uppsala University, Department of Chemistry, Solid State Chemistry Group. He carries out and conducts research on chemical vapor deposition (CVD). Some areas of emphasis are design of CVD experiments, nucleation, kinetics, modelling and factors influencing the morphology, adhesion and properties of CVD materials.

John G. Fish, Ph.D., Member of the Technical Staff, Central Research Laboratories, and Corporate Manager of University Ph.D. Recruiting, Texas Instruments, Inc., Dallas, Texas. His responsibilities have included consultation and laboratory evaluation of all aspects of polymer technology as used in the electronics industry. He has worked on many coating technologies for microelectronics, printed circuit boards and adhesives, as well as decorative and protective applications for equipment.

Birgit E. Jacobson, Ph.D., Assistant Professor at the Department of Physics and Measurement Technology, Linkoping University, Sweden. She has been involved in research in coating technology since 1976 until recently at Stanford University and at present at Linkoping University. This research is focused on the relationship between processing parameters and the microstructure of deposited films and how these features can be varied and optimized in order to improve film properties.

Donald M. Mattox, M.S., Supervisor of Surface Metallurgy Division of Sandia National Laboratories, a Department of Energy Laboratory, Albuquerque, New Mexico. He has been active in surface science and thin film technology for many years and has published extensively in these areas. At present his activities are in the area of coatings for erosion and wear resistance, solar absorbing coatings, and coatings for use in Controlled Thermonuclear Reactors (TOKAMAKS). He obtained the basic patent on the Ion Plating Process in 1966, is the past chairman of the Thin Film Division of the AVS (American Vacuum Society), the Vice Chairman of the Fusion Technology Division and a member of the Editorial Board of the **Journal of Vacuum Science and Technology.** He is the United States representative to the Thin Applications) and is a member of the Executive Council of that group.

G.E. McGuire, Ph.D., Manager, Analytical Chemistry Laboratory, Tektronix Inc., Beaverton, Oregon. Dr. McGuire is currently responsible for the introduction and application of new analytical techniques into Tektronix Research Center. Previously with Texas Instruments, he did research on surface characterization techniques investigating thin films and metallization systems used in the microelectronics industry. He is a widely recognized expert in auger and photoelectron spectroscopy and is a member of the editorial board of the ***Journal of Electron Spectroscopy and Related Phenomena***.

Morton Schwartz, M.A., Electrochemical/Metal Finishing Consultant, Los Angeles, California. He has been actively engaged in electrodeposition in production, research and development for 38 years. His researches include alloy deposition, electroless deposition, precious metals plating for electronics, and magnetic characteristics of plated coatings for computers.

Daily Schedule

Each day will end with a 1-hour discussion period to enhance instructor/participant interaction.

Monday — I. Overview. Characterization and Cleaning Techniques

9:00-9:45
Introduction and Overview
(Bunshah)

An overview of the topics to be covered and their interrelationships, common concepts and definitions, classification of coating techniques and economic factors.

9:45-10:45
Plasmas in Deposition Processes
(Thornton)

Several deposition processes include the use of plasmas. This talk will introduce the concept of plasmas and methods of generation.

11:00-12:30
Surface Preparation
(Mattox)

This lecture will discuss the factors which govern adhesion of coating to the substrate, contamination on surfaces, cleaning of surfaces.

1:30-3:30
Analytical Techniques
(McGuire)

Elemental and Structural Characterization Techniques (including Surface Analytical Techniques, Principles of Microprobe, SEM, TEM, STEM etc.)

The techniques for elemental analysis on the surface particularly as it applies to films will be discussed. Depth profiling and thin film characterization will be reviewed. The principalities of analytical microscopy using the Microprobe, SEM, TEM, STEM will be discussed.

3:50-5:50
Non-elemental Coating Characterization Techniques
(Mattox)

Techniques for the characterization of coatings such as hardness tests, adhesion tests, thickness measurements, pinhole density measurements, etc. will be discussed.

[illegible]
General Discussion

Tuesday — II. Physical Vapor Deposition (PVD) Processes–Evaporation. Sputtering. Ion Plating

8:30-9:00
Introduction to PVD Processes
(Bunshah)

The range of PVD processes, their advantages and limitations, and the process steps common to all PVD processes will be presented.

9:00-10:30
Generation and Transport of Vapor
1. Evaporation/Deposition Process
(Bunshah)

This lecture will present the technology of the various evaporation processes, the deposition of metals, alloys, intermetallic and refractory compounds, applications.

[illegible]
3. Sputter Deposition Process
(Thornton)

[illegible]

Ion Plating Process
(Mattox)

[illegible]

Film Growth and Structure of PVD Deposits
(Thornton)

[illegible]

General Discussion

Wednesday — II. PVD Process (Continued)

8:30-10:30
Microstructure of PVD Coatings by TEM and SEM Techniques
(Jacobson)

The microstructure features as revealed by the Transmission Electron Microscope and Scanning Electron Microscope (SEM) for PVD, CVD, and electro-deposited films will be presented. Correlations of structure and properties will be explored.

10:50-12:30
Bulk Microstructures of PVD Deposits. Mechanical and Tribological Properties
(Bunshah)

The microstructure of bulk PVD deposits, mechanical properties, structure/property relationships will be presented. Wear of surfaces and the role of coatings in wear prevention for engineering surfaces and cutting tools will be discussed.

III. Chemical Processes

1:30-4:00
Chemical Vapor Deposition (CVD)
(Carlsson)

The principles, technology, materials deposited, advantages and limitation of CVD techniques will be presented. A discussion of economics and applications is included.

4:15-5:15
Plasma Assisted CVD Processes
(Thornton)

The use of plasmas in enhancing the scope of CVD processes (e.g. to lower substrate temperatures, increase rates) and applications will be discussed.

5:15-6:30
General Discussion

Thursday — Chemical Processes (continued)

8:30-10:30
Polymeric Coating Techniques
(Fish)

The basic concepts of polymer synthesis, the methodologies, coating techniques, structure and properties will be presented.

10:45-12:15
Electrodeposition and Electroless Deposition
(Schwartz)

The theory, practice, materials, advantages, limitations, structure of electrodeposited materials will be presented. A further section is devoted to electroless coating techniques.

IV. Plasma Spray and Detonation Gun Coatings and Applications

2:30-4:00
Plasma Spraying & Detention Gun Techniques
(Tucker)

The technologies of plasma spraying and detonation gun techniques will be presented. The materials to be deposited, microstructure and properties will be discussed.

4:15-5:45
Applications of Plasma Spray & D-gun Coatings.
(Tucker)

A discussion of the use of thermal spray applied coatings including D-gun and plasma spray in the solution of critical high temperature materials problems in a variety of environments [illegible] will be given. Reasons for the selection of one thermal spray deposition process over the other together with examples [illegible] coating system applications will be reviewed.

General Discussion

General Information

Continuing Education Institute

The Continuing Education Institute is a non-profit organization dedicated to providing high quality professional development in engineering and applied science. Programs offered focus on the areas of technology that are undergoing rapid change. These dynamic educational programs are developed together by CEI and outstanding experts in their related fields. These experts have demonstrated a working knowledge and expertise of the subject matter and an ability to present this material in a clear manner to a professional audience. The Continuing Education Institute is shaping the world of tomorrow by providing short courses which challenge the mind.

New Course Development

For information regarding New Program Development contact:

Dr. Tom R. Musser
Executive Director
10889 Wilshire Blvd.
Los Angeles, CA 90024
(213) 824-9545

Dr. Birgit Jacobson
European Director
Roerstorpsvägen 5
S-61200 Finspong, Sweden
46 (0122) 17570

On-Site Programs

CEI represents over 500 short course instructors covering a broad spectrum of engineering and engineering management who have courses available for offering at your facility. For information about our on-site programs, hybrid programs, and custom programs contact Helen Hegnsdal, Associate Director, On-Site Programs at (213) 824-9545.

Enrollment Information

Enrollment in this program is limited to ensure maximum group interaction. Therefore early enrollment by mail is advised. Reservations may be made by telephoning any of the Reservation Centers below. However, confirmations should be made at least one week prior to the course.

Course Fee

The course fee includes tuition, course materials and refreshments. Payment, purchase order, or letter of authorization must be received prior to the start of the course. Group discounts are available. Refund of fee (less 10% processing charge) is granted if cancellation is received before the first day of the course. Checks and purchase orders should be made payable to the Continuing Education Institute.

Registration Centers

[illegible]

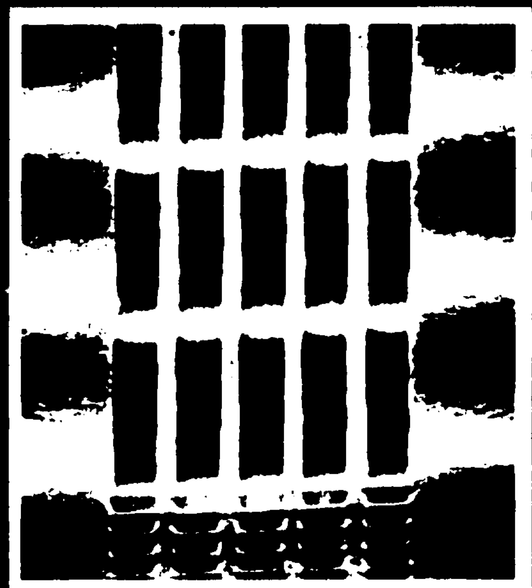
	Telephone	Telex
Los Angeles	[illegible]	704/[illegible]
[illegible]	[illegible]	86/[illegible]
Finspong, Sweden	[illegible]	644[illegible]

Microlithography

An intensive 2-day course taught by leading experts in the field.

March 7 8, 1985
Monterey California

March 28 29 1985
Cambridge Massachusetts



Dr. Fabian Pease
Professor of Electrical Engineering Stanford University

Dr. Michael C. King
G.C.A. Corporation

Dr. Alan Wilson
IBM Research Center

Dr. C. Grant Willson
IBM Research Center
Monterey, CA only

Dr. Gary N. Taylor
AT&T Bell Laboratories
Cambridge MA Only

Continuing Education Institute

Focus

Microlithography is one of the key technologies pacing the evolution of VLSI towards the ultra-high-density (sub micron) regime. By having both microlithography and plasma etching courses offered contiguously the participants can become acquainted with the complete patterning technology in one 5-day period of intense study.

Course Overview

This course will be taught by some of the leading authorities in the field from the academic community and industry. They will review the fundamentals of the physics and chemistry of photoresist and electron beam resist, and the physics and engineering of optical mask aligners including scanning projection ("Micralign®") aligners and wafer steppers. Electron beam lithography, both for mask making and direct write and x ray lithography will also be described.

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Course Summary Information

Date	March 7 8, 1985	March 28 29, 1985
Days	Thursday Friday	Thursday Friday
Time	See daily schedule	See daily schedule
Fee	$750	$750
Units	1.4 CEU	1.4 CEU
Number	Engr. 103.01	Engr. 103.02
Hotel	Holiday Inn	Sheraton Commander
City	Monterey CA	Cambridge MA

Academic Course Information

Questions on course content should be directed to the Course Director, Dr. R. Fabian Pease, McCullough 204, Stanford University 94305, telephone (415) 497-0959.

Mail Form: Enrollment and Information

Mail to: Continuing Education Institute, 10889 Wilshire Blvd. Los Angeles CA 90024

Application for Enrollment

☐ *Please enroll me in the following course:*

Microlithography

☐ **March 7-8, 1985**
Engr. 103.01
Monterey, CA
Fee: $750

☐ **March 28-29, 1985**
Engr. 103.02
Cambridge, MA
Fee: $750

☐ Check enclosed payable to: *Continuing Education Institute*
☐ Purchase order enclosed
☐ Reservation tentative pending authorization

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Specify Course ____________

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Title ____________
Company Name ____________
Company Address ____________
City State Zip ____________

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Daytime Phone Number ____________ ext.
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MICROELECTRONICS
ELECT ENG.
UNIVERSITY OF MINNESOTA
MINNEAPOLIS MN 55455

Course Director and Instructor

R. Fabian Pease, Ph.D., [illegible] ... at Bell Laboratories, Murray Hill, New Jersey ... [illegible] ... at Berkeley ... Electrical Engineering and in Natural Sciences at Cambridge University where his Doctoral research ... [illegible] ... high resolution ... [illegible]

Instructors

C. Grant Willson, Ph.D., [illegible] ... IBM Research Lab, San Jose, CA ... [illegible] ... IBM, Dr. Willson ... [illegible] ... He received his B.S. and Ph.D. degrees from the University of California at Berkeley and his M.S. degree from San Diego State University. Dr. Willson will lecture at the Monterey, CA offering of this course only.

Alan Wilson, Ph.D., [illegible] ... at the IBM Watson Research Center, Yorktown Heights, New York. His areas of responsibility ... [illegible] ... synchrotron radiation from the Brookhaven ... [illegible]

Michael C. King, Ph.D., [illegible] ... degrees in mathematics and M.S. and Ph.D. degrees in physics ... Carnegie Mellon University. In 19.. he joined Bell Laboratories, Murray Hill, New Jersey ... [illegible] ... joined Perkin-Elmer Corporation where he was ... Program Manager ... Micralign Instrument Model ... [illegible] ... of the Microlithography Division ... [illegible] ... papers and several patents in the field of optics and photolithography including a book chapter on the principles of optical lithography.

Gary N. Taylor, Ph.D., is presently supervisor of the Organic Materials for Device Fabrication Group at AT&T Bell Laboratories. He received a B.A. from Princeton University, M.S. and Ph.D. degrees from Yale University ... [illegible] ... Bell Laboratories in 19... His interests include materials and processes for microlithography, plasma ... [illegible] ... polymer and organic chemistry, and organic materials for electronic and ... [illegible] ... Dr. Taylor will lecture at the Cambridge, MA offering of this course only.

Daily Schedule

Thursday, March 7/March 28

9:00 12:00 a.m.

- Fundamentals of the lithography process
- Factors affecting sensitivity and contrast of positive and negative resists
- Basic limits to resolution of ultraviolet, electron beams, and x-ray lithography
- Fundamental tradeoffs between resolution and sensitivity in the exposure process
- Modelling of the exposure and development processes

1:30 4:30 p.m.

- Resist materials
- Negative acting polymeric resists
- Modern, high contrast, high resolution, positive photoresist materials including the choice of materials for the base resin, the photoactive compounds, and the solvent system and the developing solutions
- New materials and structures such as contrast enhancing layers and multiple level resists
- Electron beam and x-ray resist

Friday, March 8/March 29

8:30 11:30 a.m.

- Optical mask aligners
- Achieving resolution and overlay in whole wafer exposure systems such as the Perkin-Elmer Micralign® series
- Factors affecting resolution, field of view and overlay accuracy in wafer steppers
- The relative advantages of the different approaches including the 1:1 steppers

1:00 4:00 p.m.

- Electron beam and x-ray lithography
- Limits to speed, resolution and pattern placement accuracy in scanning electron beam lithography
- Description of present-day (first generation) systems and of second generation systems incorporating the variable shape concept
- Expansion x-ray lithography include both conventional and exotic (e.g., synchrotron storage ring) sources, alignment strategies and mask making techniques

Other Upcoming Short Courses

Compound Semiconductor Materials and Process Technology Monterey, CA February 4-7, 1985	G. McGuire
Plasma Etching Monterey, CA March 4-6, 1985 • Cambridge, MA March 25-27, 1985 *This course immediately precedes both courses on Microlithography and will be offered at the Holiday Inn in Monterey, CA and at the Sonesta Hotel in Cambridge, MA*	S. Broydo
Thin Films and Coatings Los Angeles, CA April 9-12, 1985	R. Bunshah
Semiconductor Silicon Technology Austin, TX April 22, 1985 • Monterey, CA April 29, 1985 Falls Church, VA May 6, 1985 • Boston, MA May 10, 1985	W. O'Mara

To obtain information on any of the above listed courses or on custom designed on-site courses, please call (213) 824-9545 or return the form on the back panel of this brochure.

General Information

Continuing Education Institute

The Continuing Education Institute is ... [illegible] ... organization dedicated to ... professional ... in engineering and applied science ... [illegible] ... areas of technology that are undergoing rapid change. These dynamic educational programs are ... [illegible] ... outstanding experts in the related fields. These experts have demonstrated a working knowledge and experience of the subject matter and an ability to present the material in a clear manner to a professional audience. The Continuing Education Institute is helping to shape the world of tomorrow by providing short courses which challenge the mind today.

New Course Development

For information regarding New Program Development, contact:

Dr. Ivan R. Mincer	Dr. Birgit Jacobson
Executive Director	European Director
10889 Wilshire Blvd.	Roerstorpsvaegen 5
Los Angeles, CA 90024	S-61200 Finspong, Sweden
(213) 824-9545	46 (0122) 175 70

On-Site Programs

For information about on-site programs, hybrid programs, and custom programs contact Helen Hegnsdal, Associate Director, On-Site Programs at (213) 824-9545.

Hotel/Setting

Monterey, California
The West Coast offering of this course will be held at the Holiday Inn Monterey located on the beach just minutes from Carmel, Cannery Row, the Naval Postgraduate School and the Monterey Peninsula Airport. For hotel reservations, please call (408) 394-3321 and request the Continuing Education Institute's group rate at least three weeks prior to the beginning of the course. The hotel address is 2600 Sand Dunes Drive, Monterey, CA 93940.

Cambridge, Massachusetts
The East Coast offering will be held at the Sheraton Commander Hotel located near exciting Harvard Square and minutes from Concord and Lexington, Peabody Museum, Harvard University, MIT, and Research Road. For hotel reservations, please call (617) 547-4800 and request the Continuing Education Institute's special group rate at least three weeks prior to the beginning of the course. The hotel address is 16 Garden Street, Cambridge, MA.

Course Fee

The course fee includes tuition, course materials, and refreshments. Faculty, student, and group discounts are available. Checks and purchase orders should be made payable to the Continuing Education Institute and are due one week prior to the course. Refund of fee (less 10% processing charge) is granted if cancellation is received before the first day of the course. The Course Director and CEI reserve the right to cancel/reschedule or change instructors.

Registration/Information Requests

You may register by calling any of the following Registration Centers or by mailing the registration form on the back panel of this brochure. Do not mail a registration form if you register by phone. A confirmation letter will be mailed to each registrant. You may also use the registration form for requesting other information, i.e., brochures, on-site course proposals, etc.

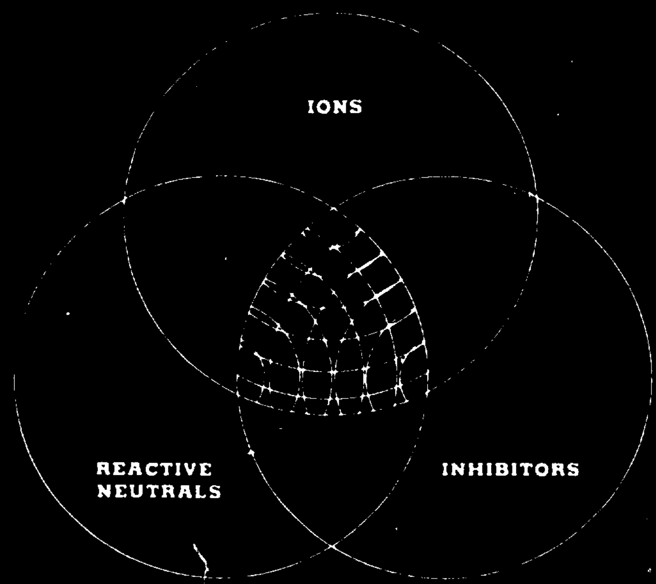
	TELEPHONE	TELEX
Los Angeles	(213) 824-9545	704789 CEI LA
Washington, DC	(301) 596-0111	898776 CEI DC
Finspong, Sweden	46 (0122) 17570	64471 CEI EUR

Plasma Etching

A Unique Three Day Course taught by some of the leading experts in the field.

March 4-6, 1985
Monterey, California

March 25-27, 1985
Cambridge, Massachusetts



Course Director
Dr. Samuel Broydo

Instructors
Dr. Richard Bruce
Dr. Brian Chapman
Dr. Daniel Flamm
Dr. Ken Herb
Dr. Thomas Mayer
Dr. Eric Sirkin
Dr. David Wang

Continuing Education Institute

Plasma Etching

Focus

Plasma etching is one of the key elements of the modern integrated circuit manufacturing technology. It is used to shape fine features in material layers forming the devices and requires sophisticated and expensive equipment. Integrated circuits using precisely defined 2 micron lines and spaces are already in production, and even smaller features need to be defined in advanced circuits presently in development. The use of plasma etching is rapidly expanding and so is the need to judge the ability of a specific plasma etching process within a given machine to satisfy the requirements of the integrated circuit fabrication.

Course Overview

Academic Course Information

Course Summary Information

Date		
Days		
No.		
Fee		
Time		
Units		
Hotel		
City		Cambridge, MA

Biographies

Course Director and Instructor

Samuel Broydo, Ph.D.

Mail Form: Enrollment and Information

Continuing Education Institute

Application for Enrollment

☐ *Please enroll me in the following course.*

PLASMA ETCHING

☐ March 4-6, 1985, Engr. 196.27, $850, Monterey, CA
☐ March 25-27, 1985, Engr. 196.28, $850, Cambridge, MA

☐ Check enclosed payable to *Continuing Education Institute*
☐ Purchase order enclosed

Information Request

Add Me to CEI Mailing List

Brochure Request

New Course Request

In-Plant Course Information Request

Continuing Education Institute

PL869

S GILBERT MGR
MICROELECTRONICS
ELECT ENG.
UNIVERSITY OF MINNESOTA
MINNEAPOLIS MN 55455

Instructors

Richard H. Bruce, Ph.D. Manager, VLSI Technology at Xerox Palo Alto Research Center, Palo Alto, California. Prior to joining Xerox he was with Perkin Elmer Co. where he was involved in research and development of plasma etching processes. He received Ph.D. degree in Solid State Physics from the University of California at Santa Barbara in 1975 and studied optical properties of materials at the City College, City University of New York.

Daniel L. Flamm, Sc.D. Member of Technical Staff at AT&T Bell Laboratories, Murray Hill, New Jersey. He is doing work in chemistry and engineering of electrical discharge processes, electronic material processing, automation and computer systems. He holds a B.S. degree in Mathematics and M.S. and Sc.D. degrees in Chemical Engineering from the Massachusetts Institute of Technology. Early in his career he designed process control software at the Foxboro Company and later joined the chemical engineering faculty at Texas A&M University. He has published more than 50 papers in [illegible] chemistry [illegible] air pollution and general chemical engineering.

G. Kenneth Herb, PhD. [illegible] Member of Technical Staff at AT&T Bell Laboratories, Allentown, Pennsylvania. For the past ten years he has been developing plasma technology [illegible] VLSI integrated circuits. Prior [illegible] development in phosphor and display technology, VLSI metallization and reliability failure mode analysis. He received Ph.D. in Solid State Physics from Lehigh University in 19[illegible].

Thomas M. Mayer, Ph.D. [illegible] at the University of North Carolina [illegible] at Bell Laboratories [illegible] VLSI [illegible] chemical film deposition.

Eric R. Sirkin, Ph.D. Project Leader, Technology Development at Zetron Corporation, Sunnyvale, CA. From 1980 to 198[illegible] he was a Member of Research Staff at Xerox Palo Alto Research Center, Palo Alto, California where he was engaged in research related to fundamental aspects of plasma etching and in plasma process development. He received his Ph.D. in chemistry in 1980 from U.C. Berkeley where he specialized in chemical lasers, spectroscopy, gas phase reaction dynamics and fast electrical discharges. He spent two years at the Hebrew University of Jerusalem where he studied multiphoton ionization of gases.

David N.K. Wang, Ph.D. Director, Materials [illegible] Applications for the [illegible] Technology [illegible] Division of Applied Materials Inc., Santa Clara, California. Prior to joining Applied Materials he was a Member of Technical Staff at Bell Laboratories, Murray Hill, New Jersey where he [illegible] Ph.D. in Materials Science from U.C. Berkeley in 197[illegible] [illegible] laboratory.

Academic Course Information

Questions on course content should be directed to the Course Director, Dr. Samuel Broydo (408) 730-8800.

Daily Schedule

Tuesday, October 2/October 23

9:00–12:00 a.m.
An Overview
(Broydo)

Important aspects of plasma physics and chemistry affecting the parameters characterizing plasma etching processes (e.g. anisotropy, uniformity and reproducibility) are examined. The correlation between these parameters and features of the etching equipment are established.

1:30–4:30 a.m.
Plasma Safety Issues
(Herb)

All equipment, material and safety aspects relevant to the handling of hazardous gases in plasma etching are discussed. Specific examples of plasma safety issues will be presented.

Wednesday, October 3/October 24

9:00–10:30 a.m.
Surface Chemistry and Physics
(Mayer)

Fundamental interactions of ions and neutral gases with surfaces in etching processes are examined. Ion beam experiments designed to simulate plasma conditions but allowing greater control and better analysis are described. The [illegible] bombardment [illegible] Ion beam [illegible] examined.

10:30–12:00 a.m.
Plasma Spectroscopy and End Point Detection
(Sirkin)

Different approaches to the analysis and the end point detection [illegible] processes, including optical [illegible] are discussed. The fundamental [illegible] techniques [illegible].

1:30–6:00 p.m.
Plasma Chemistry and Physics
(Flamm)

The chemistry of plasma etching and the physics of the [illegible] experimental data [illegible].

Thursday, October 4/October 25

9:00–12:00 a.m.
Etching in Low Pressure Plasmas
(Wang)

[illegible] low pressure plasmas is reviewed. All [illegible] etching processes [illegible] are discussed in detail.

1:30–4:30 p.m.
Etching in High Pressure Plasmas
(Bruce)

[illegible] the primary integrated circuit materials in high pressure [illegible] are discussed in detail. Models of the physics and chemistry of these processes are presented to assist in the refinement and future development of processes.

Other Upcoming Short Courses

Modern Microwave Measurements: Signal & Network Analysis	C. Adam	Boulder, CO Boston, MA Los Angeles, CA	Aug. 27–30, 84 Sep. 17–20, 84 Dec. 3–6, 84
Peripheral Array Processors	W. Karplus D. Cohen	Boston, MA San Diego, CA	Oct. 8–10, 84 Dec. 10–13, 84
Microwave Circuit Design: Linear Circuits	L. Besser	Palo Alto, CA	Nov. 5–9, 84
Microwave Circuit Design: Nonlinear Circuits	L. Besser	Palo Alto, CA Boston, MA	Nov. 26–30, 84 Dec. 3–7, 84

For brochures on these courses, call the CEI Program Office or return the form on back panel

General Information

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(213) 824-9545	46 (0122) 17570

In-Plant Programs

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Hotel/Setting

Palo Alto, California
The Continuing Education Institute has selected the Hyatt Palo Alto Hotel for the site of this course. Located near "Silicon Valley" and Stanford University, this hotel provides a convenient location for many working in this field of specialization as well as a place for those from outside the area to combine business and education. It is located mid-way between San Francisco and San Jose with regularly scheduled transportation to both airports for those participants arriving from outside the area. The hotel is set among magnolia trees and manicured lawns, with exercise facilities including swimming and nearby tennis and golf. For hotel reservations call (415) 493-0800 and request the Continuing Education Institute's preferred group rate at least 3 weeks prior to the beginning of the program. The hotel address is 4290 El Camino Real, Palo Alto, California 94306.

Arlington, Virginia
This course will be held at the Twin Bridges Marriott located on the Virginia side of the Potomac River, just minutes from National Airport, Downtown Washington and the Pentagon. Hotel facilities include an indoor/outdoor pool, sauna and game room. Scheduled transportation is available. For hotel reservations, call (202) 628-4200 and request the Continuing Education Institute's group rate at least three weeks prior to the course. The hotel address is 333 Jefferson Davis Highway, Arlington, VA 22202.

Course Fee

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	Telephone	Telex
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Washington, D.C.	(301) 596-0111	
Linköping, Sweden	46 (0122) 17570	64471