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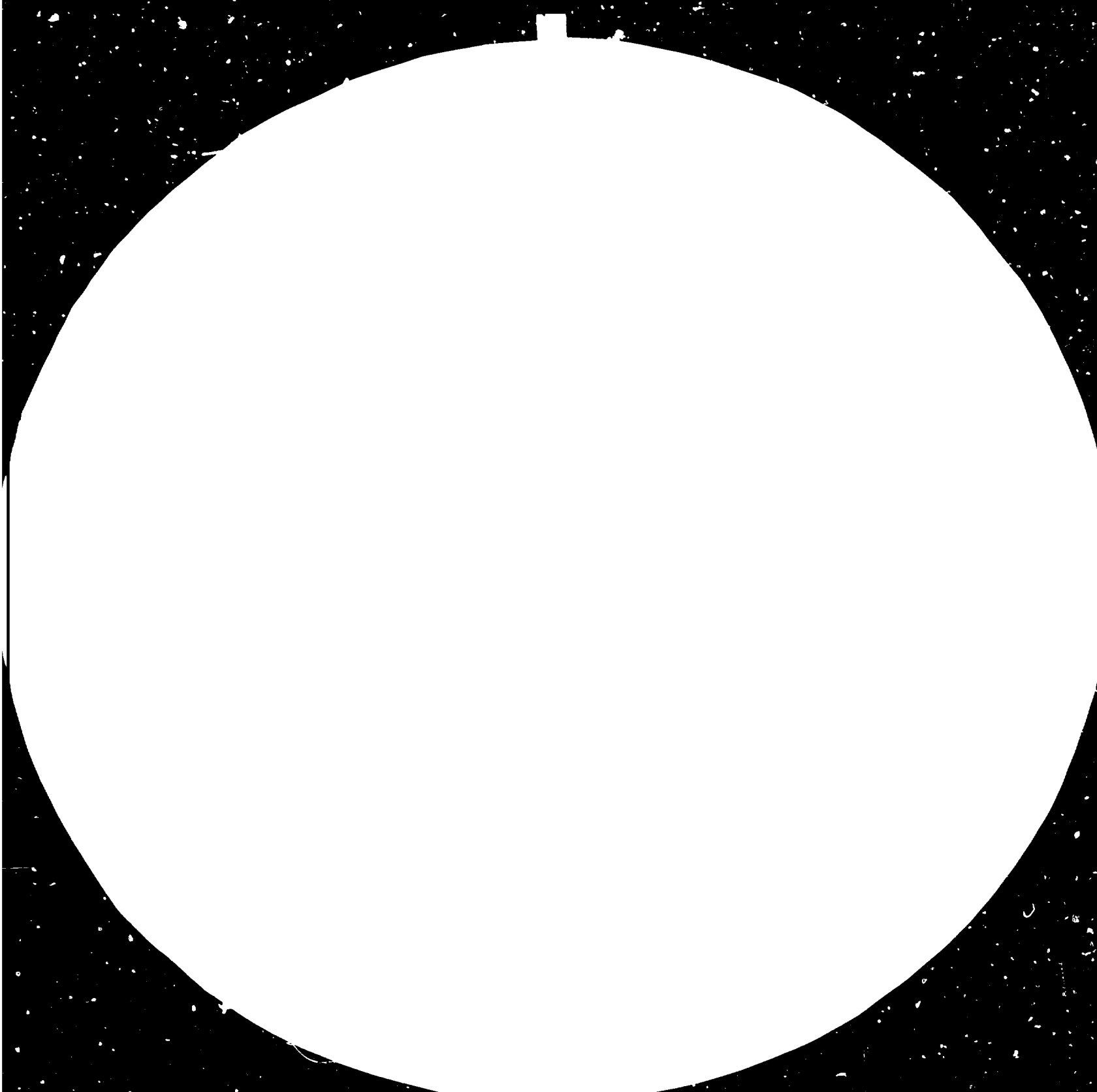

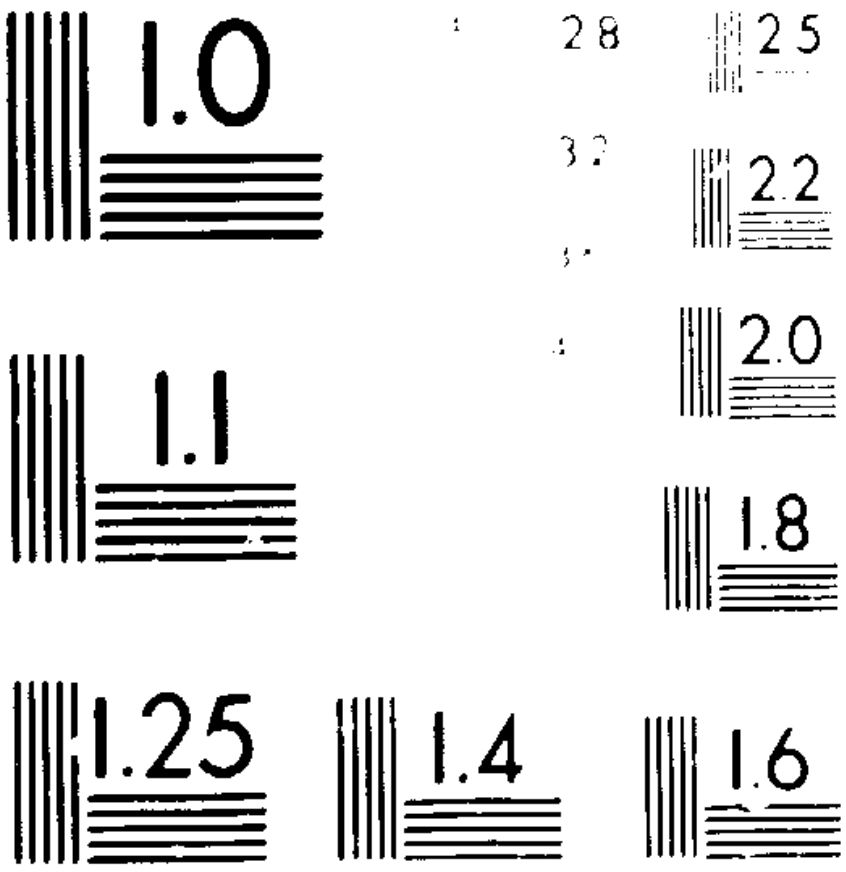

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NEW MICROELECTRONIC TECHNOLOGIES*

by

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INTRODUCTION

The evolution of micro-electronics in the past few years has been so rapid that it is often called a revolution, and rightly so. This revolution is destined to have a profound effect on all societies around the world regardless of their size or stage of development. Completely new types of products are being produced. Dramatic changes are underway in the methods of manufacture of traditional goods and the service and information handling sectors of society are changing in nature and scope. The electronics industries in the United States and Japan are clearly the major forces behind this revolution. However, many other countries are asking how they can become involved or at least what they should do to properly adapt to the changes that are occurring. By discussing the new micro-electronic technologies, I hope to provide some insight into how smaller countries might be involved and what that involvement might be.

First of all, I should make clear that I will be using the phrase "micro-electronic technologies" in a non-traditional way. Rather than meaning the techniques and materials used in the manufacture of integrated circuits such as, a three micron CMOS or five micron nMOS technology, I will be referring to the methods of design of integrated circuits.

Since its infancy in the early 1960's, there have been a number of consistent trends in the micro-electronics industry. It would be useful initially to examine some of these general trends not only to put the new micro-electronic technologies in the proper context but also to provide the background for predicting what the future holds and what opportunities exist for smaller players to take advantage of this micro-electronic revolution.

TRENDS IN MICRO-ELECTRONICS

Perhaps the most obvious trend in micro-electronics has been the rapidly increasing complexity of integrated circuits. The first experimental integrated circuit produced in the 50's contained only a few components per chip. By 1964 commercially available chips had around ten components; by 1970 that number was close to 1000; by 1976 it had risen to 30,000 and today it is close to 1,000,000. In fact, this growth has been stated in the form of a law: Moore's Law, first expressed in 1974. Based upon the short history of the industry, Moore's Law predicted that the number of components per chip would approximately double each year. And so it has. Along with the rapidly increasing complexity has come an equally rapid decrease in the cost per function for chips produced in large volumes.

These two trends have combined to make the integrated circuit suitable for a wider and wider range of applications. In the days of small and medium scale integration with fewer than about 1000 devices per chip, IC's were used mainly for fabricating the fundamental building blocks of digital computing systems such as logic gates, flip flops and so on. These types of circuits were useable in a tremendous variety of applications and were demanded in huge volumes. Thus the cost was low. However, as the complexity of chips has increased they have, in general, become more and more specialized and fewer of each are required. Thus with increasing complexity the use of IC's has become more widespread while at the same time the use of a particular type of IC has become more and more limited. Design time has increased with complexity as has the cost of documentation of the design. Therefore, the price paid for developing and producing a complex, specialized chip tends to be increasing.

There have, however, been several technological innovations which have allowed the industry, and thus the user of integrated circuits, to break out of the cycle of: greater complexity -- smaller range of applications -- higher costs.

One is the micro-processor - a complex circuit with a very wide range of applications. The fundamental reason why the micro-processor has been so successful is that its actual function is not defined until after it has been completely manufactured. The function is defined by the software and the software can be tailored to satisfy a wide range of needs. A second example is the gate array - a complex IC, the function of which is not specified until the last step in the fabrication process. A third innovation destined to have a profound effect on IC design and fabrication is the silicon foundry approach. It is these last two innovations that I want to describe in more detail.

GATE ARRAY APPROACH

The first innovation which allowed small and medium sized companies access to the benefits of integrated circuit technology was taken around 1975 with the introduction of gate arrays for the fabrication of digital logic circuits. A gate array is an integrated circuit on which has been fabricated a fixed number and distribution of standard logic gates with no inter-connections between them. The user of a gate array specifies the interconnection between the available gates required to implement the desired logic function and designs it according to a set of specifications. The basic integrated circuit is the same for all users; only the final metallization mask differs from one user to the next.

This results in a relatively low cost for medium volume production, a short design time and a reasonably high probability of successful design on the first attempt since the basic circuits have all been well tested. Gate arrays are available in a wide range of technologies including nMOS, pMOS and bipolar.

There are however, several serious drawbacks to this approach. For example, if the gate array contains 100 NAND gates and the application requires 101 an obvious problem exists. Similarly, if the application only requires 1 NAND gate, there are still 100 gates on the chip; the extra 99 take up a large amount of silicon real estate and consume power yet serve no useful purpose. Thus, gate arrays tend not to make efficient use of available area. The performance of a logic circuit is dependent upon having connections between gates as short as possible. Since the physical position of gates in the array is predetermined, performance of the circuit is often less than optimum.

In spite of these limitations the gate array approach has been proven to be quite suitable for a wide variety of applications. In the United States, there are over 35 companies offering gate array services in nMOS, CMOS, bipolar or in a few cases linear technologies. Turnaround time from design to functioning chip is in the area of 2 to 4 weeks and the cost is low for moderate volume production runs.

There are however, many situations for which gate arrays are not the answer.

SILICON FOUNDRY APPROACH

One major characteristic of the integrated circuit industry up until recently has been its vertical integration, at least to the stage of circuit production. There are many steps in the process of going from idea to integrated circuit. The initial steps of system definition, logic design, circuit design and mask design are manpower intensive and "thought intensive" and depend upon having a set of design skills which are almost independent of how the device will actualy be made. These steps also establish the eventual function of the device. On the other hand, the later steps; mask fabriction, chip fabrication, bonding and packaging require technical skills and sophisticated equipment and facilities.

However, these steps are in some sense mechanical, in that once the fabrication process has been properly established no changes are required in order to produce a completely different integrated circuit. Nonetheless, because of the enormous capital cost and operating cost of such fabrication facilities only a very few large companies could afford the risk of establishing a fabrication line.

Full Custom Design

The so called silicon foundry approach to integrated circuit design is an experiment aimed at completely restructuring the semiconductor industry in such a way that anyone with an idea can get that idea cast in silicon at a reasonable cost. To achieve this end the "thought stages" associated with design are separated from the "mechanical stages" associated with fabrication.

The resulting structure is similar to that found in the hobby photography industry. Someone exposes a piece of film according to a known set of rules. Someone else processes it into the final picture. The film processor doesn't need to know what the pictures are, how they were produced, or what they will be used for. He only needs to know the type of film used. The photographer, on the other hand, doesn't require knowledge of the film processing techniques. He only needs a set of rules given by the film manufacturer about how to expose the film in order to produce satisfactory results. It is also the photographer who tests the results and makes the final judgement of the success of the picture taking exercise.

Essential ingredients in the seperation of design from fabrication are a clear set of design rules which when followed result in a satisfactory chip and an appropriate data format for communicating the design from the designer to the fabricator. Experiments, mainly at Universities in the U.S. and other countries have demonstrated the feasibilty of the foundry approach to custom IC design and fabrication.

Standard data formats have evolved which allow the designer and foundry to communicate and sets of simplified design rules have been produced which are manageable even for inexperienced designers. Along with these developments has come an explosion in the number of books and courses designed to disseminate the knowledge of how to design integrated circuits.

By the summer of 1982 over 30 companies in the U.S. offered silicon foundry services for nMos, CMOS, pMOS or bipolar circuits. Limited prototype and production runs were offered with turnaround time being from 4 to 12 weeks.

The immediate question which arises is, "How much does it cost?" There is a fixed minimum cost which is associated with manufacturing of the set of masks required for fabrication and for a prodution run of one batch of wafers. This cost is in the area of $US 30,000. A single batch of wafers typically produces several thousand identical circuits and thus the cost per circuit is low. However, circuit design always includes at least one prototyping run to demonstrate successful operation of the circuit. The cost of a minimun wafer run is the same no matter whether the circuit is a prototype or a proven design. Furthermore, several prototype runs are often required before the design is completely debugged. Thus development costs are still very high. The real difficulty with prototyping is that using the normal procedures you still get several thousand chips from a minimum run when only a few are really required for testing purposes.

There have been several recent innovations which have changed this situation dramatically The first is what is called a multiproject chip. Each chip on the wafer contains a number of independant prototype designs, usually between five and ten. During the bonding and packaging steps only one circuit on each chip is actually connected to the pins on the package. All the other circuits are dormant. However, enough samples of each circuit can be produced from a single wafer run to ensure adequate testing. The cost of the prototype production can therefore be shared by a number of different designers. Even with multiproject, chips many more samples are produced than are actually required. The obvious next step is to produce a set of masks which have many different chip designs on them. Each chip design can still be a multiproject chip. This results in what is called a multiproject wafer. Typically, thirty to forty independant prototype circuits can be produced from one fabrication run with the cost being shared.

One example of the success of this approach is the Australian Miltiproject Chip Programme (AUSMPC) coordinated by the CSIRO in Adelaide. Prototype designs have been accepted from Universities in Australia and New Zealand, from government rsearch organizations as well as from small industries both in Australia and the U.S. Fabrication is carried out on a strictly commercial basis at foundries in the U.S. and Australia. A turnaround time of three months has been achieved at the cost to the designer is around SA375 per square mm of chip area.

In Canada, a MPC experiment was started in 1980 as a cooperative venture between Queen's University and Northern Telecom Electronics Limited. Because of the success of the effort Northern Telecom offered to provide a foundry service for all Canadian Universities and Institutes.

Up to the present time coordination of design submission and distribution of fabricated chips has been handled by Queen's and 12 Universities have participated. The success has been so great that an independant, non-profit corporation is presently being established at Queen's to provide the coordinating service. One unique aspect of the program in Canada is that Northern Telecom offers the fabrication service free of charge to educational institutions in order to encourage improvement in the training of engineering students in the area of integrated circuit design.

What skills and equipment are required to taks advantage of silicon foundry services? The most essential ingredient is skilled manpower with background in the areas of system design and circuit design. The detailed knowledge required for the mask design can be acquired relatively rapidly Graduate students' in electrical engineering at Queen's enter the program with some system and cirucit design experience but with essentially no background in the details of integrated circuit design. During a single 12 week course they not only learn the techniques of design but also produce a prototype design for fabrication. Typically, these designs contain between 1000 and 2000 components and are produced with the aid of a small computer and some very simple computer aided design tools.

Standard Cell Design

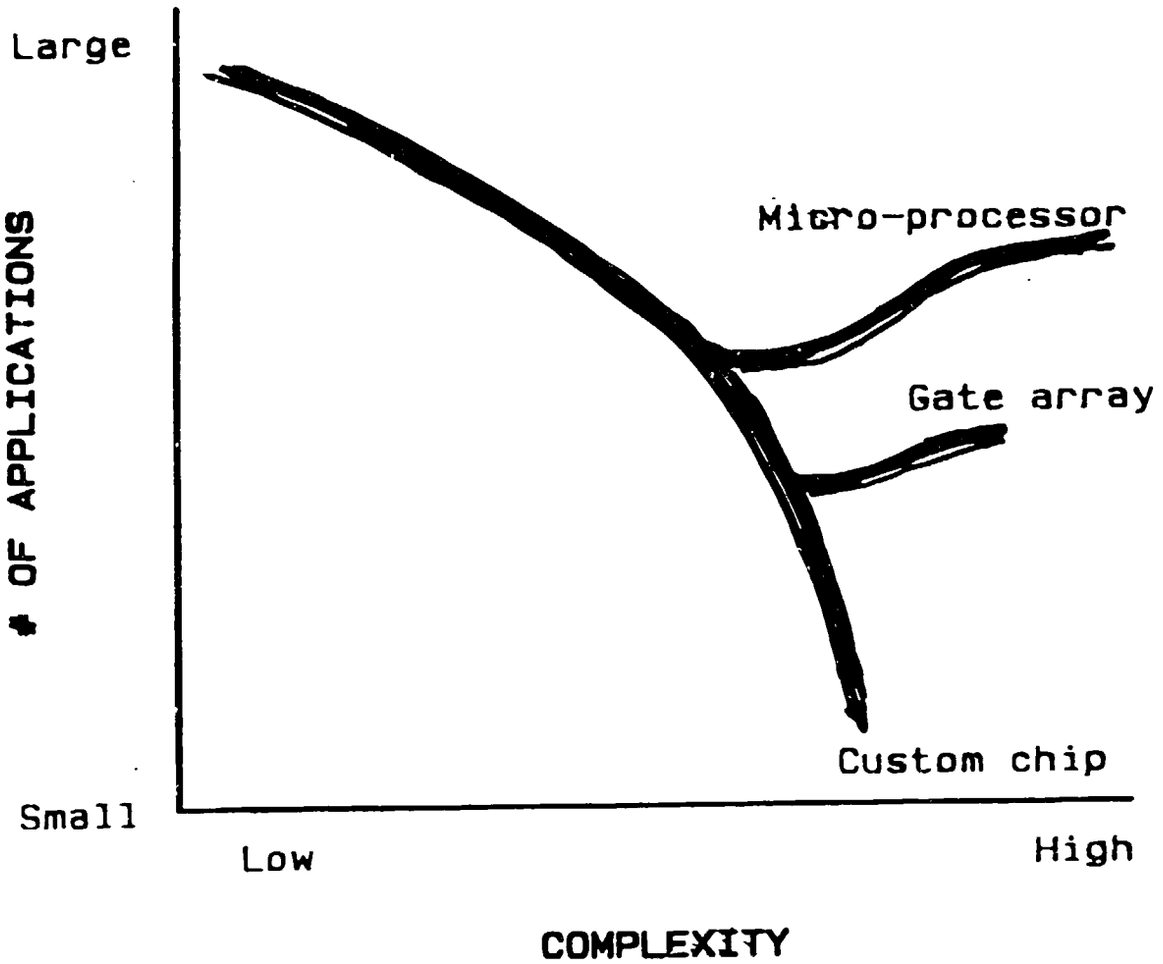
One of the initial tasks a designer of custom circuits faces is that of designing the subcircuits, such as gates and registers, which will be combined and used many times to produce the final design. A number of commercial companies have sprung up recently which supply a library of tested standard cells for a variety of different fabrication processes. The designer then has only to select, place and interconnect these standard calls in order to produce a prototype custom design Design time and therefore development cost and lead time are reduced and the design skills required are limited mainly to system design since most of the circuit design is incorporated in the library of standard cells.

CONCLUSIONS

Do these developments in the methods of design of integrated circuits mean that anyone can now compete at the leading edge of the micro-electronics revolution? The answer is certainly not. The cost of fabrication has dropped dramatically because of the silicon foundry services being offered, but complex circuits are still very expensive to design. There are however, many applications which require only simple circuits for which custom implementation is now cost effective. Also, because of the new services, no longer are huge volumes of identical circuits necessary before integration is economically viable. The trend towards increased access to fabrication will continue and a rapid proliferation of computer aided design tools will make more and more complex design possible. An integrated circuit solution to a specialized problem will become the rule rather than the exception.

ACKNOWLEDGEMENTS

Many of the background ideas have been presented by various authors in a collection of papers in a book "The Micro-electronics Revolution" edited by T. Forester (MIT Press, Cambridge, Mass, 1981). The details of present foundry and gate array services were found in "VLSI Design" a bimonthly magazine published CMP Publications Inc., Alto, Ca.


Large
OF APPLICATIONS
Small
Micro-processor
Gate array
Custom chip
Low
High
COMPLEXITY

GATE ARRAY TECHNOLOGY

Advantages	- Low cost
	- Rapid turnaround
	- Many technologies available
Disadvantages	- Inefficient use of area
	- Less than optimum performance
	- Fixed number and type of gate available

GATE ARRAY SUPPLIERS

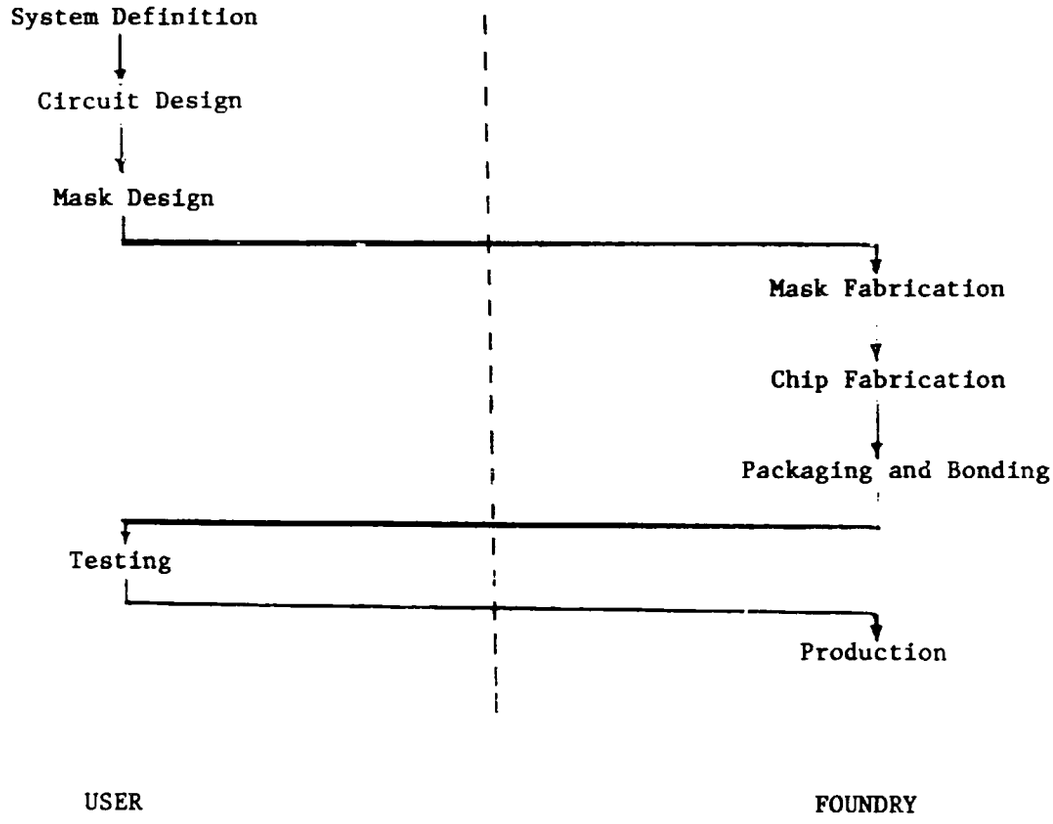
January 1982

NUMBER	: 35
TECHNOLOGIES	: nMOS, CMOS, Bipolar, Linear
TURNAROUND	: 2 to 4 weeks
COST	: Low

TRADITIONAL MICROCIRCUIT DESIGN STEPS

System Definition
↓
Circuit Design
↓
Mask Design
↓
Mask Fabrication
↓
Chip Fabrication
↓
Packaging and Bonding
↓
Testing
↓
Production

SILICON FOUNDRY APPROACH TO CUSTOM INTEGRATED CIRCUIT DESIGN



SILICON FOUNDRIES

Summer 1982

NUMBER	: Over 30
TECHNOLOGIES	: nMOS, pMOS, CMOS, Bipolar
DATA FORMAT	: CIF, masks, standard data base formats
MINIMUM QUANTITY	: Prototype 5 to 20 wafers Production 25 to 100 wafers
TURNAROUND	: 4 to 12 weeks
COST	: Variable

REDUCING PROTOTYPING COSTS

MULTIPROJECT CHIPS:

- many independent designs occur on same chip
- only one is bonded to package pins

MULTIPROJECT WAFERS:

- many independent chips occur on the same wafer
- each chip can be a multiproject chip

RESULT

- fixed minimum cost is shared by many designers
- each designer receives an adequate number of chips for testing

AUSTRALIAN MULTIPROJECT CHIPS

PARTICIPANTS	: Government Organizations Universities - Australia and New Zealand Industries - Australian and American
COORDINATION	: CSIRO, Australia
FABRICATION	: in USA and Australia
TURNAROUND	: 3 months
COST TO DESIGNER	: A$375 per square mm.

CANADIAN MULTIPROJECT CHIPS

PARTICIPANTS	: Canadian Universities and Institutes
COORDINATION	: Canadian Microelectronics Corporation (an independent non-profit company)
FABRICATION	: Northern Telecom. Canada
TURNAROUND	: 4 to 8 months
COST TO DESIGNERS	: none

CUSTOMIZATION HIERARCHY

PORTION OF WAFER PROCESSED	LEVEL	DEVELOPMENT COST	LEAD TIME
0%	Full Custom	$50-200K	9-10 months
0%	Standard Cell	$30-90K	4-2 months
80-90%	Gate Array	$5-20K	1-2 months

CONCLUSIONS

- Microelectronics evolution is making integrated circuits cost effective for less complex applications
- Low volume applications can be implemented economically
- The essential skill required is system design