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UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION
Vienna International Centre, P.O. Box 300, 1400 Vienna, Austria
Tel: (+43-1) 26026-0 · www.unido.org · unido@unido.org

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MICROPROCESSOR APPLICATION ENGINEERING PROGRAMME

DP/IND/84/030

INDIA

Technical report: Standardization of interfaces*

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of Andrew M. Norton, expert in microprocessor hardware and software development

Backstopping officer: V. Smirnov, Engineering Industries Branch

United Nations Industrial Development Organization
Vienna

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* This document has not been edited.

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ABSTRACT

This report documents the expert's return mission to India during the period Dec. 3 - 17, 1988. The first part of the mission involved attendance and presentation of a paper at the International Seminar on Microprocessor Applications for Productivity Improvement in New Delhi 6-8 December 1988.

The second part of the mission consisted of a return visit to the Southern Regional Centre of the Microprocessor Applications Engineering Programme based at Indian Telephone Industries in Bangalore. The experts activities consisted of project reviews, discussions and meetings with MAEP personnel.

This report briefly examines data communications interface standards relevant to the on-going work at the Southern Regional MAEP Centre. It examines project progress since the initial mission to Bangalore, May - July 1988 and details current project status as well as recommendations, observations and conclusions of the expert.

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1. INTRODUCTION

The objectives of the mission as Expert in Standardization of Interfaces as originally described under the job description DP/IND/84/030/11-08 were to include:

- appraisal of the current status of microprocessor applications in the Indian industry
- appraisal of the objectives, status and results of various system engineering development projects going on in various centres
- participate in hardware and software project discussions
- impart training of project personnel on new methodologies for microprocessor based systems engineering
- presentation of a final report, setting out the findings of the mission and recommendations to the government on further action which might be taken.

The expert received an invitation from the Chief MAEP Coordinator, Dr. Krishna Kant, to attend and present a paper at the International Seminar on Microprocessor Applications for Productivity Improvement (INMAP88) in New Delhi during the period Dec. 6-8.

The remainder of the mission concentrated on communications interface standards at the Southern Regional MAEP centre at the Indian Telephone Industries in Bangalore. This return mission to Bangalore was to review progress made on various projects and indicate current project status.

2. COMMUNICATION INTERFACE STANDARDS

Communication interface standards have been proposed largely by two international organizations: CCITT (Consultative Committee on International Telephony and Telegraphy), and ISO (International Standards Organization). The ISO has developed a network architecture model known as OSI (Open Systems Interconnection or CCITT X.200) which is the accepted logical model used for distributed data networks. ISO defines an open system as a system that can interoperate with other computers, perhaps of a different manufacturer, through a network. The OSI reference model serves as a common basis for comparison of network architecture and a framework for network standards acceptable to all manufacturers providing compatibility between products offered by different vendors. It supports evolutionary changes in the network protocol to reflect changes in technology since each layer acts as a seperate module. International standards have been defined and are being defined at each layer. The OSI model is a general model and applies both to wide area networks as well as local area networks.

2.1 The OSI Reference Model

The OSI reference model is composed of 7 layers: physical (lowest layer or level 1), data link, network, transport, session, presentation and application (uppermost layer or level 7). This layered architecture approach decomposes complex data communications problems into managable pieces with well defined interfaces. Layers are well defined as well as interaction between layers. The upper layers use services provided by the lower layers. Adoption of the OSI reference model has led to standards being defined that offer widely accepted means of meeting each layers requirements.

The Physical layer provides the electrical interface and physical path for bit by bit transmission. It defines the characteristics of the signals and specifies mechanical properties. This layer provides the only real connection between nodes. Major physical layer standards include RS232C/V.24, V35, X.21 and X.21bis.

The Data-link layer defines the rules of how the physical layer is shared among the nodes. It is responsible for error-free data transmission or data integrity between adjacent nodes across a data circuit. Data-link layer standards include HDLC, LAPB, CSMA/CD and token passing.

The Network layer is responsible for routing data packets through the network. It is an essential function for wide area networks but only necessary for local area networks for inter-network communications. Major standards include X.25 Packet layer/ISO 8208, ISO 8880/3, ISO 8473.

The Transport layer is considered the interface boundary between the upper layers (implementing high level protocols) and the lower layers (network, data-link, physical). This layer hides the existence of a data circuit from the lower layers as well. It is responsible for end-to-end control and partitioning of messages into data packets for transmission to the lower layers. Standards include CCITT X.224/ISO 8073 and the DARPA TCP.

The Session layer is concerned with dialogue management and synchronization. This layer establishes the session while negotiating parameters, session control and session termination. Standards include the CCITT X.225/ISO 8327.

The Presentation Layer is concerned with data formatting. It selects, negotiates and transforms data transfer syntax as required. This layer would be concerned with code conversion, data compression and data encryption. Standards include ISO 8823/X.226 and ISO 8825.

The Application Layer contains the processes that use the network. Typical network applications include electronic mail, file transfer and electronic funds transfer. Application standards include the CCITT X.400 series Message Handling Subsystem and the ISO 8571 FTAM (File Transfer Access Management).

Interaction between layers is defined by the service primitives between adjacent layers. Four types of service primitives are defined: request, indication, response and confirm.

2.2 The X.25 Standard

CCITT recommendation X.25 was first adopted in March 1976 and has gained widespread acceptance since then. It defines the communications interface standard between DTE (data terminal equipment) and DCE (data circuit terminating equipment) for packet mode operation on a public data network. X.25 recommends the use of existing protocols for the first two levels (physical and data-link layers) while its main focus is on level 3 (network layer or packet layer in X.25 terminology).

X.25 recommends two physical layer standards: X.21 and X.21bis while V.35 is also used. At the data link layer it specifies two protocols: LAP (not recommended for new implementations) and LAPB (Link Access Procedures Balanced. Both LAP and LAPB are subsets of the international standard High Level Data Link Control (HDLC). At the network layer it specifies the packet level procedure, establishment of end-to-end virtual circuits and controls virtual calls in a PDN (public data network.

The X.25 standard provides access to a PDN, provides data concentration, guarantees sequential delivery of data packets and permits establishment of multiple virtual circuits. Statistical Time Division Multiplexers often use X.25 to concentrate information from various data channels. In order to support asynchronous terminals (non-packet mode DTEs) a protocol conversion can be accomplished by the use of a PAD (Packet Assembler Disassembler) which hides the existence of a packet switched network from the terminal. PAD standards include CCITT X.3, X.28 and X.29.

2.3 Local Area Network Standards

Local area networks are data networks covering a small geography as in an industrial complex or building. They are private networks used by a single organization with a short distance between users. They provide access to a large number of devices and users. Typical applications include data processing, distributed processing, office automation, electronic mail, file transfer, electronic filing, resource sharing, factory automation and building management.

The IEEE 802 or ISO 8802 standard defines the two lower layers of the OSI reference model for local area networks. The data link layer is divided into two sublayers: Logical Link Control (LLC) and the Media Access Control (MAC). The LLC defines the frame formats and types and is based on but is not a subset of the international standard HDLC. These are are series of standards all using the same LLC but differing in the access control method or MAC.

The 802.2 standard is the LLC specification. It is an interface service spec to the network layer above, defines the LLC procedures and an interface service spec to the MAC below. It defines calls for an unacknowledged connectionless service known as DATAGRAM service. Although based on HDLC, it has been extended for multistation, multiaccess environment of a local area network.

The 802.3 spec specifies a baseband bus, CSMA/CD (Carrier Sense Multiple Access with Collision Detection) and either coaxial cable for 10Mbps throughput or twisted pair for 1Mbps throughput as well as cable lengths associated with each implementation.

The 802.4 spec uses a token-bus access method, broadband and 5 or 10Mbps throughput. It uses CATV cable and is mainly used in MAP (Manufacturers Automation Protocol) applications. A de facto baseband standard based on the 802.4 access method is ARCNET.

The 802.5 and 802.6 specs use token ring and slotted ring access methods, respectively, with either twisted pair or fiber optics with 4 - 16Mbps throughputs.

2.4 Application Layer Standards

The application layer of the OSI reference model allows full communications between users of OSI networks. Standards for the lowest four layers (physical, data-link, network, transport) specify mechanisms for reliable transfer of information across the communications network. Session and presentation layer standards specify the mechanism for dialogue management, synchronization and syntactical representation of the transferred data. Application layer standards define conceptual schemes that allow application processes to communicate in an agreed upon manner. These schemes define the rules governing the data transfer, the associated semantics and syntax employed. The application layer is the only layer that interfaces with the application process. Two application layer protocols and standards that have received a large amount of attention are: File Transfer, Access and Management (FTAM) and Message Handling Subsystem (MHS).

Each of the OSI application layer standards requires various subsets of presentation and session layer services. Transport layer services then provide access with specified class of service to the lower layers for communication over the data network.

2.4.1 Message Handling System CCITT X.400 Series Standards

The CCITT X.400 series is a collection of standards allowing users to exchange messages on a store and forward basis. Two message handling services are provided: Interpersonal messaging (IPM) and Message transfer (MT). IPM provides a messaging service between people such as electronic mail while MT supports general purpose message transfers between applications. Mail services implemented in conformance to the standard allow networks from different vendors to interchange mail. X.400 itself is the service specification presenting a reference model for mail interchange. It defines objects such as the mail envelope, User Agents (UA), Message Transfer Agents (MTA), Message Transfer System (MTS) and Message Transfer Service Elements.

The User Agent assists the originator with message preparation, formats user messages, interacts with the message transfer system (MTS) and delivers messages to the receipient. It may provide other local services such as word processing, document exchange, filing and report generation. The Message Transfer System consists of message transfer agents (MTAs). The MTAs relay messages between UAs over communications links. The MTS provides a general, application independent store and forward message transfer service.

Mandatory and optional service groups are defined by the specification for services such as: access management, delivery time stamp indication, deferred delivery, delivery notification, multi-destination delivery, probing and alternate recipient assignment.

2.4.2 ISO 8571 File Transfer, Access and Management (FTAM) standard

The FTAM spec defines the services, procedures and primitives associated with file transfer, file access and file management. File transfer moves a file between open systems. File access permits inspection, modification, replacement or erasure of part of a files contents. File management permits creation and deletion of files as well as inspection and manipulation of the file attributes.

FTAM services are accessed by a terminal via a user interface which permits issuance of FTAM commands. It is a connection oriented protocol using common application service elements for session establishment and termination. Once an association is established between FTAM users (known as the FTAM regime), file selection, file open and data transfer services may be invoked. Functional units describing the associated services, file service primitives and transfer sequences are specified.

3. RECOMMENDATIONS

Specific recommendations with regards to the southern regional MAEP centre in Bangalore follow. It should be noted that many of the recommendations as specified in this expert's previous report dated 23 August 1988 still apply.

3.1 Regional MAEP project coordination remains of prime importance to the ongoing progress of MAEP projects. With the resignation of the previous project coordinator, an MAEP project coordinator must be found as soon as possible.

3.2 MAEP project coordination must be considered a full time position. The host organization for MAEP centres should insure that the MAEP project coordinator be given all facilities permiting MAEP to function autonomously.

3.3 In spite of available facilities within the Indian Telephone Industries, services provided to the MAEP centre continue to be inadequate. Access to printed circuit board design and fabrication facilities should be improved and better turn around time provided.

3.4 The ITI management together with the Dept. of Electronics should decide how communication network products developed by the MAEP group can be integrated with standard network software packages to provide a system solution available to users of networking products.

3.5 The ITI management together with the Dept. of Electronics should investigate technology exchange agreements with vendors of network software packages already available and currently used within India. ITI uses network software packages internally and the possibility of integrating these packages along with MAEP developed network products should be thoroughly investigated.

3.6 Additional UNIDO expert assistance should be provided to this centre with emphasis on computer communications network software, software design engineering and computer communications standards.

3.7 Additional UNIDO expert assistance should be provided to all centres with emphasis on technical project management and systems engineering.

4. ACTIVITIES OF THE EXPERT DURING MISSION

Activities consisted primarily of two parts: participation at the INMAP88 seminar in New Delhi during the first week of the mission, the second week consisting of project discussions and design reviews at the Southern Regional MAEP Centre at the Indian Telephone Industries in Bangalore.

4.1 INMAP '88 Seminar

The International Seminar on Microprocessor Applications for Productivity Improvement sponsored jointly by the Government of India, Dept. of Electronics (DoE) and UNDP was held in New Delhi at the Hotel Ashok from 6-8 December 1988. The expert participated in the seminar, presenting a paper (see Appendix III) and as chairperson for the session on Microprocessor Applications in Communications.

4.2 Project Discussions and Design Reviews

The expert reviewed project progress and current project status since the last mission to the Southern Regional MAEP Centre at Bangalore. The current projects that were reviewed were:

4.2.1 A Local Area Network communications board for the PC bus based on the ARCNET technology from Standard Microsystems Corporation.

4.2.2 An intelligent Multiplexer/Demultiplexer using statistical multiplexer techniques.

4.3 Lecture on Computer Communications Standards

An introduction to the International Standards Organization (ISO) Open Systems Interconnection (OSI) reference model was presented as applicable to the current communications projects. Relevant communication standards are presented in section 2 of this report.

4.4 Other Activities

Other activities included:

4.4.1 Discussions with DOE coordinators regarding centre activities and future projects

4.4.2 Discussions with Indian Telephone Industries Executive Director for Microelectronics and Computer Division.

5. INMAP '88 Seminar

The International Seminar on Microprocessor Applications for Productivity Improvement was given 6-8 December 1988 in New Delhi. It was organized jointly by the Dept. of Electronics and UNDP.

5.1 Introduction

The INMAP '88 seminar permitted the expert to meet one of the objectives outlined in the general introduction (section 1): appraisal of the objectives, status and results of the various system engineering development projects going on in the various MAEP centres. Papers were presented on microprocessor applications in the various service sectors as outlined in appendix II. Engineers from MAEP centres, industry, universities and research centres presented papers on the respective themes providing the expert with the opportunity to appraise the state of the art in microprocessor design, development and applications in India.

5.2 Summary of Main Points raised by Delegates during Concluding Discussion Session

A summary of main points raised by delegates during the concluding discussion session follows. These notes were jointly compiled by the following UNIDO experts who attended the discussion session:

C.A. Hobson	U.K.
A.M. Norton	USA/Mexico
J.L. Peters	Netherland
D. Popovic	FRG
W.R. Slater	USA
B.G. Taylor	Switzerland
E.J. Wightman	U.K.

5.2.1 Sensors. There is a need to define what is available in India, possibly in the form of a data bank. Sourcing is a major problem affecting the whole of MAEP. Consideration should be given to forming an indigenous sensor development programme.

5.2.2 Cooperative projects are recommended between Industry, MAEP, universities and research establishments (CERI etc.).

5.2.3 During the MAEP activities to date, results show that industry has a better track record of achievement than MAEP centres which are part of D.O.E. or are university based. Examples: Bangalore and Ranchi have performed better than Pune and Jabalpur.

5.2.4 The end products of the MAEP were queried. Who utilized the outputs of the programme?

5.2.5 MAEP should promote software with system engineering and applications of microprocessor based systems.

5.2.6 There is a need for pilot projects for future systems development to develop project management expertise.

5.2.7 There is a need for awareness and education programmes at all organizational levels, from chief executive, directors, managers, development engineers and shop floor, with emphasis on senior management levels.

6. SOUTHERN REGIONAL MAEP CENTRE - BANGALORE

The Southern Regional MAEP Centre is based at the Indian Telephone Industries in Bangalore. MAEP activities are focused on communications applications with current MAEP projects encompassing local area networks and statistical multiplexer for interface to wide area networks.

The MAEP Project Coordinator, Mr. Rajaram resigned from ITI effective November 30, 1988. Mr. Rajaram was considered to be a key person to this MAEP group as well as to ITI. Dr. Prabakhar, the executive director of the Microelectronics and Computer Division is currently managing the administrative aspects of the MAEP until a suitable replacement can be found for the Project Coordinator.

The new building which will house the MAEP labs, equipment and personnel is now expected to be completed later this month (Dec. 1988). This building will provide a degree of autonomy within ITI as well as the necessary physical facilities to the MAEP group.

6.1 Review of Current MAEP Projects

6.1.1 Local Area Network Communications board for the PC bus

The main objective of this project was to provide local area network communications for the PC bus. Two prototype boards have been built based on the ARCNET local area network technology. Prototype hardware has been tested with two nodes on the network using menu driven software developed for demonstration purposes.

Hardware testing has so far been limited to tests with two nodes. The printed circuit board is currently being fabricated and it is anticipated that the boards will be ready for pre-production prototype testing in January. Orders have been placed for additional components which will permit testing of up to 6 nodes on the network. Delivery of the remaining components and the printed circuit board are required before additional hardware testing can proceed.

Menu driven software has been developed for demonstration purposes. The demo package permits the broadcasting of messages from a node, sending mail to a specified recipient which is stored in a mail directory as well as providing network status and limited management.

The anticipated completion date of the menu driven software package and a 6 node prototype network configuration remains March 1989.

6.1.2 Statistical Multiplexer

A hardware prototype of an intelligent multiplexer/demultiplexer has been developed and is currently being tested based on the specifications and design documents that were developed along with this expert during the period May-July 1988. A large portion of the hardware has been tested and is currently functional although there remain sections that still require testing.

Software implementation has been initiated and is in the early stages of development. The software design based on the concepts discussed by this expert during the previous mission has been completed.

The anticipated completion date of a finished prototype multiplexer with integrated hardware and software remains March 1989. It is the opinion of this expert that this date is quite ambitious and more time will be required to complete the software portion of this project.

6.2 Future Projects

Future projects were discussed with MAEP engineers. Continuing along the same product lines as the current development projects, future projects identified could include:

6.2.1 Integration of the PC based Standard Microsystems Controller chip (highly integrated version instead of seperate components) on the PC bus as a second revision to the current project.

6.2.2 Development of a CSMA/CD network interface board for the PC bus

6.2.3 Using the same statistical multiplexer hardware, modifying the software to produce a Packet Assembler Disassembler (PAD) for interfacing non packet mode terminals to X.25 packet mode networks

6.2.4 Development of an X.25 to ARCNET gateway providing local area network access to Public Data Networks.

6.3 National Seminar on Microprocessors and Communication Systems

A two day national seminar detailing the current status of microprocessor applications in communications is being organized by the Southern Regional Centre for MAEP jointly with the Dept. of Electronics. This national seminar will be given from Feb. 23-24, 1989 in Bangalore. The seminar is intended for technical personnel in the various sectors of communication engineering.

6.4 UNIDO Training Fellowships

Three engineers are presently undergoing training through the UNIDO fellowships in Germany and the U.S.A. The three engineers are: Chidambara, Somashekar and Nalinakshan. They are currently at the University of Bremen in W. Germany and will be proceeding later this month to the University of Southern California. They will have spent 2 months at the University of Bremen and 1 month at the University of Southern California.

It is proposed to depute two other engineers, Mohan and Roopchandar for continued training through the fellowship program early in 1989. Fellowship training will take place at the same two universities in W. Germany and the U.S.A.

APPENDIX I

Itinerary: A.M. Norton

December 3-17, 1988

Date	Activity
Sat., 3 Dec.	Leave Mexico for India.
Mon., 5 Dec.	Arrive New Delhi. UNDP Administrative briefing Meeting with Dr. K. Kant, Dept. of Electronics
Tues, 6 Dec.	Attendance at INMAP '88 Seminar
Wed, 7 Dec.	Presentation of Paper at INMAP '88 Seminar
Thurs, 8 Dec.	Attendance at INMAP '88 Seminar
Fri, 9 Dec.	Meeting with Dr. K. Kant, Dept. of Electronics Meeting with other UNIDO experts
Mon, 12 Dec.	Leave/Arrive Bangalore
Tues, 13 Dec.	Meeting with Dr. Prabhakar, Executive Director Indian Telephone Industries Meeting with MAEP Project Personnel for Project Reviews and Discussions
Wed, 14 Dec.	Meeting with MAEP Project Personnel for Project Reviews and Discussions
Thurs,15 Dec.	Meeting with MAEP Project Personnel
Fri, 16 Dec.	Leave Bangalore/Arrive New Delhi Meeting with Dr. K. Kant, Dept. of Electronics Leave New Delhi, India
Sat, 17 Dec.	Arrive San Francisco, California

APPENDIX II

International Seminar on Microprocessors & Productivity Improvement
Hotel Ashok, New Delhi, India
December 6-8, 1988

Session I: Microprocessor Architectural Advancements

Session II: Microprocessor Applications in Medicine

Session III: Microprocessor Applications in Railways

Session IVa: Microprocessor Applications in Service Sector

Session IVb: Microprocessor Applications in Communications

Session Va: Microprocessor Applications in Process Industries

Session Vb: Microprocessor Applications in Agriculture & Education

Session VIa: Microprocessor Applications in Steel

Session VIb: Microprocessor Applications in Test & Measuring Instruments

Session VII: Microprocessor Applications in Industrial Control

Session VIII: Microprocessor Applications in Manufacturing Automation and Standardization

Discussion Session: Microprocessor & Productivity: Technology and Challenges

APPENDIX III

Abstract of experts paper presented at INMAP88

Microprocessor Interfacing Techniques using Programmable Logic Devices

Andrew M. Norton, M.S.E.E.

Professor, Dept. of Electronic Engineering
Investigator, Institute of Advanced Studies
Universidad de las Americas, Puebla, Mexico

Expert Consultant, UNIDO

Methods and techniques used to interface the microprocessor with external devices and system components have been greatly influenced by the advent of Programmable Logic Devices (PLDs). While PLDs have evolved from first and second generation programmable AND-OR array architectures to the function specific and application specific devices of today, the use of PLDs has become the preferred method in solving digital design and microprocessor interfacing problems.

Interfaces designed with discrete logic ICs resulted in higher parts count, power consumption, development time and cost. Programmable Logic Device based implementations provide custom design solutions while shortening design cycle, reducing the number of ICs required, minimizing power consumption and resulting in a lower cost, higher performance design. Further, the user configurable features of PLDs permit design changes even in completed designs without PC board modifications.

Gate arrays and custom solutions do not always provide exactly the functions that are needed in an interface design. Function/application specific PLDs can provide the glue logic required to implement various system level buses with the desired degree of customization. While PLD technology is still relatively new and users are slow to accept new technologies, economic pressures combined with the need to compress more logic onto smaller printed circuit boards force todays design engineers to use Programmable Logic Devices.

In this paper, PLD architecture is briefly reviewed and PLD design tools examined. Application examples using programmable logic devices resolving typical microprocessor interfacing problems are included.