OCCASION

This publication has been made available to the public on the occasion of the 50th anniversary of the United Nations Industrial Development Organisation.

DISCLAIMER

FAIR USE POLICY

CONTACT

Please contact publications@unido.org for further information concerning UNIDO publications.

For more information about UNIDO, please visit us at www.unido.org

UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION
Vienna International Centre, P.O. Box 300, 1400 Vienna, Austria
Tel: (+43-1) 26026-0 · www.unido.org · unido@unido.org

RESTRICTED

17392

DP/ID/SER.B/641
16 February 1989
ORIGINAL: ENGLISH

SEMICONDUCTOR DEVICES AND ELECTRONIC SUB-SYSTEMS FOR TRANSPORTATION

DP/IND/84/015

INDIA

Terminal report*

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of the
Central Electronics Engineering Research Institute
prepared by the National Project Director

Backstopping officer: J. Fürkus
Engineering Industries Branch

United Nations Industrial Development Organization

Vienna

---

* This document has not been edited.

V.89 51648

CONTENTS

1. INTRODUCTION:

1. This terminal repor briefly presents an analysis of the project implementation and results obtained up to Nov. 20, 1988. It describes the activities, outputs and the extent to which the project objectives could be achieved and in line with the project document, it concludes with the recommendations for future UNDP assistance to translate the results achieved and likely to be achieved in the near future due to the expertise facilities developed by the project, into prototype fabrication and technology utilisation.

2. UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION (UNIDO) was the executing agency and COUNCIL OF SCIENTIFIC AND INDUSTRIAL RESEARCH (CSIR) India through Central Electronics Engineering Research Institute (CEERI) Pilani (Rajasthan) India was the implementing agency for the project.

3. The project commenced in Nov, 1984 four months behind Schedule of estimated starting date i.e. July, 1984. The project duration of three years was extended by one year up to Oct, 1988 on the basis of careful scrutiny of availability of materials & equipment and recommendation of Tripartite Review meeting held in January, 1987. The international component of the planned input of US$ 1,467,000 was reduced to US$ 1,402,335 (budget revision F). It was revised upwards to US$ 1,682,335 (budget revision J) on the recommendations of TPR meeting of Jan, 1987 and covers a total allotment of US$ 1,687,395 under budget revision L. The counterpart contribution planned was Rs.13,900,000 and against this the contribution of Rs.23,600,000 (Rs.18,800,000 for equipment Rs.4,800,000 for consumables) has been utilised. The actual counterpart inputs are estimated to be higher.

OBJECTIVES

5. Basically Electronic systems needed for all the Transportation systems are of three types: electronic control systems, data handling systems and safety systems. In view of the inherent advantages of energy saving and other features relating to the emerging technology of Electric vehicles, the R & D efforts on this project were concentrated on Integrated Electronic Control Systems. The electronic Controls for current range of vehicles and future electrical vehicles are based on electrical motor control using inverters (A.C. Motor Drives) or choppers,(for D.C.Motor Drives), and continuous effort on making them energy efficient is being committed by many countries. Compared to conventional systems the electronic control systems are much more precise in their operation and do not involve moving parts with inherent wear and tear. In addition to this electronic control devices are highly energy efficient.

6. Use of variable frequency three phase solid state A.C. Motor drives for Traction applications has steadily grown during the last decade largly due to the development of high power inverter grade semiconductor devices. These drives will also be useful for other requirements of drives used in process control industry. The ideal drive for these applications is a micro processor based PWM AC Drive. Such a drive when developed will cover very wide range of applications, because of the inherent Software Control available with Microprocessor based systems.

7. These high efficiency drives require Application Specific Integrated Circuits (ASICs) to perform brain functions (i.e. Logic & Control) Power Transistors to perform muscle function (i.e. driving the motor) and Hybrid microcircuits to provide intermediate links.

8. The project envisaged the development of application specific integrated circuits, Power Transistors, Hybrid microcircuits and Solid State AC Drives.

The development objective and immediate objectives were defined in the project document as follows:

A. Development objective:

The development objective of the project is to promote the utilisation of electronic systems for transportation by increasing the operational efficiency of electric vehicles and to achieve a self-reliant product development capacity in this field.

B. Immediate objectives: *

The immediate objectives of the project are:

(i) Development of power transistors for power control in electric drives for transportation.

(ii) Development of custom designed monolithic integrated circuits especially for use in transportation

* Same as per original proposal

(iii) Development of hybrid integrated modules for control of electric drives especially for transporation.

(iv) Development of Silid State AC Motor Drives and System packages to suit the requirement of transportation, including electrically driven vehicles.

9. The objective of the project were conceptualised to be achieved in the following stages.

(i) Conceptual paper design of system packages Integrated Circuits, Power Transistors and Hybrid Microcircuits (using CAD wherever applicable).

(ii) Implementation of design and iteration.

(iii) Prototype development,

(iv) Batch fabrication of semiconductor devices.

(v) Testing of the semiconductor devices independently and in the system package.

III. ACTIVITIES CARRIED OUT AND OUTPUTS ACHIEVED

10. Based on the main activies outlined in the project document, detailed work plan was prepared in May 1985. This work plan contained the major activies as given in the project document and subactivities with their estimated date of start and duration of the activities.

The work plan was reviewed periodically by the project Director, in 6 monthly progress reports, and by PAC and TPR. Depending upon the external constraints target dates of the activities were revised so as to correspond to

revised completion date of the project. The activities were divided into general activities and Project activities. These activities were carried out through the project personnel, UNDP provided expert/consultants and UNIDO assistance. A brief account of the activities according to which the project was implemented are given below:

a. General Activities

i) Preparation of detailed work plan for implementation of the project.

ii) Budgetary provision and assignment of national staff to provide counterpart inputs.

iii) Identification of International Consultants and making arrangments.

iv) Identification of sources of supply of equipments based on the Formulation of specifications, prepared through detailed technical discussions.

v) Identification of places for fellowship training.

vi) Arranging PAC and TPR meetings and preparation of notes for discussion in these meetings.

vii) Interaction with UNDP/UNIDO, CSIR and DEA in relation to project implementation.

b. Project Activities

i) Placement of orders for the equipment.

ii) In consultation with CSIR and UNDP a Project Advisory Committee (PAC) to monitor the progress and to guide on the implementation of the project was constituted. The constitution and terms of reference of the PAC are given at Annexure I. The action taken on the recommendations of PAC are given in Annexure XV.

iii) Coordination of Specifications of Devices and system. After drawing the specifications of the system the input output parameters and other specifications of power transistors, hybrid circuits, and monolithic integrated circuits were evolved, through brain storming sessions and periodic discussions with experts.

iv) The above conceptual specifications were discussed among project personnel and consultants and design rules etc. were prepared.

v) The project was carried out basically through the following stages.

a) Design of the system, sub-systems and devices (using CAD wherever applicable).

b) Processing the devices

c) Testing the devices/sub-system

d) Iteration.

11. The availability of the project personnel was adequate (Necessary internal mobilisation of personnel was done wherever required). The consultants/experts were available for the project. The consultants helped the project in defining the design parameters more accurately, designing and processing. Some of the consultants accepted the project personnel for fellowsip training and also assisted in design and processing of monolithic integrated circuits (Prof. P. Jespers, UCL Belgium). Out of a provision 23.7 m/m of consultant 22.3 m/m have been utilised. The list of the experts is given in Annexure - II. The action taken on the recommendations of UNDP consultants is given in Annexture XIV.

12. A list of the scientific and technical personnel of Central Electronics Engineering Research Institute is given at Annexure - III.

13. 18 Project personnel received fellowship training abroad at Centres of higher learning and technology. Three study tours by National Expert, Project Director and Area Coordinator, Semiconductor Devices Area were undertaken. The details are given in Annexure IV and V. The fellowship programme was specific and involved the fellows working actively on ongoing research programmes.

Two of the fellows, e.g. Dr. Chandra Shekhar and Sh. OP Wadhawan, designed and processed the two IC chips at UCL Belgium.

14. Procurement of Equipment

The procurement of equipment was carried out by UNIDO and CEERI. The equipment procured under UNDP funds and counterpart funds is given at Annexure VI and VII respectively. The total equipment (expendable and nonexpendable) procured under UNDP was of the order of $ 1,257,072. Some comments on the implementation of equipment procurement are give below:

i) Prior to sending requisition on major pieces of equipment, the project management carried out preparatory work of identification of equipment meeting the desired specification and possible vendors.

ii) Most of the equipments were commissioned either directly by project personnel or with the help of vendors' representatives/Engineers.

iii) One piece of equipment i.e. Cold Wall Vacuum furnace could not be commissioned till date. The supplier of the equipment also was not cooperative enough to help the Institute in sorting out problems of this equipment inspite of continuous follow up and sustained efforts of the Project personnel & UNDP officers. The non-commissioning of this furnace has delayed the delivery of the out put.

iv) Another piece of equipment Laser Trimming System could be commissioned by the vendors only after two years and it worked upto the specifications only for less than two months. All efforts to pursuade the vendor for providing warranty service have failed.

v) The position of procurement of expendable equipment was satisfactory except for the above two cases,for which alternative arrangements through outside assistance had to be made by the Institute. The authorisation for field purchase were very useful.

vi) The following two cases of procurement have caused considerable delay in implementation of the project.

Procurement of 300 Amps. power transistors. The first indent for this purchase was raised in 1984, but these items of expendable equipment could not be procured. A few pieces would be procured through counter part funds only by the end of 1987. This resulted in delays for the assembly and testing of the system module. A respective equipment requisition was sent to UNIDO in February '88. Goods were ordered and shipped on 9 December 1988.

vii) The order for the procurement of packages for 300A transistors were placed mid-February '88. The delivery of goods, however, has been delayed very much thereby affecting the project progress.

15. The interation with Project Advisory Committee, Experts/Consultants, Indian Industry, Department of Electronics, Govt. of India and other agencies helped in the project implementation. The scientific and technical work of the project to meet the outputs was carried out under four different groups, viz (A) Power Transistors; (B) Monolithic Integrated Circuits; (C) Hybrid Integrated Modules; (D) Solid State AC Motor Drives and System Packages.

Continuous interaction between groups was established through day-to-day working level contact and periodic meetings arranged by the Area Coordinator and Project Director and Project Leaders associated with the project teams.

16. A note on the nature of the products and processes developed under the UNDP Project is placed at Annexure VIII.

17. The details regarding Hard and soft out of the four groups of the project are given at Annexure IX.

18. A list of engineers/scientists trained within the country is given at Annexure X.

19. The details regarding linkages established with the industrial organisations are given at Annexure XI.

20. The details of International collaboration in the subject areas covered under the UNDP project are given at Annexure XII.

21. The list of Seminars/Symposia/Workshops etc. arranged at CEERI is given at Annexure XIII.

A. DEVELOPMRNT OF 100 AND 300 AMPERE DARLINGTON POWER TRANSISTORS

(i) INTRODUCTION:

The recent addition of GTOs, Darlington Power Transistors and Power MOSFETs to the existing families of Bipolar Junction Transistors (BJTs) and thyristors have widened the choice for the selection of power switches for solid-state power control involving inverters and converters. At the same time, further developments in these original power switching devices to give them a competitive performance have added a new dimension to the power electronics field. In the low and medium power applications Power Transistors have started replacing thyristors because of their inherent advantages such as

a) Lesser number of power devices required compared to thyristor control because no commutation is required with transistors for turning them off.

b) Higher switching speed.

c) Lower losses and lower EMI problems.

(ii) Accordingly, in the development programme under UNDP Power Darlington Transistors were taken as intrinsic components for AC Motor Drives. At higher power rating, the current gain of an individual power transistor is low. Darlington configuration overcomes this problem to a larger extent due to its higher gain at high currents and it is widely accepted in PWM AC Motor drives for electric vehicles.

(iii) Computer Aided Design (CAD) approach and design results:

"CAD" as a tool has been used to design 100A and 300A Darlington Transistor. A separate design report on this has been submitted, which constitutes one of the important outputs of this project. The approach uses "Bipole" programme which has been equipped with physical models of heavy doping, base widening and emitter crowding effect and is capable of analysing the device laterally and vertically. Results obtained using CAD approach (Table AI) show that it is desirable to use thin emitter fingers which again reduces the effective emitter area, that is the silicon size for same electrical characteristics.

TABLE AI

SIMULATED RESULTS FOR JCmax AND CROWD FACTOR
(Composite gain and current Ic for device under study)

Jcmax A/cm2	I µm	B cm	hrs	Ic A	Vbe VOLTS	CROWD
79	650	64	10.0	40	0.826	0.50
68	550	25	10.7	47	0.845	0.59
41	350	66	9.6	74.6	0.803	0.80
23	250	64	10.3	35.8	0.747	0.90
22	200	16	10.2	7.5	0.736	0.93
16	150	64	10.2	17.0	0.718	0.99
85	4000	10	12.0	20.0	0.800	0.20

COMPOSITE DARLINGTON TRANSISTOR

Jcmax	Comp.hm	Ic	Vbe	CROWD
80	107.30	183	0.99	0.56
90	97.12	196	1.04	0.55
100	90.40	205	1.12	0.54

Based on CAD results, it has been possible to make emitter layout for the device. In the first stage, 100A transistor layout has been made as shown in Fig. A1. This single emitter geometry has emitters for input transistor T2 (Driver transistor) and output transistor T2 (output transistor), the emitter segments of output transistor T2 having p-layer region form a free wheeling diode 'D'. These different regions T1 ,T2 and 'D' have been connected through in-built diffused resistors R1 and R2 (which are formed on Metallization). Both input and output emitter segments have been made on single layout, to ensure same peak gain and breakdown voltage for both transistors. For ease of phtomasking, emitter fingers have been made little wider than computed finger width, to check the feasibility of design approach.

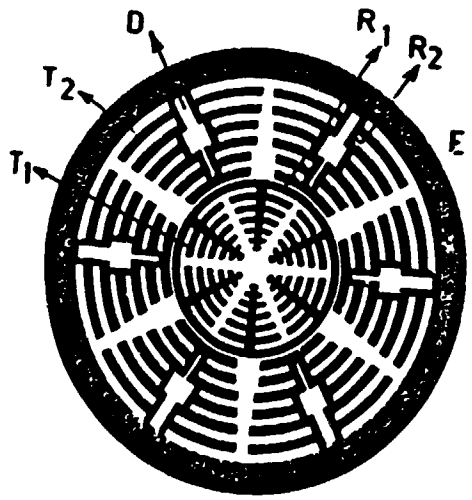


Fig. A1 Actual Emitter Geometry of 100 A Darlington Transistor.

IV. Devices Simulation for network analysis:

'WATAND' program has been used to study the theoretical switching behaviour and $h_{fe} - I_c$ variation, under different load conditions, of the designed transistor. It was noted in relation to the proposed application for AC Motor drives that most critical condition for this operation is inductive load therefore emphasis has been put to analyse the device during turn-off, with inductive load.

During inductive turn-off Darlington transistor must pass from the fully "on" stage to the "off" state as quickly as possible to minimize power loss. The ability of the device to withstand such current and voltage stresses during inductive turn-off is defined as RBSOA. To predict such ability of device, "WATAND" network circuit for inductive load is used as shown in Fig.A2.

In simulation study, it is assumed that device is already in the 'on' state and each section of emitters of the developed device is divided into five individual sub-sections. Simulated behaviour of collector current with time in these five sections of output transistor is illustrated in Fig.A3. It is found from such other simulated results that with increasing magnitude of reverse base current, the current focussing in the centre region just under emitter is enhanced and thus increases the temperature in that local region which makes device unstable. For present device the current density up to 87A/cm2 is obtained in simulation results while for initiation of "RBSB" the essential current density should be of the order of $160 A/cm^2$. This implies that even under large reverse base current power dissipation across Darlington transistor is not high enough as the product of $V_{CE}(t)$ and $I_c(t)$ at any time lies in the region bounded by V_{CE} and I_c, as predicted by Bipole programme.

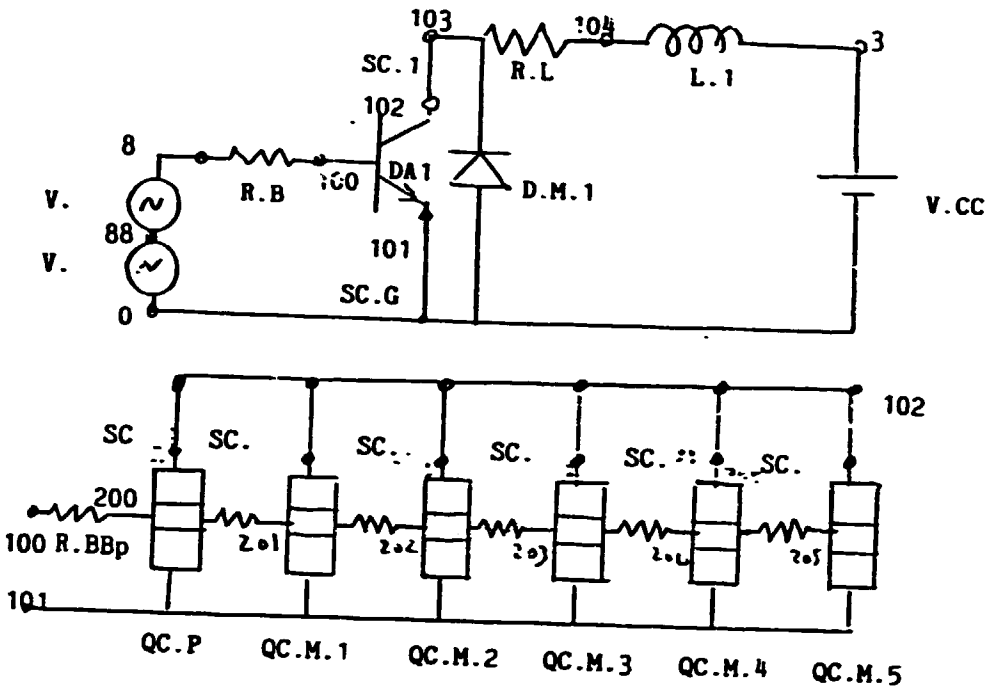


Fig. A2 Inductive circuit and sectioned representation of Darlington Transistor used in WATAND transient analysis.

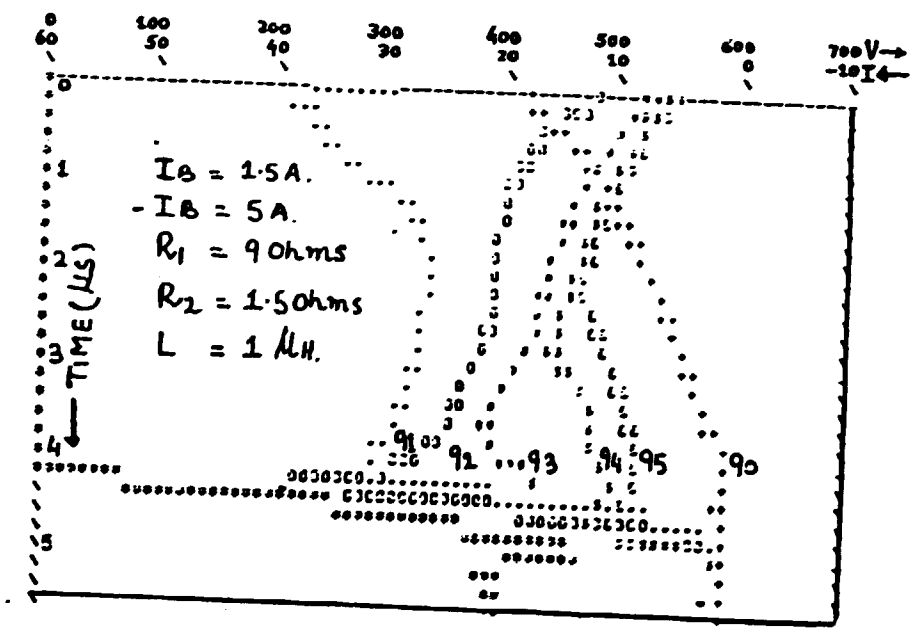


Fig. A3 Computed current variation with time in different emitter sections under inductive load condition.

vi. Based on approximate geometry, using CAD design approach, the physical and electrical parameters of 100A Darlington transistor have been tabulated in Table-AII.

CAD studies on 100A transistor have been extended to 300A transistor design and so upscaling of 100A emitter layout has been done to make emitter geometry for 300A transistor. The upscaled 300A emitter geometry as shown in Fig.A4, consists of dual base contact for fast recovery.

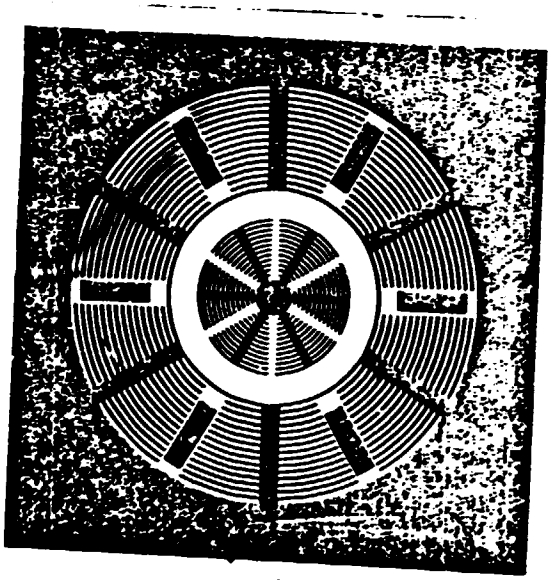


Fig. A4 CAD based geometrical layout of 300 A Darlington Transistor.

TABLE AII

Physical Parameter		Electrical Characteristics	
N_D	$10^{14}/cm^3$	Composite h_{fE} (V_{CE} = 5 Volt I_C = 100 A)	100
Epi thickness	85 um	$V_{CE\ sat}$ (at I_C = 100A)	1.9 Volt
Substrate Conc.	$10^{19}/cm^3$	V_{CBO}	856 Volt
X_j, N^+	9 μm	h_{fE1}	16
X_{jp^+}	22 μm	h_{fE2}	8.6
W_B	13 μm	V_{CEO}	625
W_C	63 μm	$V_{CEO\ sus}$	500 Volts
Q_B/D_B	1.185×10^{12} cm^{-4} sec.	t_{on} (I_C =100A, V_{CC} = 400 Volt, L = 10 μH)	1.2 usec.
Q_B	2.37×10^{13}	t_{off} (I_C = 100 A, V_{CC} = 400 Volt, L = 10 μH)	8 usec.
Ae_1	0.4879 cm^2	h_{FEO} at 50 A	300
Ae_2	3.002 cm^2		
R_1	9 ohms		
R_2	1.5 ohms		
Q_E/D_E	4×10^{13} cm^{-4} sec.		

Fabrication of Monoloithic Darlington Transistor:

VII. Fabrication Facility Set Up

On completion of designed emitter layout the fabrication facility for large area power devices, has been initiated. The planar device structure has been used for the fabrication of the following 100A and 300A Darlington transistor and therefore facilities for different fabrication processes have been established:

A. Sealed tube deep diffusion

B. Bevelling and contouring

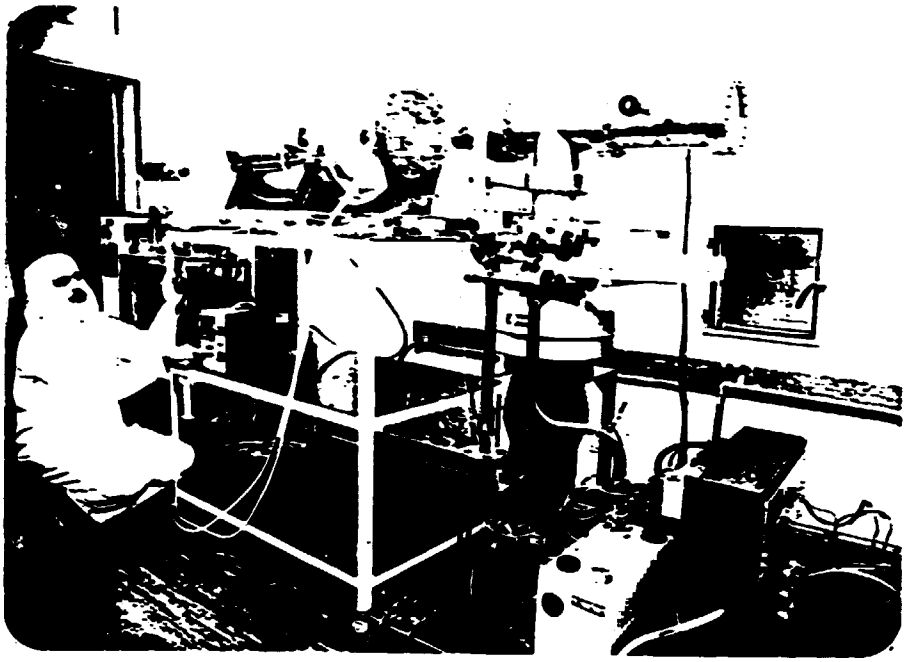
C. Spin Etching

D. Pyrogenic Oxidation

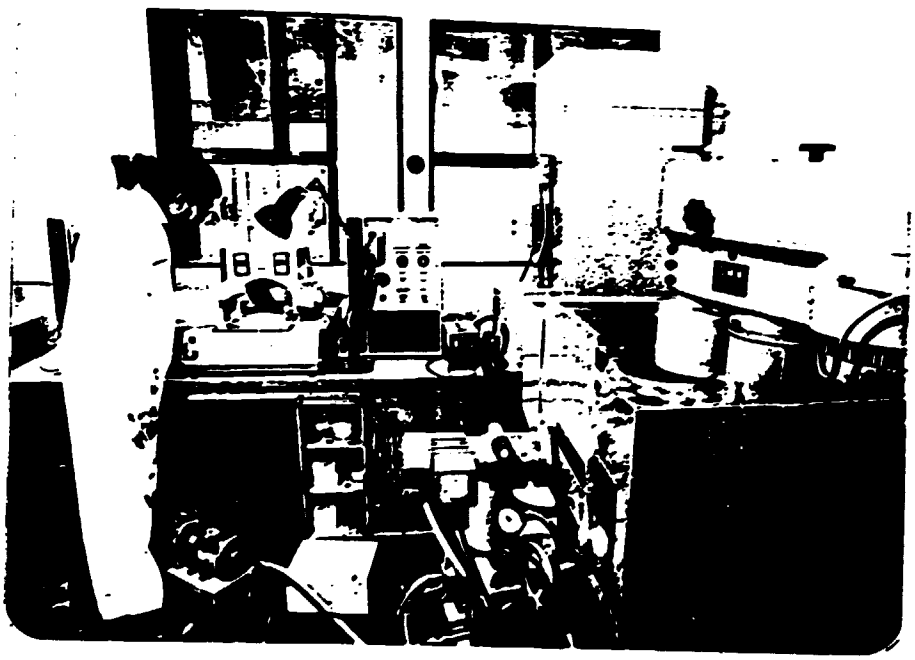
E. D.C. and A.C. measurement set up

a) Sealed tube deep diffusion:

Initial set up for diffusion has been replaced on procurement of VHS-6 Varian Vacuum System under UNDP Programme. To initiate deep diffusion for large area devices up to 3" a sealing adaptor for holding quartz capsule, was locally fabricated. Such a facility is a basic requirement for high voltage devices. Elemental gallium as p-type impurity has been used for deep diffusion because of its high diffusion co-efficient and low mismatch factor with silicon lattice. In sealed tube diffusion, uniform spread in sheet resistance and high lifetime have been achieved and large number of wafers could be diffused. Photograph 'AI' shows complete set up for sealed tube deep diffusion for high voltage junctions, commissioned by the CEERI project team.



Photograph 'A1' Sealed Tube Deep Diffusion



Phograph 'A2' Bevelling and Contouring Equipment

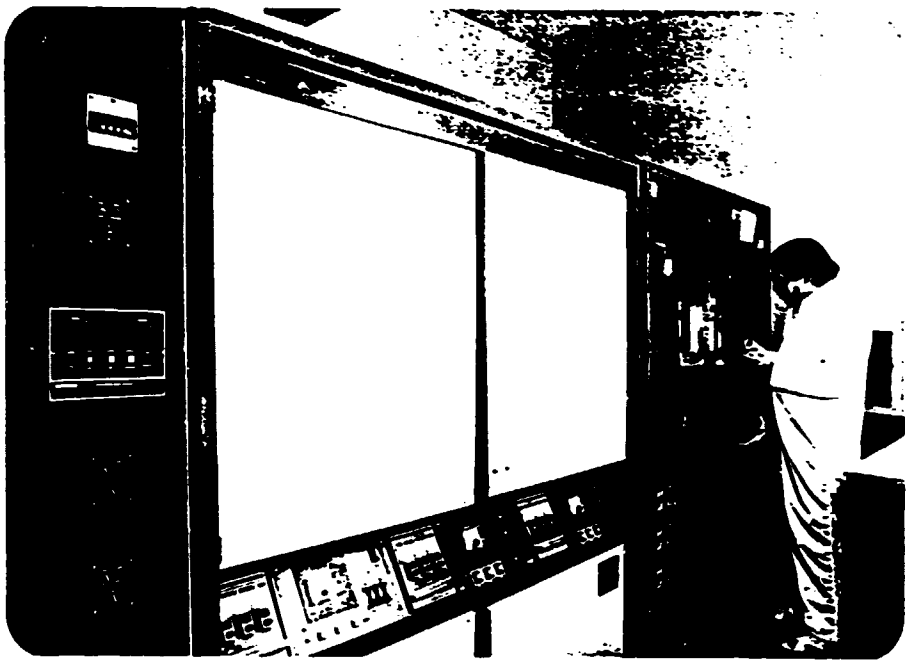
b) Bevelling and Contouring:

Planar structure has its limitations for high voltage junction due to the curvature effect It is very essential to control or shape the surface so that depletion region could be extended and does not tend to terminate at the surface. In present planar structure therefore shaping of the surface of p-n junction has been introduced to achieve high breakdown voltage. Bevelling and contouring set up is shown in Photograph 'A2'. This set up has been utilised for sand blasting the peripheral damages which occur in alloying and laso used for bevelling the p-n junction at particular angle to avoid premature surface breakdown and to achieve high bulk breakdown voltage. The speed of the wafer, charge quantity, pressure and the angle of contour have been optimised for required purpose to get high breakdown voltage of the transistor.

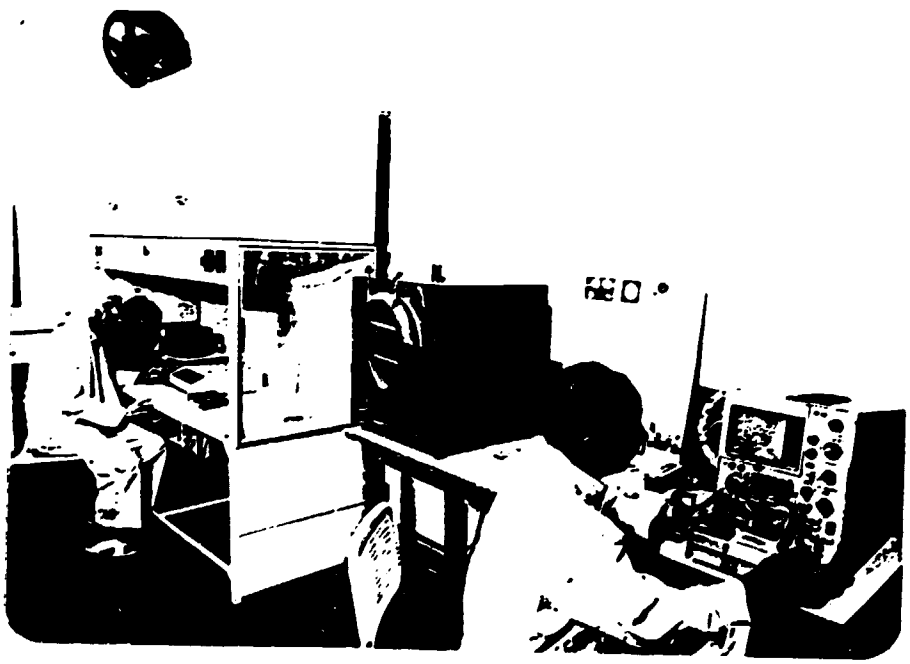
c) Spin Etching of Bevelled Junction:

The bevelled surface of p-n junction has the damaged surface after bevelling and it gives rise to large junction leakage. It is essential to get a damage free and smooth surface to support high breakdown voltage with minimum junction leakage current. In this regard, a spin etching technique has been introduced to chemically etch bevelled surface without deteriorating the metallised E-B regions of the transistor. Spin Etch Set-up is shown in Photograph 'A3' System holds the transistor fusion and rotates it at the required speed and acid jet sprays the chemical to etch the surface. Speed of rotation, flow of etchant, etching angle and time have been optimised for its proper function. The smooth damaged free surface has been obtained which suports the high voltage.

Photograph 'A3' Spin Etching Equipment



Photograph 'A4' Pyrogenic Oxidation System



Photograph 'A5' Measurement Set-up

d) Pyrogenic Oxidation:

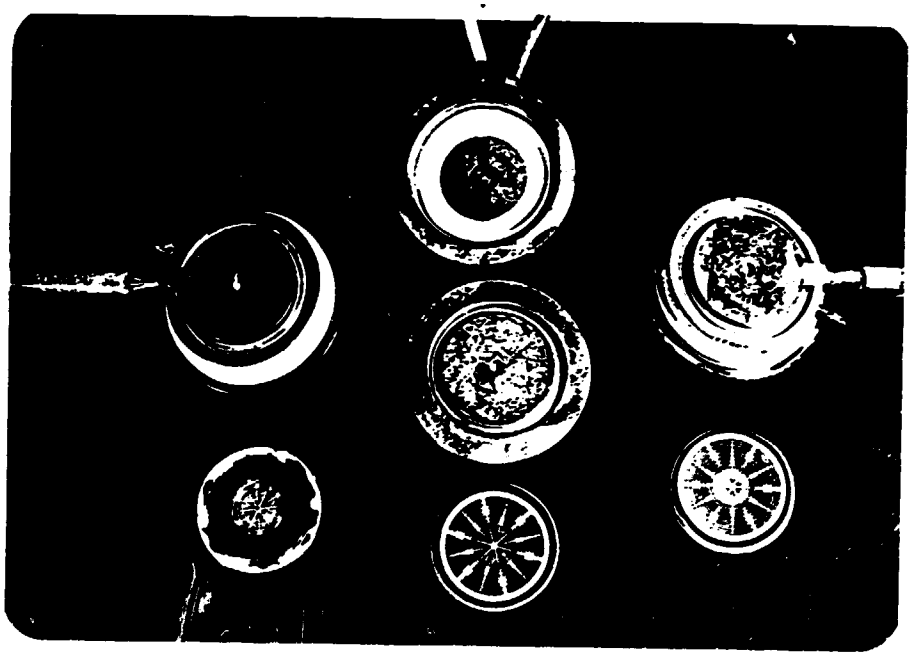
The fabrication of high voltage transistor requires high minority carrier lifetime in p and n base of the transistor. Wet oxidation and thermaltreatments of silicon wafer deterioprates the minority carrier; life time due to heavy metal impurities in D.I. water cleaning chemicals and thermal stresses. Pyrogenic oxidation as a process, used hydrogen and oxygen for steam at high temperature. This process is cleaner and it yields low oxide charge and uniform oxide thickness. Photograph 'A4'shows established pyrogenic oxidation system. For pyrogenic oxidation special hydrogen injection has been fabricated in house at CEERI. It injects H at 700 - 800 C and oxygen at the end of the opening in required ratio so that any explosion in tube can be avoided.

e) Measurement Set up

Measurement set up as shown in Photograph 'A5' has been commissioned to measure breakdown voltages, gain characteristics, V_{CESAT} $V_{}$, $R_{}$, $R_{}$ and switching parameters of the transistor.

VIII. Fabrication Process of 100A and 300A Transistor:

The process developed at CEERI for fabrication of 100A and 300A transistor uses epitaxial wafer non n high breakdown and for low saturation voltage. Transistors have been fabricated using epitaxial double diffusion process. The alloyed fusions are mounted into a compression type package. The developed monolithic Darlington transistor has planar emitter-base; hence Ni-plated molybdenum preform for emitter contact has been introduced. The developed 100A transistor with different stage and its packaged version has been displayed in Photograph 'A6'.

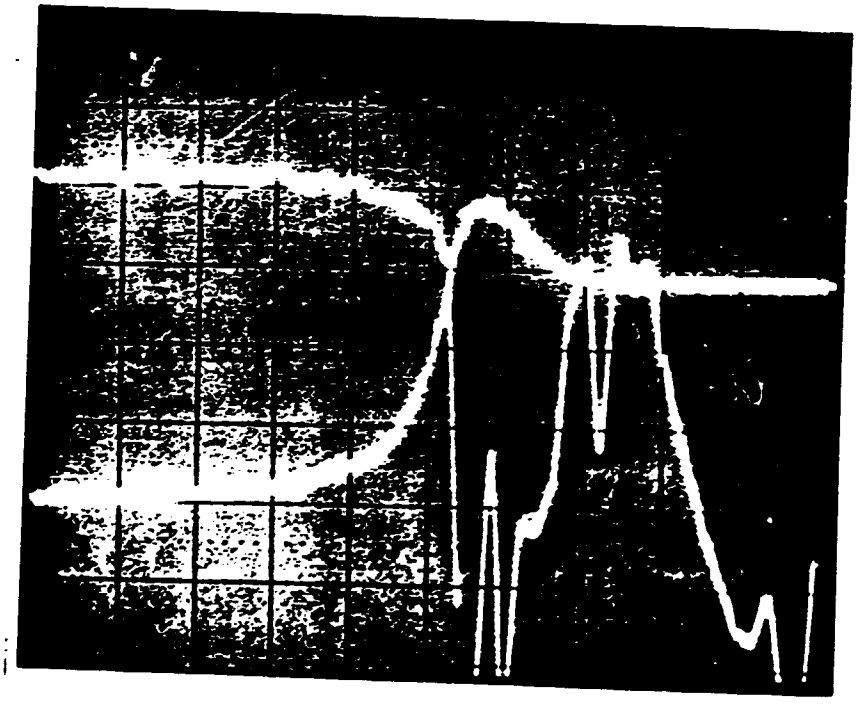


Photograph 'A6' Packaged 100A Transistor
with Different Stages

The 300A monolithic darlington transistor has also been developed but it can be fully tested only after the availability of dual base packages. The fabrication steps involved in their development are shown in Fig. 'A5'.

IX. Test Results and User's Trials

The developed 100A transistor has been checked and the results obtained meet the required specifications for its use in A.C. Motor drives. The transistors have been checked by internal users in the Power Electronics Systems and their results are shown in Table-III. The testing of 100A transistor under inductive load condition has been done. The Photograph A-7 shows the behaviour of I and V during turn-off condition.



PHOTOGRAPH 'A7' Variation of I and V during inductive turn-off.

TABLE-III

TEST RESULTS ON
CEERI DEVELOPED DARLINGTON TRANSISTORS

TEST CONDITIONS

Base Drive Power Supply = ± 8V

Vcc = 150 V

Serial No.	1	2	3	4	5	6	7	8	UNIT
Base-Emitter Resistance	15.0	14.5	16.0	16.8	15.0	16.9	1.6	1.5	ohms
ON CHARACTERISTICS:									
V_{BE} (Sat)	1.4	1.5	1.5	1.3	1.4	1.5	1.35	1.35	Volts
+ve Base Current	1.4	1.4	1.45	1.4	1.4	1.4	1.55	1.60	Amp.
-ve Base Current	0.4	0.45	0.4	0.4	0.5	0.3	>0.5	>0.5	Amp.
Collector Current (Ic) (As which the device is tested)	70	76	70	72	80	70	70	70	Amp.
V_{CE} (sat) at above test current	0.8	0.9	1.1	1.2	1.3	1	1	1.2	Volts.

Sl.No.	1	2	3	4	5	6	7	8	UNIT
SWITCHING CHARACTERISTICS:									
(a) R-L Load (Vcc = 150V, Ic = 70 Amp.)									
Storage time (t_s)	7.0	8.0	7.0	6.5	-	7.5	7.0	8.0	µs
Fall time(t_f)	1.4	1.5	1.5	2.0	-	1.5	1.5	2.0	µs
(b) Resistive Load (Vcc = 50V, Ic = 80 Amp; tested for one device)									
Delay Time (t_d)	0.2								µs
Rise Time (t_r)	0.2								µs
Power Dissipation									
Max.PD Tested, Tc = 120° C	450								Watts

B. MONOLITHIC INTEGRATED CIRCUITS

x) Application Specific Integrated Circuits (ASICs) are rapidly becoming the key microelectronic components in realising any modern electronic system. They provide a compact, low power, high performance, cost effective and reliable alternative to the use of standard SSI and MSI circuits. The °brain' prtion of a modern microprocessor based electronic system can be functionally partitioned into several ASICs including co processor and other components. The ASIC chips and microprocessor software are then developed to realise the system.

xi) In line with the above approach, the following objectives were set for the microelectronics activities under this project.

(a) Design of a VME-Bus compatible controller for multichannel analog data acquisition [here after referred to as chip 1].

(b) Development of 6 micron NMOS process technology and fabrication of chip 1.

(c) Design of a dedicated 16-bit co-processor for the generation of Pulse Width Modulation Pattern of inverter controlled A.C. Motor drives.

(d) Validation of this design through chip fabrication at a suitable foundry and iteration.

A functional block diagram of the system showing the roles of these chips is shown in Fig. B1.

xii) Identification of ASICs :

a) The implementation strategies for Pulse Width Modulation (PWM) control of A.C.Motor drives were jointly examined and debated by system designers and VLSI designers. It emerged from these discussions that there were two distinct sub-tasks for which ASICs could be most gainfully designed.

b) The first of these tasks was the interfacing of analogue feedback signals (such as instantaneous voltage and current, transformed into digital signals) from the motor to the microprocessor. An ASIC for this purpose would simplify system design and significantly reduce the total chip count of the system. It was, therefore, decided to design a VME bus compatible controller chip for multichannel analog data acquisitions (chip 1). It should be noted here that since Motorola 68000 was chosen as the CPU for the system, this VME bus compatible chip was so designed as to be useful to all similar 68000 based micro computer controled systems.

c) The other task was the repetitive, computation intensive, time critical task of calculating modulated pulse widths and generating the PWM signals in real time. Analysis showed that the microprocessor component of the system would spend most of its time doing the above task, and infact, would not be able to cope up with this task beyond a certain switching frequency - thus limiting the range of output frequencies and harmonic purity of the inverter drive.

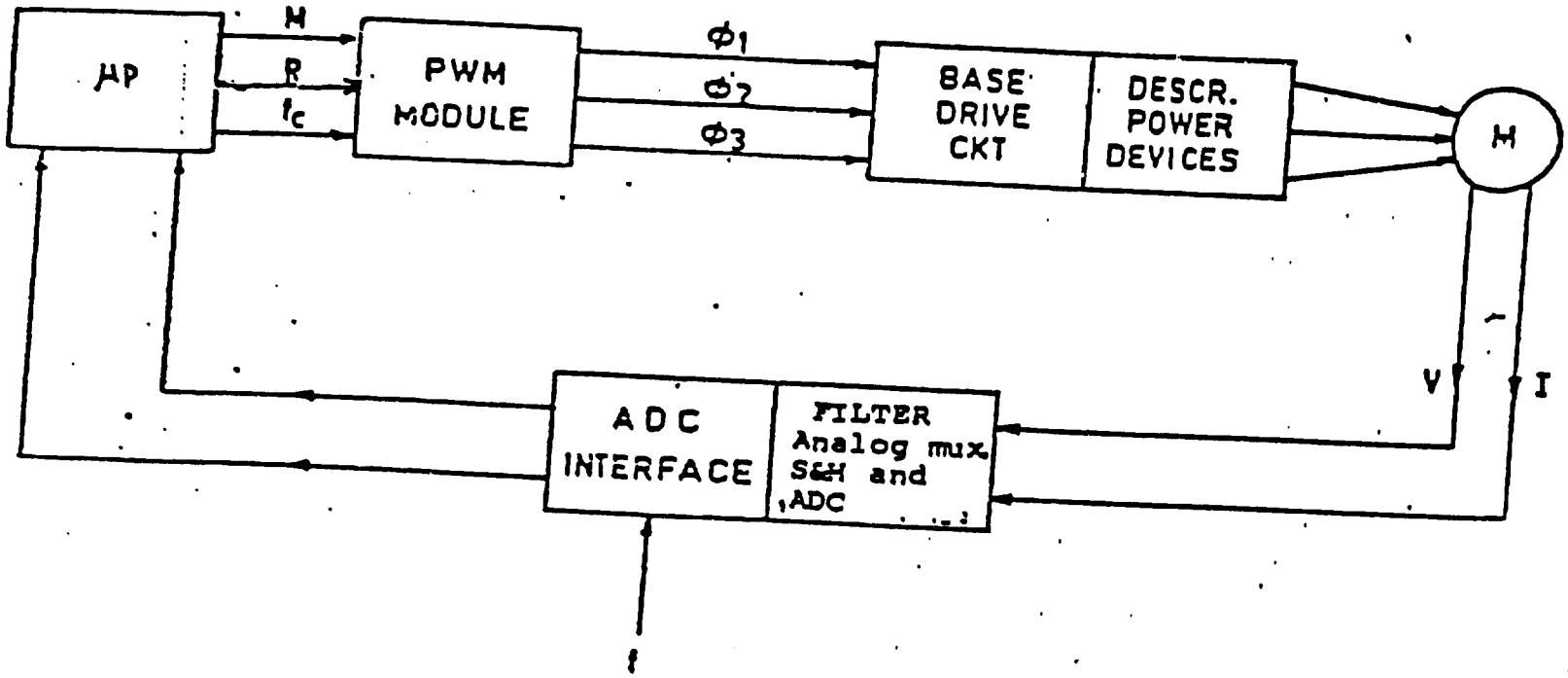

μP
M
R
f_c
PWM MODULE
ϕ_1
ϕ_2
ϕ_3
BASE DRIVE CKT
DESCR. POWER DEVICES
M
~
V
I
ADC INTERFACE
FILTER Analog mux, S&H and ADC
f

FIG. B·1

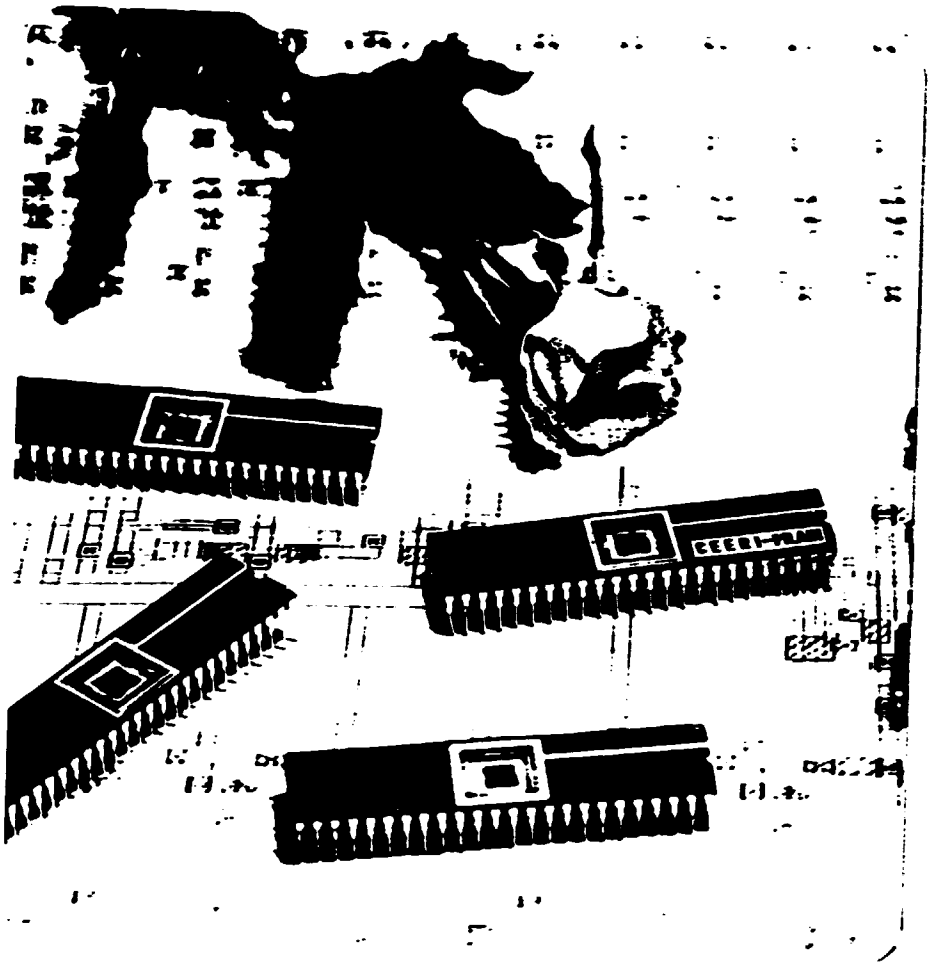
d) It was, therefore, decided to develop a 16-bit PWM processor that would take over this task from the microprocessor relieving the associated frequency constraints from the AC drive and freeing the microprocessor for other system tasks.

xiii) Design

VME bus compatible controller for multi-channel analog data acquisition (Chip 1).

a) This chip was designed by the VLSI design team at CEERI using the Applicon AGS-860 interactive graphics system and the circuit simulator MSINC running on HP-1000 computer. The design was based on CEERI's own inhouse 6 micron NMOS technology rules (design rules).

b) The chip is designed to accept a channel number for analog data acquisition from the microprocessor via the VME bus. It then generates the necessary sequence of control signals for the analog multiplexer, sample and hold circuit, and Analog-to Digital converter to initiate data conversion on the channel. The status of conversion is monitored by the chip and the microprocessor is interrupted when conversion is complete. The chip then identifies itself to the microprocessor during the interrupt acknowledge cycle and then sends over the acquired digital data from the channel to the microprocessor.



Chip No.1 : VME Bus Compatible Controller Chip for Multichannel Analogue Data Acquisition

c) Special pin programmability features permit the chip to control practically any analog multiplexer, sample and hold and Analog-to Digital converter circuits and thus interface them to the microprocessor via the VME bus. Masks for this design were made inhouse by the mask making team using the Electromask - 250 Combo pattern generator and image repeater machine.

d) Chips were also fabricated inhouse using the 6 micron NMOS process technology. Packaged chips were successfully tested against all the design specifications and samples of chips have been made available to the system designers.

e) A detailed technical report on the design is available. The design details were also published in an international journal. A picture of the chip and a summary information on its transistor count, pin count, power consumption, maximum clock speed etc. are given in Fig. B2 and Table BI.

xiv) Design of a dedicated 16-bit PWM Processor (Chip 2 and Chip 3)

a) Based on discussions with the system designers, broad specifications of this chip set were worked out during the consultancy visit of Prof. P. Jespers to CEERI. Since the estimated chip complexity was beyond the capability of Computer Aided Design (CAD) tools and wafer fabrication facilities at CEERI, Prof. Jespers offered the use of CAD tools and wafer fabrication facility at his laboratory - labo. microelectronique, Universite' Catholique de Louvain, Belgium - for the development of these chips.

VME BUS COMPATIBLE ADC CONTROLLER CHIP

(Acts as a multichannel data acquisition controller in VME Bus based systems)

CHIP SIZE 4.3x4.3 mm^2

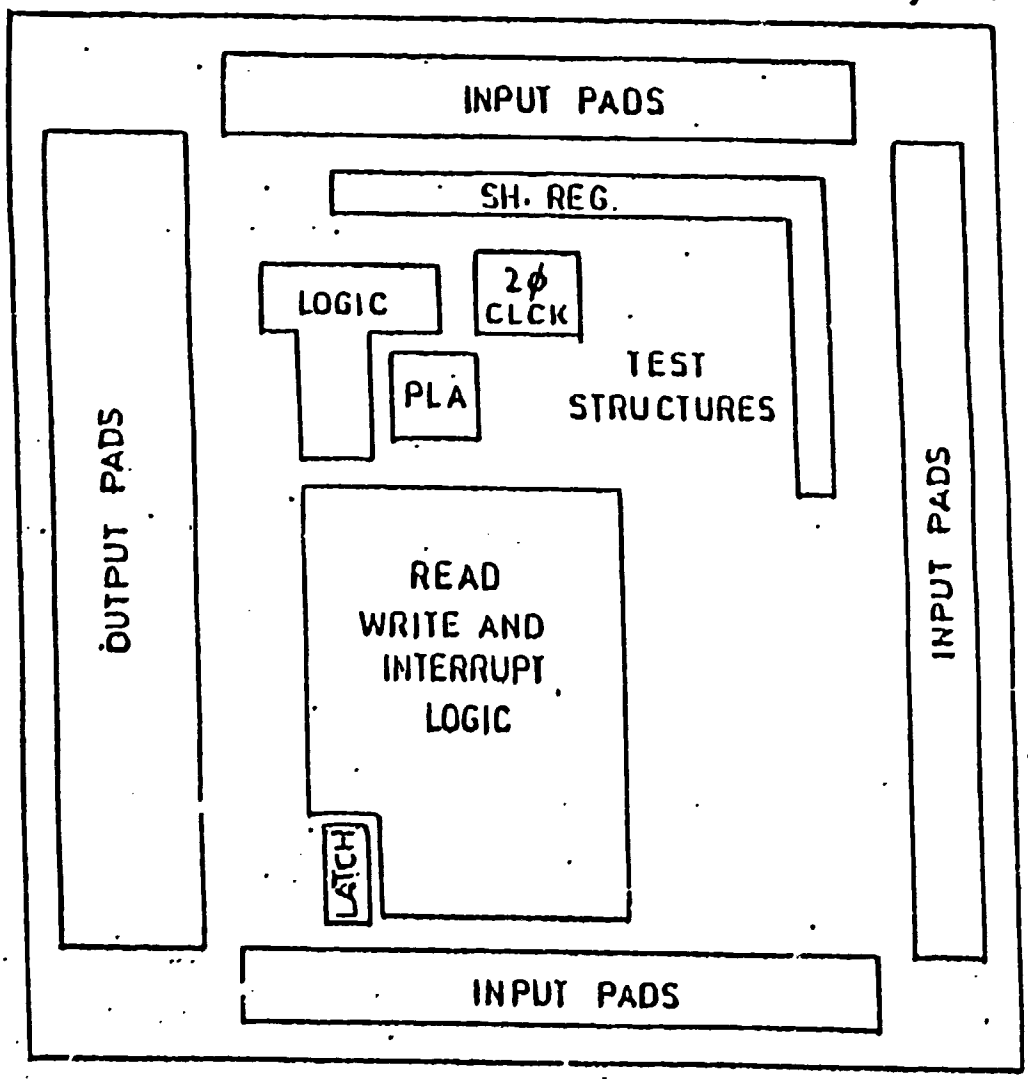
No. of Components - 800

Pin Count - 44

Package - DIP 48 Pin

OPERATIONAL FREQ. - 2 MHz

APPLICATIONS - Industrial Control - Instrumentation & Systems



FLOOR PLAN

FIG.B2.

b) Accordingly, the set of two chips namely the PWM Data Path chip (chip 2) containing about 7500 transistors and the PWM controller chip (chip 3) containing about 3000 transistors which together constitute the dedicated 16-bit PWM processor were designed by a VLSI designer from CEERI during the tenure of his UNDP fellowship at UCL, Belgium.

c) These chips accept the four parameters (namely A.C. output frequency of the inverter, frequency ratio, modulation index, and minimum pulse width for pulse retention) that characterise the PWM signals from the host microprocessor. Using these and the sine function samples from a ROM, the chips execute one million operations per second to compute and generate the three phase PWM signals for inverter control.

d) The PWM processor can handle any of the popular sampling techniques e.g. regular symmetric, regular asymmetric, averaging based and constant area based. It can support output frequencies from 1 Hz to 300 Hz using frequency ratios that are odd multiples of three in the range of 3 to 45.(It may be noted that these limits cover a wide range of applications of PWM AC Motor drives used in Transportation and Industry) The output voltage level of the inverter can be controlled in 128 steps. The processor also handles overmodulation and pulse dropping which are often required to achieve the full voltage capability of the inverter. The processor can control inverters designed with different kinds of switching devices meant for different power levels.

Masks for chip 2 and chip 3 were fabricated by a commercial mask house and chips were fabricated at UCL, Belgium. Packaged devices were tested at CEERI. As no VLSI tester was available at CEERI, special test setups and cards had to be developed to test the chips. This did cause delays in the testing of the chips.

e) Results of testing established the correctness of design of chip 2. However, a defect in the mask (caused during mask handling) had caused malfunctioning of a very small portion (one register) of this chip. It,therefore, became necessary to repeat mask fabrication and chip fabrication for this design.

f) Testing of the PWM controller (chip 3) showed that there was a design error (wrong interconnection in the feed back part of the main finite state machine) in that chip. Redesign of this chip was carried out at CEERI using the Applicon AGS-860 interactive graphics system and a specialised CAD tool (NMOS PLA based silicon compiler for finite state machines) developed at CEERI.

g) Mask fabrication at a commercial mask house and chip fabrication at UCL, Belgium for these chips (chip 2 and chip 3) would be completed by Nov./Dec. 1988. Simultaneously, a mask set for the modified design of chip 3 is presently being fabricated inhouse and its chip fabrication at CEERI would commence shortly.

A detailed technical report on the design of the PWM processor is available. Part of the design details were presented at a technical conference. Block diagram of the PWM data path and controller chips together with their transistor counts, pin counts, maximum frequencies of operation and power consumption etc. are given in Figs.B3 and B4.

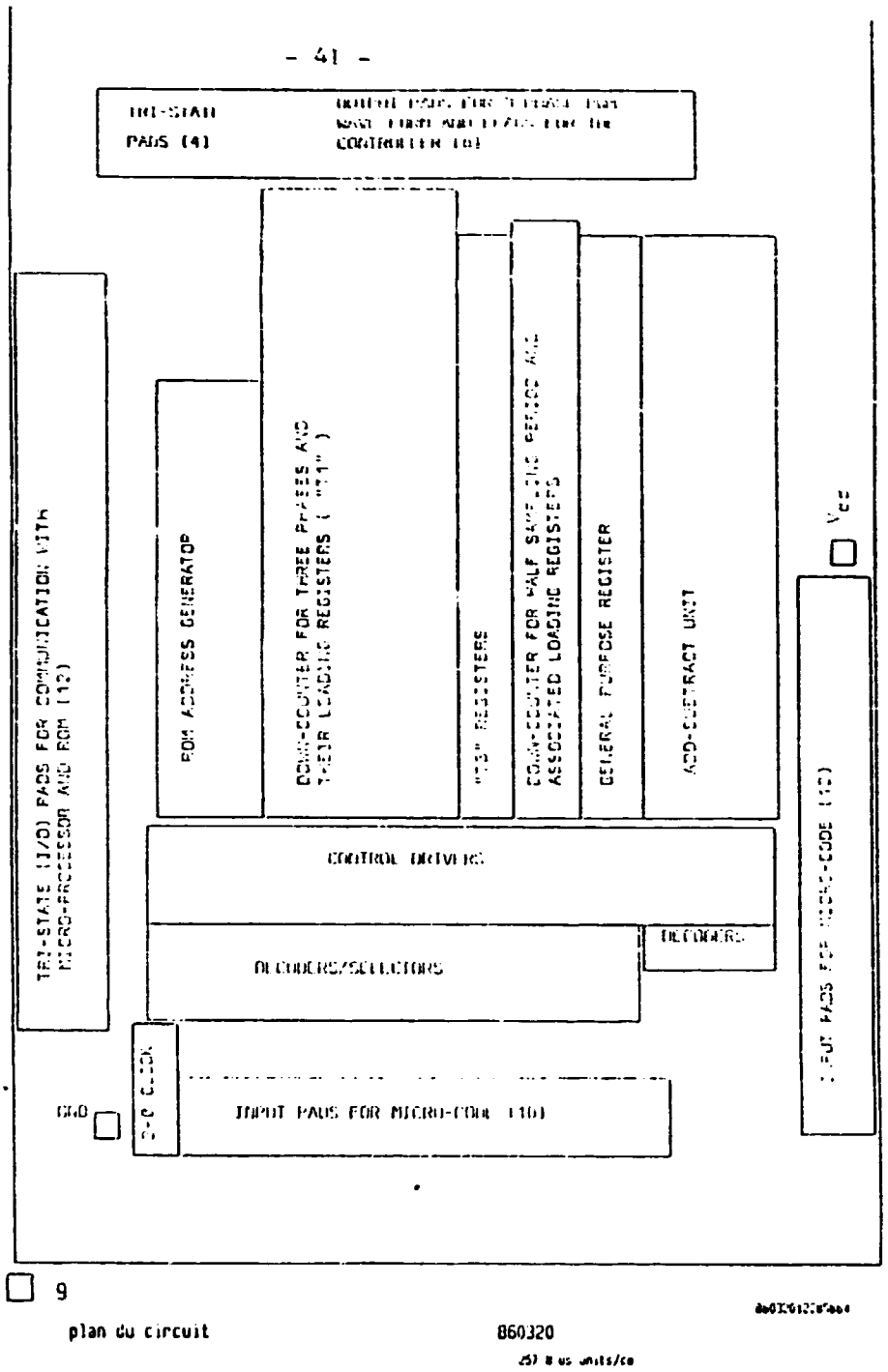
xv) Development of Silicon Gate NMOS Technology

Development of silicon gate NMOS process technology for the fabrication of integrated circuits, was initiated with the help of UNDP experts. The effort was started with the help of test masks designed at CEERI. This set of masks contained the following test structures.

a. Enhancement mode transistors
b. Depletion mode transistors
c. Field transistors
d. Inverters with depletion and enhancement load
e. Ring Oscillators with depletion and enhancement load
f. Step coverage patterns
g. Alignment monitoring structures
h. Structures for different layers
i. Capacitors
j. Contact characterisation structures

The detailed report on these structures was also prepared. The process evaluation using these masks helped to standardise various process parameters. The tolerances on these parameters were determined by collecting statistical data on wafers from

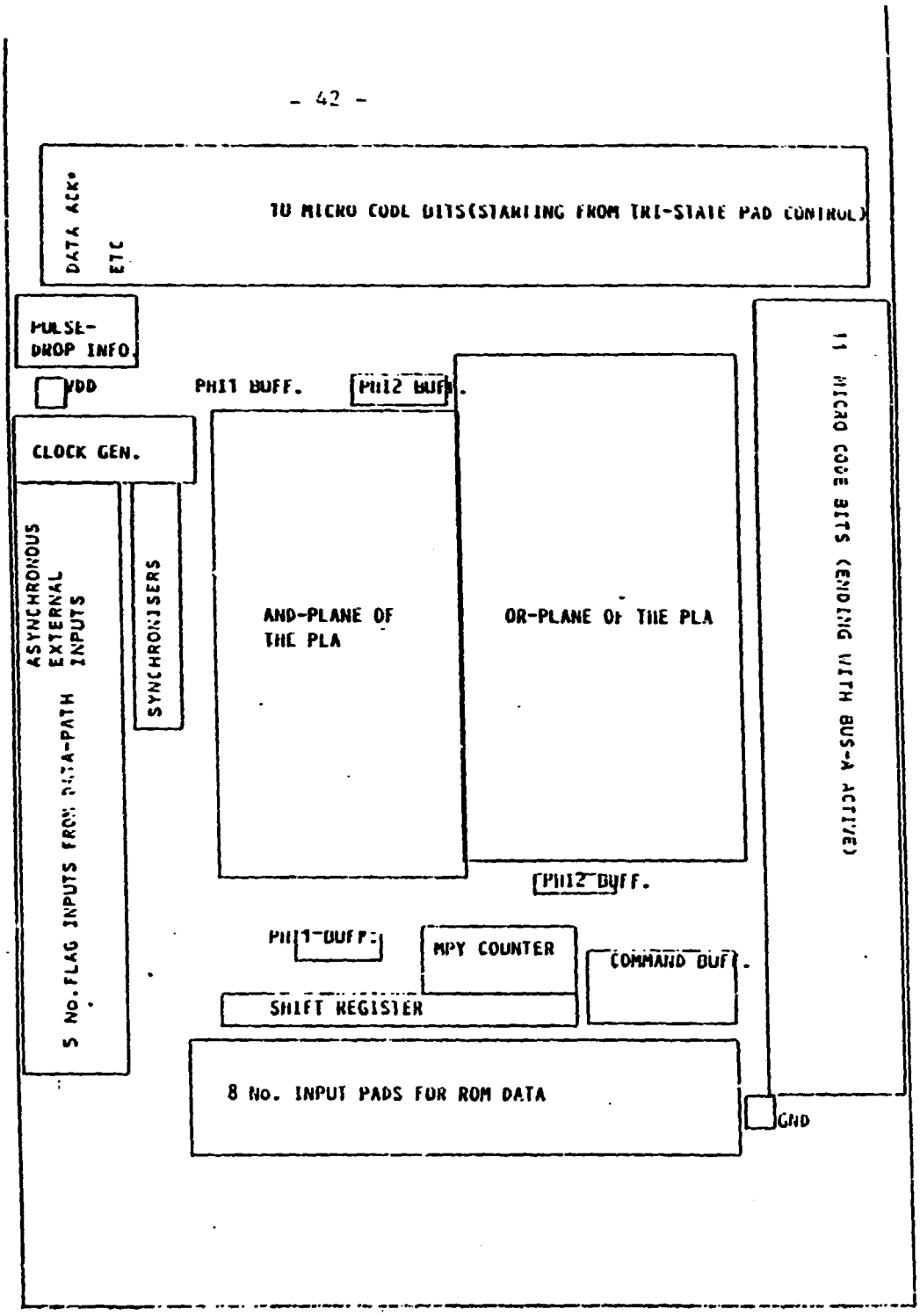
Chip 4: PWM Processor Data Path Chip



plan du circuit 860320

Number of Transistors	**= 7,500 (approx.)**
Chip size	**= 5.2x4.3 mm2**
Power dissipation	**= 270 mW**
Number of Pins	**= 48**
Power Supply	**= 5V**
Technology	**= 6 micron NMOS**
Maximum Colck Frequency	**= 1.5 MHz**

Chip 3 : PWM Processor Controller Chip



Number of Transistors	=	3000 (approx.)
Chip size	=	3.3x3.2 mm^2
Power dissipation	=	120 mW
Number of Pins	=	43
Power Supply	=	5V
Technology	=	6 micron NMOS
Maximum Clock Frequency	=	1.5 MHz

FIG.B4.

different process runs. The design rules were then evolved. These are given in Table C.I. The details of technology developed were published in an international journal (Annexure VIII).

xvi) Chip Fabrication

VME Bus compatible controller chip for multichannel analogue data acquisition, was fabricated using the above mentioned process technology. Various threshold voltage were checked on test devices. The constituent cells of the circuit i.e. PLA, shift register, clock, super buffer, delay element with latches were also tested on the wafer. The good chips were diced out, inspected and encapsulated in 48 lead ceramic dual in line package. Functional testing of the circuit which was later done on the encapsulated chips met all the design specifications.

TABLE B.1

DESIGN RULES

SILICON GATE NMOS TECHNOLOGY

Enhancement threshold	-	1 ± 0.2 V
Depletion threshold	-	-3 to 3.5 V
Field threshold	-	15 - 22 V
Minimum feature size (contact on level 7)	-	6 x 6 micron^2
Minimum diffusion width	-	8 micron
Min. Diff. to Diff. separation	-	8 micron
Minimum poly width	-	8 micron
Min. poly to poly separation	-	8 micron

Min. metal width		-	10 micron
Metal to Metal separation		-	10 micron
Min. Metal to Diffusion separation/overlap		-	2 micron
Min. Metal to poly separation/overlap		-	2 micron
Min Diffusion to poly separation		-	4 micron
Poly overhang in Transistors		-	5 micron
Contact on level 6		-	8 x 8 micron^2
Diffusion/Poly extension around contact (7)		-	4 micron
Metal extension around contact		-	2 micron
Butting contact	a) Level 6	-	16 x 10 micron^2
	b) Level 7	-	12 x 6 micron^2
Diffusion poly overlap for butting contact		-	2 micron
Implant extension around Depletion Transistor areas		-	6 micron
Separation between depletion implant and enhancement transistor		-	6 micron

xvii) Achievements :

1. VME bus compatible controller chip for multichannel analog data acquisition (chip 1) successfully designed, fabricated and tested.
2. Silicon gate NMOS technology successfully developed.
3. Design of the PWM processor's data path chip (chip 2) successfully completed and validated through the testing of fabricated chips.

4. Design of the PWM processor's controller chip (chip 3) debugged through testing of the fabricated chips. Design modifications completed and refabrication initiated.

Chips from the modified designs expected in Nov. - Dec. 1988 would be made available to these users besides in-house users for developing prototype systems.

xviii) Any other Relevant Point :

Based on the design expertise gained through this project, Deptt. of Electronics (Govt. of India) has funded the setting up of a VLSI Design Centre for Industrial ASICs at CEERI. Under this project, Deptt. of Electronics would provide grants to strengthen CAD facilities at CEERI and CEERI will design chips for industrial applications besides software CAD tools. A serial Data Communication Controller Chip for C-DoT is presently being developed besides another in-house chip.

A mutually benefitial bilateral R&D co-operation project has evolved between CEERI and University Catholique de Louvain, Belgium, as a direct result of interaction between these two organisation during the course of the UNDP project details of which have appeared earlier in this report. Under this project, advanced microchips for industrial and Power control applica tions would be developed jointly.

Based on the expertise gained development of Silicon gate NMOS technology and a certain level of infrastructural facilities available at CEERI, Deptt. of Electronics (Govt. of India) has started funding a project on the development of - 'Multilevel Interconnect Technology for VLSI' at CEERI.

C. DEVELOPMENT OF HYBRID CIRCUIT MODULES:

xix) SUMMARY

The increased usage of electronics in Control Systems makes reliability of electronic circuits a major concern. Recognising the importance of Hybrid Micro Circuit(HMC) Technology over PCB technology in terms of reliability, size, performance, weight etc., two different types of Base drive HMCs to drive 100 Amp. transistors & 300 Amp. transistors have been developed. Both these HMCs have met the electrical specifications provided by the Power Electronics Laboratory of the Institute. To accomplish this task computer programmes for resistor design and for calculating hybrid package to junction temperature rise have also been developed and successfully used. Power Resistors and Power conductors were designed, fabricated and evaluated. The data generated by these experiments was used in the design of Power HMCs. As a by-product Power Resistors (3 ohms,15 watts) were fabricated, to help the systems group. These have been used by them in the inverter system.

xx) Design Considerations

a) In any hybrid ciruit design, component attachment techniques, package materials and circuit layout are all significant variables effecting the cost and operation of the finished product. When designing high power hybrid circuits, these variables become even more critical.

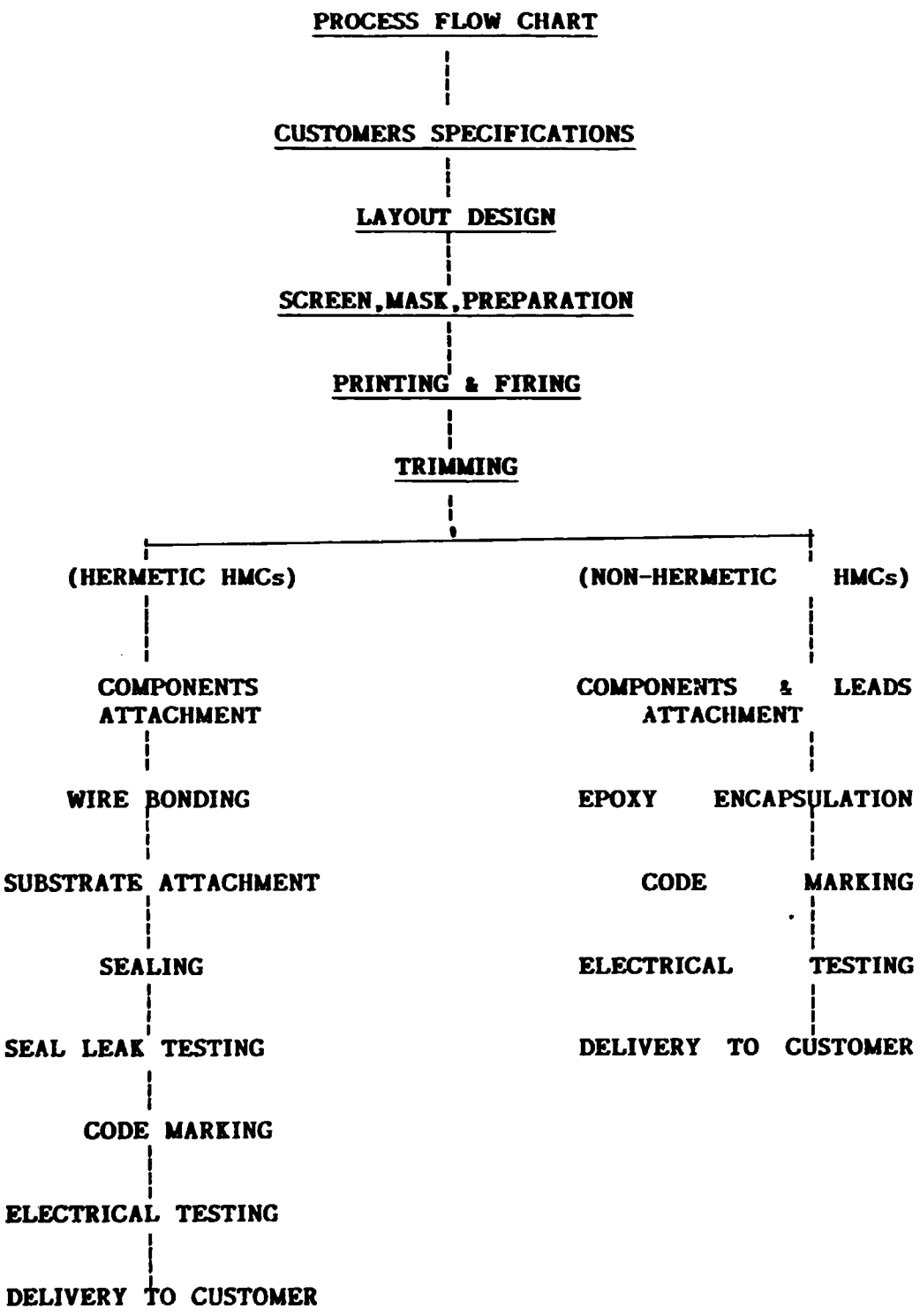

PROCESS FLOW CHART
CUSTOMERS SPECIFICATIONS
LAYOUT DESIGN
SCREEN,MASK,PREPARATION
PRINTING & FIRING
TRIMMING
(HERMETIC HMCs)
(NON-HERMETIC HMCs)
COMPONENTS ATTACHMENT
COMPONENTS & LEADS ATTACHMENT
WIRE BONDING
EPOXY ENCAPSULATION
SUBSTRATE ATTACHMENT
CODE MARKING
SEALING
ELECTRICAL TESTING
SEAL LEAK TESTING
DELIVERY TO CUSTOMER
CODE MARKING
ELECTRICAL TESTING
DELIVERY TO CUSTOMER

FIG.C1

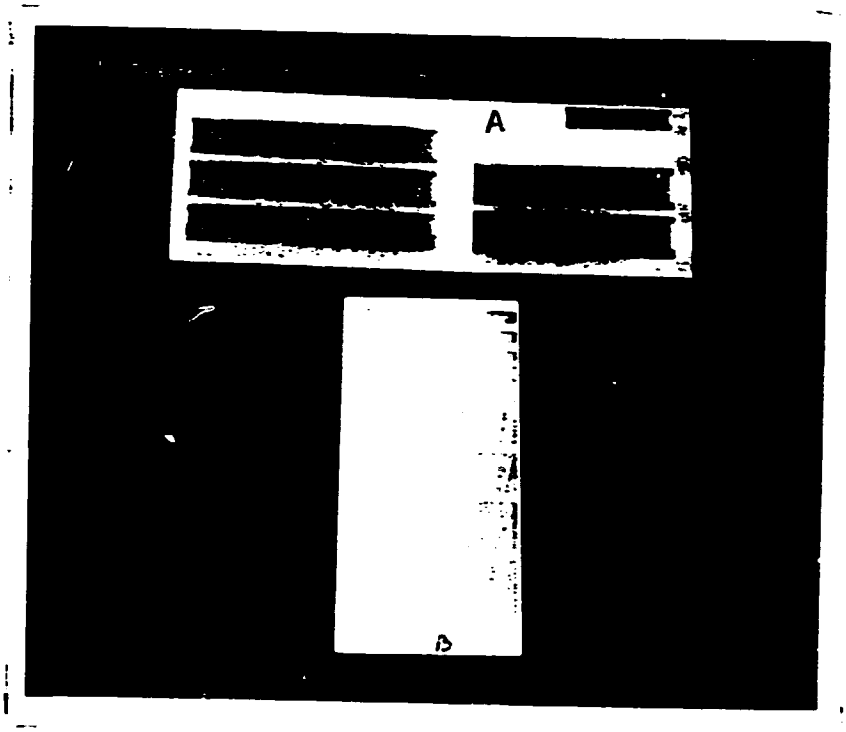


Fig. C2A and C2B

Depending upon the user requirements, materials, components, type of package, process etc. can be selected. For Base Drive circuit, being a power hybrid, alumina substrate, and aluminium and copper packages have been selected.

Before actual design of the layout, study of resistor test pattern and coductor test pattern was carried out.

b) Resistor Test Pattern (Power)

A resistor test pattern (shown in Fig. 2A) having six numbers of resistors (resistance value 1 ohm) was designed and fabricated on 3" x 1" x 0.005" alumina substrate. Measurement were taken on a set of eighteen resistors. Hot temperature coefficient of resistance, Noise index, power handling capacity and thermal storage at 150 C for a period of 2000 hrs were studied. The results are summarised as follows:

1. Hot TCR 50 ppm/ C
2. Noise Index - 7 db
3. % change of resistance after 200 hrs at 150 C - 0.5%
4. Power handling capacity - 100 watt/inch

c) Conductor Test Pattern (Power)

A conductor test pattern (shown in Fig. 2B) having different width 1 mm to 7 mm of Pd/Ag conductor was designed and fabricated on 2" x 1" C 0.025" alumina substrate. Sheet resistance was found to be 25 m ohm/sq. Current capacity of 1 mm line was found to be 1000 ma. In order to increase the current capacity, solder cream was printed on 1 mm line and then reflowed. After reflow of the solder, sheet resistace came down to 2.5 m ohm/sq. It was

further reduced to 1.2 m ohm/sq. by multiple printing & reflowing the solder cream.

xxi) Layout

Considering size of components like transistors, diodes and capacitors, layout pattern was designed on a graph sheet. Resistor dimensions were calculated using a computer program, developed by the group.

In the present HMCs developed at CEERI, add-on components like transistors, diodes, capacitors, and ICs are soldered on thick film pattern. Case of the power transistor being surface mount type, is soldered on to substrate. SIL type leads are clipped on the substrate edge and dip soldered. Then this assembly is mounted on a aluminium and or copper plate using thermally conducting epoxy. Selection of components, leads and package is given in section xxiii.

xxii) Thermal Design

A computer program in PASCAL for computing Hybrid case to junction temperature has been developed. Calculating the hybrid case to junction rise for various transistors and other components actual temperature of the hybrid case can be predicted.

xxiii). Componets & Their Placement technique

Transistors, diodes and ICs are available in semicoductor chip, micro-packaged and normally packaged forms.

For these types of circuits the ideal design is to use surface mounted devices (SMD). Extensive literature survey was done. It was found that all the devices are at present not available in SMD form. Only 10 devices out of 15 devices used in the circuits are commercially available as SMD. The manufacturers/small quantity suppliers were requested to supply them. However, SMD's come in packaged tapes/reels containing 100,500,1000 devices per reel. Hence no one even quoted for them inspite of our several reminders. It was, therefore, decided to use normally packaged and SOT semiconductor components due to their availability. In our design of the HMC, case of high power transistors BD 203,BD 137 and BD 138 was flatly mounted on to Pd/Ag conductor pad using solder material. Their leads were bent in a special manner so that these could be attached to the required pads. While designing the layout, bonding pads of the case of all the transistors were kept away from other circuit elements in order to minimise their heating effects on other components. Other low power components like opto coupler were mounted above the resistors as they do not dissipate any appreciable power. High power resistors were also spaced well in order to avoid their heating effects to other components. All the add-on components (transistors, ICs, diodes and chip capacitors) were soldered in a single reflow cycle, i.e., by printing of solder cream, placement of components and reflow technique.

xxiv). Leads

During design of the HMCs layout, all the input/output and other connection pads were kept in one line so that single in line type of leads could be available to the user for direct soldering of input/output wires.

xxv) Package

Special type of packages were designed and fabricated so that they could meet the environmental conditions, power handling capacity, protection to components integrated on alumina substrate etc. Aluminium and copper materials for packages were selected because of their good thermal conductivity, availability and cost etc. These packages can be rigidly mounted on the desired place with the help of two screws.

Hybrid versions of Base driver circuit for 100 amp. transistor and 300 amp. transistor are shown in Fig. 3. Mechanical and Electrical data of both of these HMCs are given in Annexure 3 & 4.

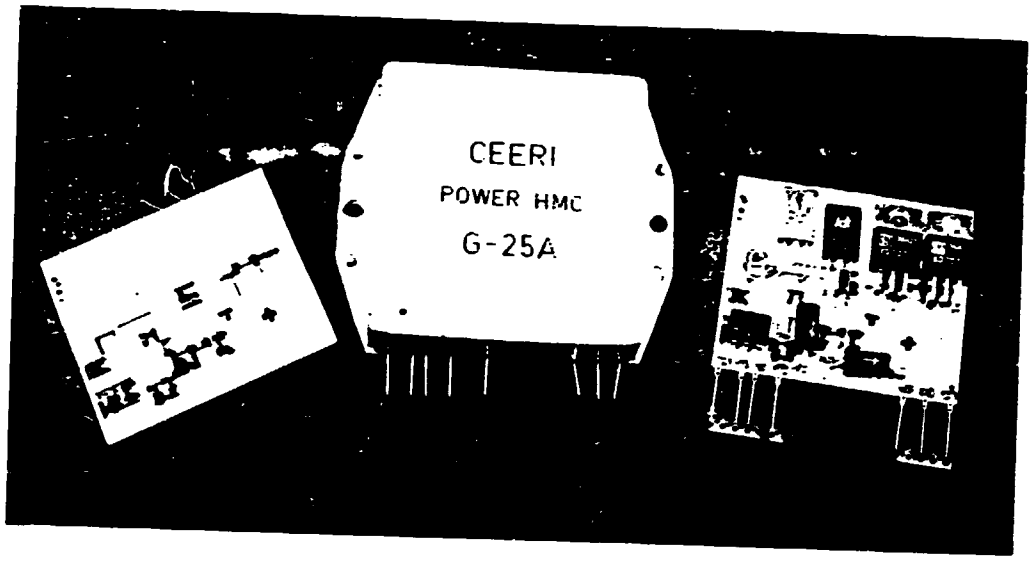


Fig.C3 (A) BASE DRIVE HYBRID MICRO CIRCUIT
(B) THICK FILM SUBTRATE
(C) H.M.C. BEFORE PACKAGING

BASE DRIVE CIRCUIT FOR 300 AMPERE TRANSISTOR

APPLICATION:

- TO DRIVE THE POWER DARLINGTON WITH ISOLATION (UPTO 300 Amp. Transistor)
- SPECIALLY DEVELOPED FOR ELECTRIC VEHICLES.

FEATURES:

- SMALL SIZE AND WEIGHT
- COMPACTNESS
- HIGH RELIABILITY
- GOOD HEAT TRANSFER
- EASY MOUNTING
- CIRCUIT SECRECY

SPECIFICATIONS:

(A) Electrical:

(1) OPERATING VOLTAGE ± 8V
(2) OUTPUT POWER 20 WATT (Approx.)

(B) Mechanical:

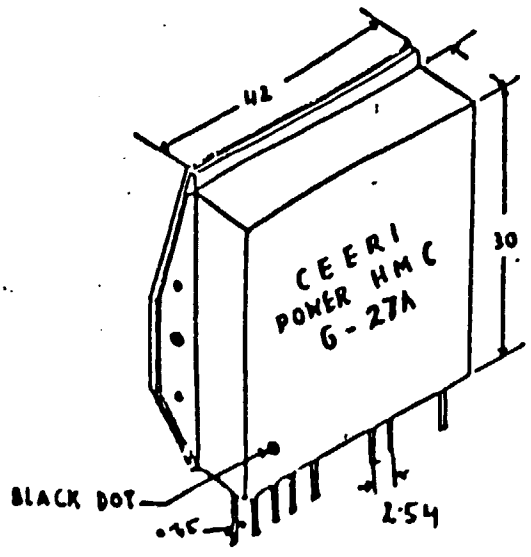


Fig. C4

High Power Resistors for Inverter

D. DEVELOPMENT OF SOLID STATE AC MOTOR DRIVE AND SYSTEM PACKAGES

xxvi) Objective

The main objective of the project is to promote the utilization of power electronics systems for decreasing the production costs and increasing the operational efficiency of electric vehicle drives. This objective has gained further importance due to the recent crisis and price rise in fossil fuels. Electronic control systems for future electric vehicles will be mostly based on either AC motor control with inverters or DC motor control with choppers. Although the modern DC traction motor has been developed to a high degree of sophistications; the AC motor offers many advantages, particularly for battery operated vehicles.

xxvii) CEERI Power Electronics Group, therefore, identified the "development of an efficient AC Induction motor drive for transportation applications" as the immediate project aim.

This was subdivided into following main tasks:

(a) Study and analysis of Pulse Width Modulated (PWM) signal/waveform with respect to losses in motor due to harmonic contents and switching losses in inverter.

(b) Design and development of Microprocessor based PWM logic and control system.

(c) Study of various feed back control schemes to select suitable control strategy for electric vehicles.

(d) Design and development of Microprocessor based feedback control system.

(e) Design and development of 20 KVA Transistor inverter using 300 Amp. transistors.

(f) Testing of 20 KVA transistor inverter with microprocessor based PWM logic.

(g) Testing of 20 KVA transistor inverter alongwith microprocessor based PWM logic, feedback control system and motor as AC motor drive.

(h) Simulation of Inverter driven induction motor for adaptive control applications.

xxviii) Design & Development

(i) Detailed theoretical analysis on harmonic distortion for the following PWM techniques was completed so as to choose the best PWM technique which gives minimum lower order harmonics.

(a) Natural sampling technique

(b) Symmetric regular sampling technique

(c) Asymmetric regular sampling technique

(d) Modified asymmetric regular sampling technique (suggested by CEERI)

(e) Area method (suggested by CEERI)

(f) Modified area method (suggested by CEERI).

Measurement of harmonic distortion was carried out on 40 KVA PWM inverter (please see photograph) in order to support the theory with practical observations.

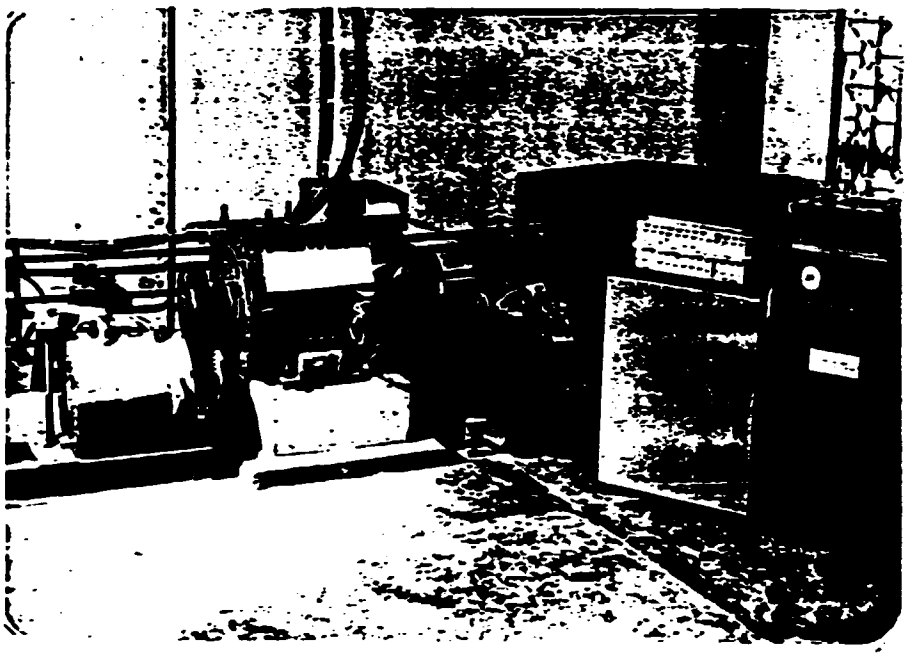


Fig.D.1 - 40 KVA PWM Inverter for AC Motor Drive

(j) A general purpose microprocessor based pulse width modulated logic was designed and developed. The speciality of this microprocessor based system is its flexibility to handle the following PWM techniques with suitable (minor) changes in the software :

(a) Symmetric regular sampling

(b) Asymmetric regular sampling

(c) Modified asymmetric regular sampling

(d) Area method, and

(e) Modified area method.

xxix) In order to achieve the required torque speed characteristics of induction motor to suit transportation applications necessary feedback control is needed. A detailed study of various feedback control schemes was undertaken. Two new feedback control techniques namely "Air gap flux control using reactive power measurement" and "Rotor Slot Method" were developed. The first technique is implemented using 68000 microprocessor in the present AC motor drive developed under UNDP.

xxx) The inverter controls the power supplied to the load by using the logic signals generated by PWM control logic using 300 Amp. transistors. A transistor inverter as shown in photograph 2 as switches with following special features was designed, developed and tested:

(a) Compact fabrication to minimise lead inductances

(b) Use of switched mode power supplies (SMPS) for logic and base drive circuits to improve the efficiency and decrease the size.

(c) Base drive circuits with interlocking facility to protect from 'shoot through' in the inverter.

(d) Use of non-inductive shunt to measure the dc input current for protection.

xxxi) The transistor inverter using 100 Amp. transistors was tested at 50 Hz in six step mode and Table-1 shows the observations regarding the power handling capacity of the inverter.

xxxii) The transistor inverter using 300 Amps transistors was tested and Table-2 shows the observations from 10 Hz to 30 Hz with microprocessor based PWM logic in open loop condition. 30 Hz is

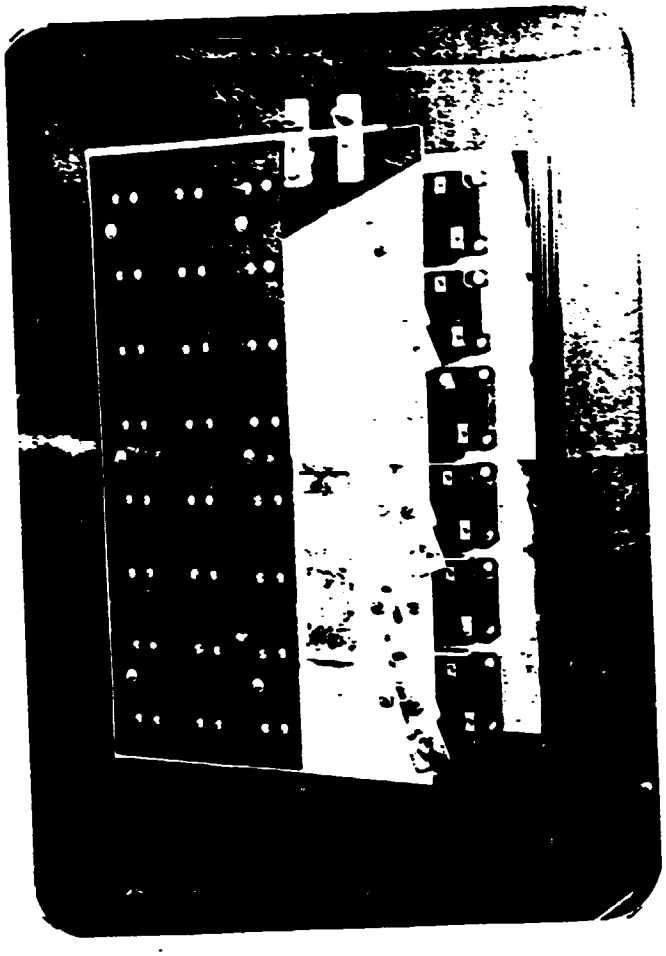


Fig. D.2 - AMP Transistor Inverter

the base frequency of the AC drive where maximum power is consumed. Photograph 3 shows the complete test setup of the AC motor drive with microprocessor based PWM logic, feedback logic, transistor inverter and motor.

TABLE - 1

S.N.	Vdc	Idc	freq.	RPM	VAC (RMS)	IAC (RMS)	VDC	IDC
1.	100V	15A	10 Hz	277	11.2V	41.00A	24 V	8A
2.	100V	30A	15 Hz	415	17.1V	58.75A	40 V	24 A
3.	100V	50A	20 Hz	553	23.2V	76.25A	55 V	33 A
4.	100V	72A	25 Hz	686	29.3V	98.75A	70 V	42 A
5.	100V	90A	30 Hz	850	42.6V	75.00A	80 V	50 A

TABLE - 2

Frequency = 50Hz

Edc(v)	Idc(a)	Pdc(w)	VAC(v)	IAC(A)	PAC Motor VA	Slip	VG(v)	IG(A)	PG(W)
80	20	1600	67	25	2901	0.49	0	0	0
80	30	2400	67	29.25	3395	0.603	30	20	600
80	180	14400	62.4	120	12969	2.38	120	60	7800
100	254	25400	77.5	165.25	2215	2.54	180V	61	11078

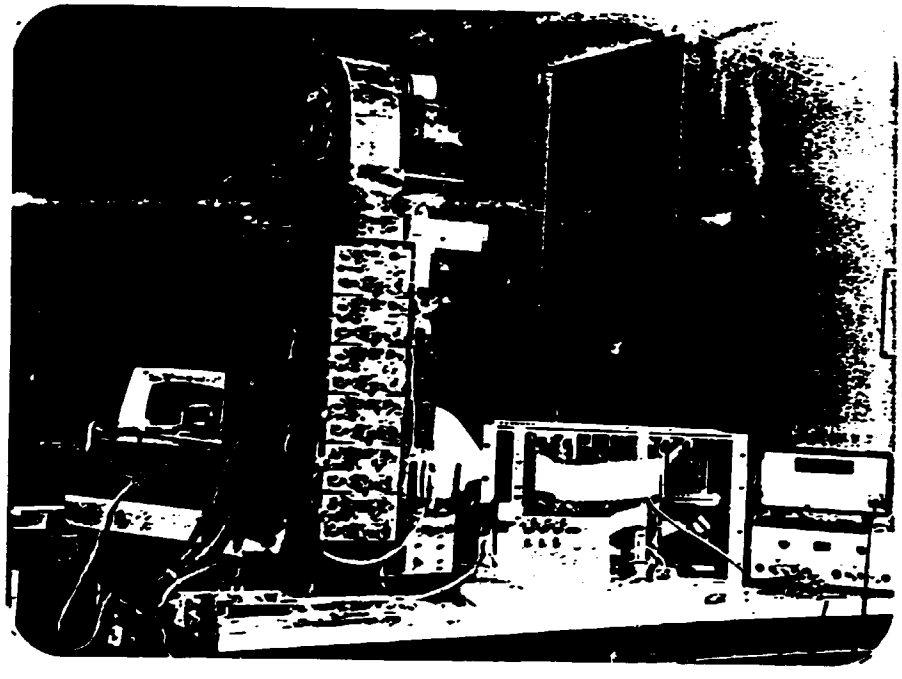


Fig.D.3 - Total Test Set up for 300 Amp. Transistor Inverter

xxxiii) The transistor inverter using 300 Amp. transistors with microprocessor based PWM logic and feedback control logic is presently under test.

xxxiv) The activity on simulation of inverter fed induction motor was carried out at University of Wisconsin and results were used in developing the PWM transistor inverter.

xxxv) The following activities were undertaken to provide necessary design inputs to the semiconductor device group.

(a) complete specifications were prepared for three VLSI chips namely "VME BUS COMPATIBLE CHIP",(Chip 1), "PWM Chip 2" and "PWM Chip 3" in consultation with VLSI group.

(b) Two base drive circuits one for 100 Amp.and other for 300 Amp.transistors was designed and developed. The designs were provided to Hybrid microcircuits group for fabrication.

(c) Tested a batch of 100 Amps.transistors, developed by CEERI alongwith CEERI HMC group developed base drive circuit. Fig. 4 shows the test set up for the same.

(d) Preliminary testing of PWM 1 and 2 chips and VME bus compatible chip, was completed.

(e) Design and fabrication of ADC card using VME bus compatible chip is in progress.

(f) Tested Hybrid base drive circuits for 100 Amp.and 300 Amp.transistors.

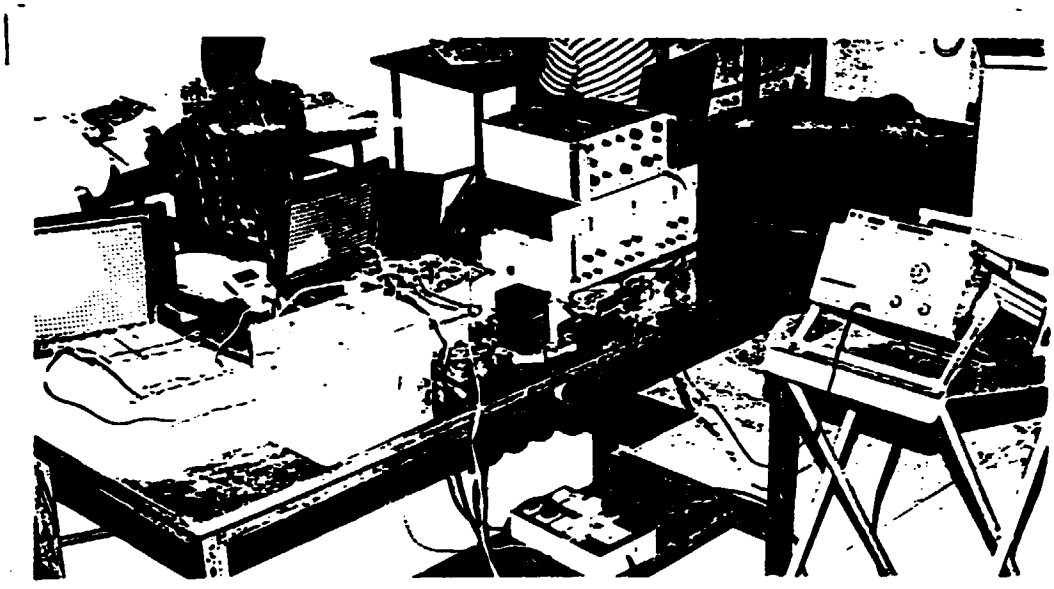


Fig. D.4 - Test Set Up for CEERI Made Transistor

xxxvi) MAJOR ACHIEVEMENTS

The objective mentioned in the section 2 are achieved. The other hard and soft outputs are as follows:

xxxvii) OUTPUTS

A total system package for 20 KVA transistor inverter suitable for transportation applications consisting of the following modules was developed.

(a) A system package for microprocessor based pulse width modulation (PWM) logic.

(b) A system package for microprocessor based feedback logic

(c) 20 KVA transistor inverter using 300 Amp.transistors (photograph 2)

(d) Improved model of 300 Amp. transistor inverter, partially engineered (photograph 5)

(e) Prototype model of transistor inverter using CEERI 100 Amp.transistors (Photograph 6).

(f) A single phase to three phase converter was developed using 100 AMp. power transistor (CEERI make) to use with irrigation pumps for rural applications.

(g) 300 watt. SMPS (Switched Mod. Power Supply) with 24 V DC (Battery) input for material movement application in industry.

Established the basic infrastructure and facilities to undertake power electronics project upto 200 KVA power level.

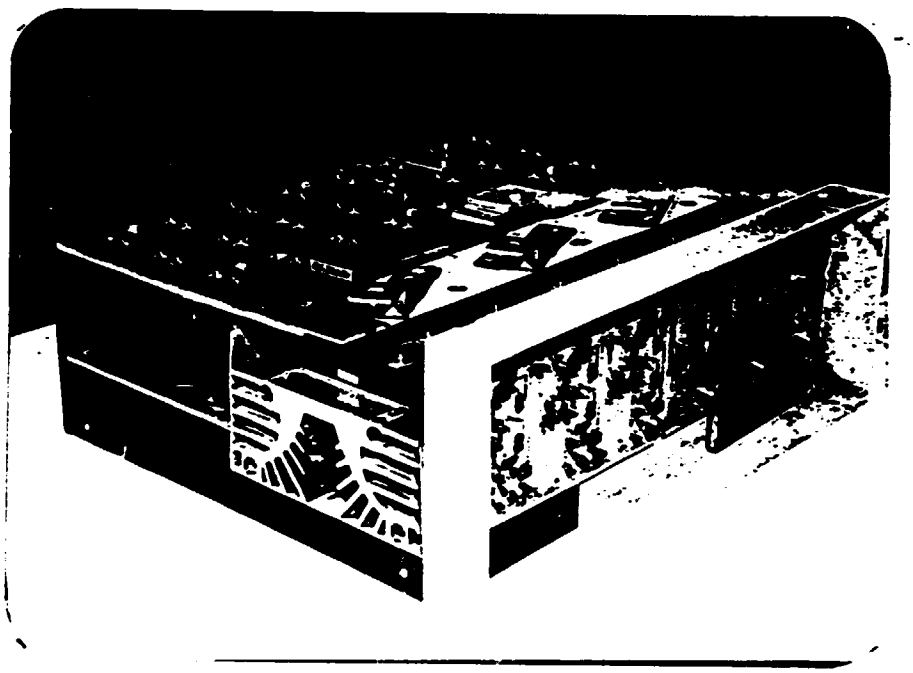


Fig.D.5 - 300 Amp Transistor Inverter : Engineering Model

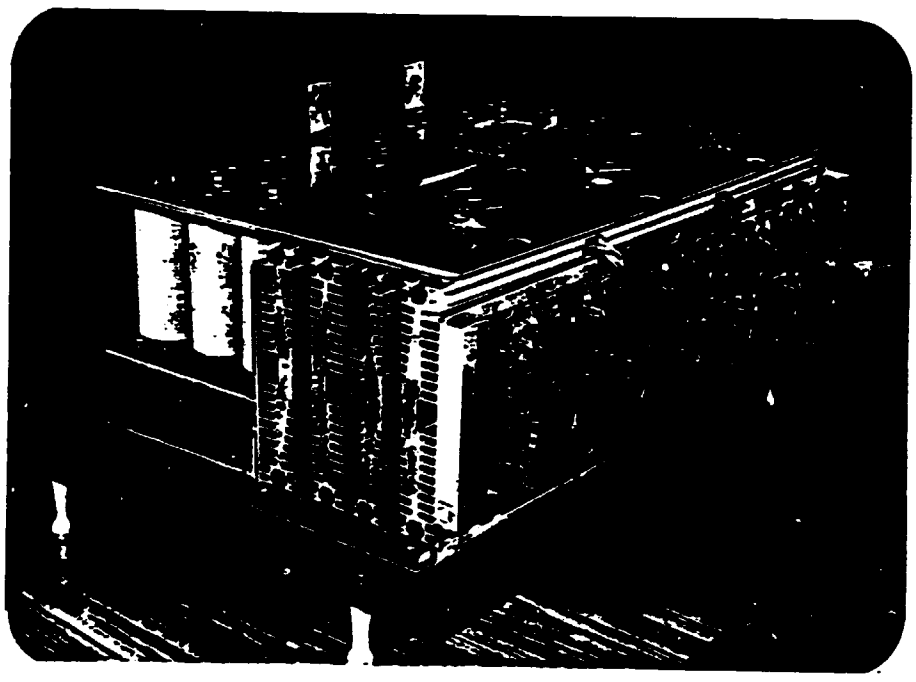


Fig. D.6 - CEERI, 100 Amp Transistor Inverter

xxxviii) Bottlenecks faced and remedial measures taken:

a) The main problem was of procurement of components in time especially the power transistors. This was solved with the help of UNDP experts, consultants and their contacts but the transistors indented through UNDP could not be procured till date. Only a few pieces were received by end of 1987.

b) The second main problem was the operation of inverter on full voltage. This was initially not possible due to voltage spike at the collector of the transistor due to stray inductances. This problem was solved by employing a new approach to fabricate the power module.

c) A need for the protection of the power devices of inverters under abnormal condition was felt. A simple and cheaper non-inductive shunt (fabricated in CEERI) is used to measure the d.c. input current for the protection of the system.

16. From the foregoing it is seen that the outputs as listed in the project document have been completed execpt a few which are likely to be completed in the near future. The delay has been due to external factors as mentioned in the previous paragraphs.

The details of these out puts is as given below:

(i) Batches of Power transistors for power control in electric drives for transportation.

a) Darlington Transistor 100 Amp.

A batch of about 17 Nos. of 100 Amps. Darlington transistors have been delivered to the systems group. These transistors meet the specifications required for the Transportation applications, particularly low power inverter drives. These transistors have been used in CEERI make Inverter to drive A.C.motor. These devices have successfully worked for Single Phase and Three Phase A.C. drive system.

On account of this successful achievement BHEL have rdered for large No. of Darlington Transistors to be used by BHEL, Bhopal.

b) Darlington Transistor 300 Amps.

The design for this transistor have been completed and P.G. tape is ready. Further processing is in progress.

(ii) Batches of custom design Monolithic integrated circuits for PWM drives for use in transportation.

a) Chip No. 1 : VME Bus compatible controller chip for Multichannel analogue data acquisition, successfully designed and tested 12 Pieces have been fabricated.

b) Chip No. 2 : Design of the PWM processor data path chip successfully completed and validated through the testing of fabricated chips.

c) Chip No. 3 : Design of the PWM processor controller chip debugged through testing of the fabricated chip. Design modifications completed and refabrication initiated.

In the original project document only design and fabrication of a batch of chip 1 was envisaged. After the visit of Prof. Jespers from UCL Belgium, the design of more complex chips (chip 2 - 7500 components and chip 3 3000 components) were thought of as Professor Jespers agreed to provide CAD and chip fabrication facilities.

Chip 2 had a fault in the mask fabrication and chip 3 had design fault. These faults have been rectified. The processing is being done in Belgium for chip 2 & 3 and also simultaneously for chip 3 at Pilani. It is hoped that by Nov/Dec 1988 the good fabricated chips would become available.

One batch of fabricated wafers from UCL, Belgium for the PWM data path and the modified PWM controller design have been received. The design modification was

achieved during the UNDP fellowship training of Dr. Mrs. Srivastava and the wafer fabrication was achieved durin g the UNDP fellowship training of Dr. V.K.Dwivedi.

The parameter and functional testing on the wafers is to be completed.

A batch of modified PWM controller design whose masks were made inhouse at CEERI is at the final stages of fabrication at CEERI. Resulting chips will be tested along with the chips received from UCL, Belgium.

iii) Batches of hybrid Integrated Modules for control of Electric drive for transportation.

Base drive circuit for 100 Amp.(5 pieces) and 300 Amp.(11 pieces) transistor have been developed. Both these circuits have been tested by the system group and meet the specifications. These circuits have been delivered in batches of circuits.

iv) Prototype of solid state AC drive and system modules for transportation applications.

A prototype of 20 KVA transistor inverter using 300A transistor has been designed, fabricated and tested.

v) Technical report on the development of 100 Amp Darlington Transistor.

Completed.

b) Technical report on the development of 300 Amp. Darlington transistor

under preparation

c) MoS IC development.

i) Report for the design and development of chip 1

Completed

ii) Report for the design and development of chip 2 & 3.

Completed.

d) Report on Hybrid Integrated Module Development.

Completed.

e) Technical report on development of 40 KVA AC drive.

Completed

f) Technical report on development of 300 Amp. transistor inverter.

Completed.

vi) Video tapes of lectures (15 Nos.)

Ready.

Conclusions

Outputs as envisaged in the project documents have been achieved except the fabrication of 300 Amp. transistor which is in progress. Additional outputs, i.e., fabrication of chip-2 and Chip-3 were fabricated and there are being reprocessed at UCL Belgium and are likely to be completed by Nov./Dec. 1988.

Taking note of the above it can be stated that about 90% of the envisaged outputs have been completed and further additional outputs Chip-2 and Chip-3, are at the advanced stage of de very.

IV. ACHIEVEMENT OF OBJECTIVES

17. The Power Transistors are being manufactured by a few companies, in the world. These companies are selling system modules and not the transistors. And under such situation the development of capability for the development and manufacture of Power Transistors has been well recognised by leading manufactures of systems in India (BHEL) and planners. BHEL provided excellent facilities, almost all required to package the 100 Amp. transistor. The developed device has met all specifications and passed reliability tests as desired by System Group. BHEL Bangalore and Bhopal have matched the progress towards this direction. Now BHEL Bhopal has already orered for large number of transistors, match would be produced at BHEL Bangalore, with the consultancy of CEERI.

18. The approach of the project to develop Application Specific Integrated Circuits (ASICs) for performing the brain functions of the systems have been accepted world wide and the production of ASICs is increasing in the world market. In India the largest manufacturer of Integrated Circuits, the Semiconductor Complex Limited has also oriented its production program for the development & manufacture of ASICs.

19. The Hybrid Circuits are known for their reliability and the manufacturers of systems have started using them in larger numbers. A number of companies have started manufacturing Hybrid Circuits in India. One of them M/s Minicircuits Pvt. Ltd., Bangalore has been set up in collaboration with CEERI. A couple of more companies are contemplating know-how from this Institute.

20. There is now complete awareness that the Electronics Systems using AC Drives for transportation are cheaper, efficient and reliable. These systems reduce the consumption of energy and are well suited for fast energy sources depicting situations and reduction in environmental polution.

V. UTILIZATION OF PROJECT RESULTS

(1) Power Transistors

21. The expertised developed in the project has been used to design and develop fast switching Power Thyristor for BHEL. Specifications 1700V, 1300A, with 40 microsecond switching tune.

22. The interaction with BHEL has been developed to such an extent that the development of transistors (wafer processing and packaging) has been done at BHEL, almost free of cost.

23. The silicon gate NMOS technology developed, has been used to fabricate other circuits (e.g. a custom chip for microprocessor controlled 32-line PABX).

24. Samples of the VME-bus compatible controller chip for multichannel analog data acquisition have been given to in-house system designers for building prototype systems.

A dialogue has been initiated with SCL, Chandigarh for assessing the possibility of their productionising this design or a CMOS version of it at Chandigarh.

25. Two industrial units (BHEL, L&T) as well as some academic organisations have shown interest and requested for the samples of the PWM processor chips.

(2) Hybrid Microcircuits

26. One factory M/s. Minicircuits Private Limited, Bangalore has been setup with the know-how and consultancy from CEERI. This

factory is likely to achieve a turnover of Rs. 20 million during this financial year.

27. Indian Space Research Organization(ISRO) has recognised CEERI as the only supplier of space qualified Hybrid Microcircuits.

(3) Electronic Systems

28. The system group developed a prototype transistorised power supply system for ICED LIN REFRIGERATOR (ILR) to be used in Immunization Programme under National Health Programme supported by WHO, using the inverter fabrication techniques developed during UNDP Programme.

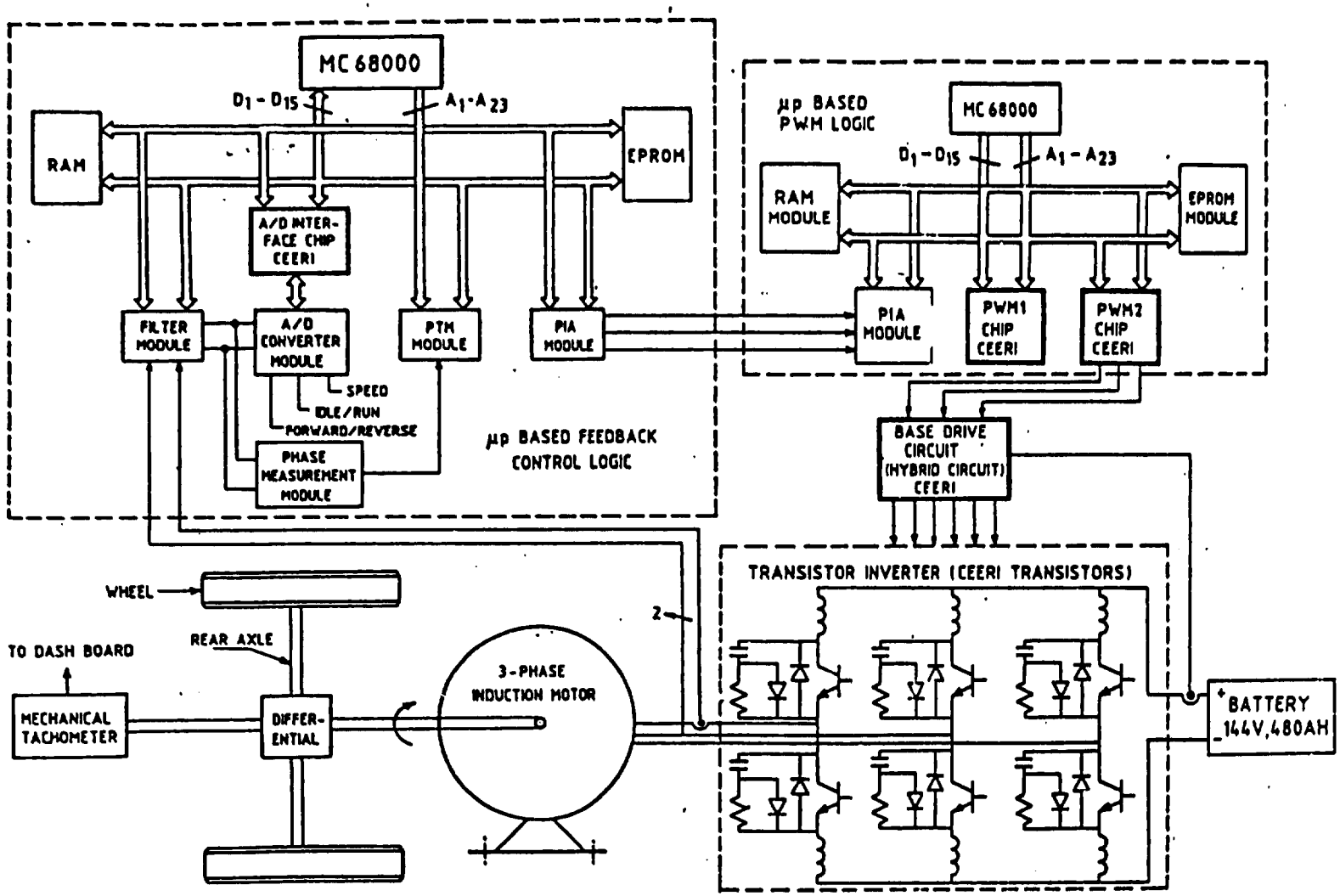
29. BHEL has recently shown interest in utilizing the Know-how of 20 KVA transistorised inverter developed by CEERI under UNDP project for their electric vehicle programme.

30. Considering the expertise gained and capability developed by CEERI under UNDP project, CSIR is proposing to design and develop "SOLAR POWERED CAR" which will use most of the UNDP project outputs directly or indirectly.

30A. The 40 KVA PWM Inverter for Mining Locomotive has been identified by BHEL.

VI. FINDINGS

31. The supply of Power Transistors from International market is becoming more and more difficult. The International Industrial Houses intends to sell more and more of systems or system modules. The project has demonstrated that the Power Transistors can be designed and developed in the country. Adequate resources may be put in, to make the availability of these devices



PROPOSED CONFIGURATION OF THE MICROPROCESSOR BASED A.C MOTOR DRIVE SYSTEM FOR BATTERY POWERED ELECTRIC VEHICLE FIG VA

commercially in the country. Otherwise the manufacture of the systems based on these devices will have to be discontinued or the production programme will be controlled by the supplies from abroad.

32. More and more Integrated Electronic Systems using Application Specific Integrated Circuits (ASICs) for signal processing and control functions are appearing on the World market. The revolution is taking place all over the world and all the major Industrial Houses in the world have started using ASICs in their equipment and systems and future would clearly see systems on microchips performing a variety of logic control functions and higher level of intelligence leading to new area of Artificial Intelligence and Expert Systems. The market for ASICs is growing world wide at a much faster rate and it is expected that by 1995 ASICs will have the 90% share of the Integrated Circuit market of the world.

b) It is high time that India orients its efforts in the development and manufacture of ASICs, through setting up prototype fabrication centres to give a fair trial to the VLSI designs (ASICs).

The wafer fabrication facility at CEERI be upgraded to finer geometries (2-1 micron) and switch over be made to CMOs technology that has now emerged as leading technology.

c) The experience gained clearly indicate the need for an in house chip prototyping facility for carrying out design iterations, and evolving chip designs, for limited fabrication. A validated design with demonstrated use in prototype and system has for

greater chances of being productionised.

d) Strengthening of CAD and testing facilities is also very essential.

33. There is need for a national mask fabrication and inspection facility to be run on commercial lines as per standard practices abroad.

34. The capability created for development of electronic systems can be directed to develop efficient AC drives using smart power electronic devices and control techniques for Industrial, agrobase and food processing sectors.

The Institute can take up, with suitable inputs, the development of efficient adjustable speed AC drives (upto 500 KVA) soft starters (up to 500 HP motors) by optimising configuration of smart power switches (such as SIT, MCT) and other hybrid devices/latest electric machines and Microprocessor/PC based control techniques for specific applications.

The work done during the project has been internationally acknowledged.

VII. RECOMMENDATIONS

35. Concentrated efforts on the design development of ASICs and establishment of design verification and prototyping facility with adequate inputs. (Emphasis to be on Industrial ASICs suitable for operation in tropical countries like India).

36. Setting up of National Mask fabrication and inspection facility on commercial lines in private or joint sector.

37. Concentrated efforts on the design and manufacture of Power Transistors with matching inputs so as to make country self reliant and setting up a base for advanced Power Devices such as MOS controlled Thyristors (MCT's).

38. Wider use of Electronic Systems for the control and operation of AC motor drives. CEERI may be made Centre of Excellance for R&D in Power Electronics (AC drives) with suitable linkages with industry.

ANNEXURE - I

CONSTITUTION OF PROJECT ADVISORY COMMITTEE
AND ITS TERMS OF REFERENCE.

CONSTITUTION

1.	Dr. S.N. Acharya Director, Central Electronics Engineering Research Institute, Pilani.	Chairman
2.	Sh. M.S. Vasudeva Jt. Director, Department of Electronics, Government of India, New Delhi.	Member
3.	Sh. G.P. Dodeja, Executive Director, BHEL. New Delhi	Member
4.	Sh. B.V. Sehadri Head, EFF Div., ISRO, Bangalore	Member
5.	Sh. Virender Mohan CMD, S.C.L., SAS Nagar, Chandigarh.	Member
6.	Sh. K.N. Johry, Head, ISC, Council of Scientific & Industrial Research, Rafi Marg, New Delhi	Member
7.	Sh. G.M. Pillai, Deputy Secy. Dept. of Economic Affairs, Govt. of India.	Member
8.	Sr. Industrial Dev. Field Advisor, United Nations Industrial Development Organization, New Delhi.	Member
9.	Resident Representative, United Nations Development Programme, New Delhi.	Member

10. Dr. Amarjit Singh, National Expert, — Coopted Member

11. Dr. W.S. Khokle, Scientist, Central Electronics Engineering Research Institute, Pilani (Rajasthan) — Member-Convener

Terms of Reference

1. To review the progress of the project

2. To advise on the implementation of the project.

3. To advise on the utilization of the results by industry.

4. Any other matter related with the project implementation or utilization of its outputs.

13.	Power Transistors Design of 300 Darlington Transistor.	Dr. P.Rai Choudhary U.S.A.	Nov.-Dec. 1986 1 M/M
14.	Monolithic Integrated Circuits Development of LSI/VLSI Circuits.	Prof. P.Jespers Belgium	Dec.86-Jan.1987 .1 M/M
15.	Power Transistors: Computer Aided design of Power Transistors.	Prof. D.J.Roulston Canada	Dec. 1986 4 M/M
16.	Monolithic Integrated Circuits: Design for testability in NMOS EICMOS digital Circuits.	Dr. Peter Maxwel Australia	Jan.-Feb. 1987 1 M/M
17.	Power Transistor Devices for Transportation equipments.	Dr. H.Assalit, U.S.A.	Feb.-May 1987 3 M/M
18.	Solid State AC Motor Drive for Transportation and Adaptive Control Systems.	Prof. K. Matsuse Japan	Feb.-March 1987 1 M/M
19.	Solid State AC Motor Drive for Transportation Design & Fabrication of Transistor Inverter.	Prof. Ing.J.Holtz FRG	Dec.87-Jan.1988 1 M/M
20.	Monolithic Integrated Circuits,IC Processing & Fabrication.	Dr. S.P.Murarka U.S.A.	Dec.87-Jan.1988 1 M/M
21.	Solid State AC Motor Drive for Transportation.	Prof. Ing. J. Holtz FRG	1988 *
22.	National Expert	Dr. Amarjit Singh India	Dec.84-Jan.1987 (Split mission) 14.7 m/m

*Second visit Subject to availability.

ANNEXURE - III

NATIONAL PERSONNEL

1.	Dr. G.N. Acharya	Project Director
2.	Dr. W.S. Khokle	Scientist G
3.	Dr. S. Ahmad	Scientist EII
4.	Dr. P.D. Vyas	Scientist EII
5.	Shri K.L. Jasuja	Scientist EII
6.	Sh. O.P. Wadhawan	Scientist EII
7.	Dr. S.K. Bhatnagar	Scientist E
8.	Dr. Awatar Singh	Scientist E
9.	Sh. U.M. Rao	Scientist EII
10.	B.B. Dixit	Scientist E
11.	Sh. I.M. Sabharwal	Scientist E
12.	Dr. S.N. Gupta	Scientist E
13.	Sh. R.C. Dubey	Scientist E
14.	Sh. Y.K. Jain	Scientist C
15.	Dr. R.K. Nahar	Scientist C
16.	Dr. D.K. Thakur	Scientist C
17.	Sh. V.P. Deswal	Scientist C
18.	Dr. J.K. Singh	Scientist E
19.	Dr.Chandra Shekhar	Scientist E
20.	Sh. D. Pyne	Scientist C
21.	Sh. P.R. Deshmukh	Scientist C
22.	Sh. C. Ramachandra	Scientist C
23.	Sh. Rahul Varma	Scientist C
24.	Sh. R.P. Gupta	Scientist E
25.	Sh. N.K.I. Raja	Scientist C

54.	Sh. Anil Kumar	Scientist B
55.	Sh. B.D. Pant	Scientist B
56.	Sh. D.P. Runthala	Scientist C
57.	Sh. D.R. Nagpal	Scientist B
58.	Sh. A.K. Dubey	Scientist B
59.	Sh. J.P. Sharma	Scientist B
60.	Sh. D.S. Chawla	Scientist B
61.	Sh. A.K. Bagchi	Tech. Officer A
62.	Sh. M.S. Rathore	Tech. Officer A
63.	Sh. Satish Kumar	Sr. Technical Asstt.
64.	Sh. K. Pant	Scientist B
65.	Sh. Kamal Sadar	Tech. Officer A
66.	Sh. Suresh Chandra	Sr. Technical Asstt.
67.	Sh. Dwaraka Prasad	Sr. Technical Asstt.
68.	Sh. A.K. Sharma	Jr. Technical Asstt.
69.	Sh. K. Prasad	Jr. Technical Asstt.
70.	Sh. Baljit Singh	Jr. Tech. Asstt.
71.	Sh. R.N. Singh	Jr. Tech. Asstt.
72.	Sh. P.K. Sharma	Sr. Tech. Asstt.
73.	Sh. B.C. Joshi	Jr. Tech. Asstt.
74.	Sh. P.K. Yadav	Jr. Tech. Asstt.
75.	Sh. Mahesh Kumar	Jr. Tech. Asstt.
76.	Sh. Bhanwar Singh	Jr. Tech. Asstt.
77.	Sh. H.C. Pathak	Jr. Tech. Asstt.
78.	Sh. O.P. Sharma	Jr. Tech. Asstt.
79.	Sh. D.D. Joshi	Jr. Mech. Asstt.
80.	Sh. B .C. Pathak	Sr. Tech. Asstt.

ANNEXURE - IV

FELLOWSHIP TRAINING

S.No.	Name	Duration	Place v
1.	Dry Processing Technique (Dr. U.S.Tandon)	No.84-Jan.85 2.5 M/M	U.S.A.,
2.	Power Devices Design Testing (Mr. K.L.Jasuja)	April-Sept.1985 5 M/M	U.S.A,C
3.	High Power Transistor Processing (Dr. D.K.Thakur)	June-Oct.1985 4.3 M/M	U.S.A.
4.	Harmonic Elimination in PWM Inverter for AC Drives (Mr. S.D.Perlekar)	Sept.85-Jan.1986 5 M/M	U.S.A.
5.	Processing of Monolithic MOS ICs (Dr. Chandra Shekhar)	Nov.85-May 1986 6 M/M	Belgium
6.	Hybrid ICs (Dr. S.K.Bhatnagar)	Oct.85-March 1986 5 M/M	U.S.A.
7.	Monolithic ICs (Mr. O.P.Wadhawan)	Feb.86-July 1986 5 M/M	Belgiur
8.	Maintenance of Equipment (Mr. C.Ramachandra)	Feb.86-June 1986 4 M/M	U.S.A., Belgiur
9.	Hybrid ICs Training on Laser Trimmer. (Mr. Y.K.Jain & Mr. HC Pandey)	Feb.86-March86 1 M/M	U.S.A.
10.	CAD of Power Devices (Mr. S.K.Mahajan)	May 86-Aug.1986 3 M/M	Canada
11.	CAD of Power Transistor (Mr. Anil Kumar)	May 86-Aug.1986 3 M/M	Canada
12.	Feed Back Controls of AC Drives (Mr. Rahul Varma)	Nov.86-April 87 5 M/M	U.S.A.
13.	Monolithic ICs Mr. KVS Hanumantha Rao)	Feb.87-April 87 2 M/M	Belgium
14.	Mask Making Dr. S.N.Gupta)	Feb.87-May 1987 3 M/M	U.S.A.,I France,(

15.	Efficiency Optimisation of AC Drives. (Mr. U.M.Rao)	May 87-Oct.87 5 M/M	U.S.A.
16.	VLSI Design Dr(Mrs.)S.Srivastava	June 88-Aug.1988 2 M/M	Belgium
17,	VLSI Processing (Dr. V.K.Dwivedi)	Sept.88 Nov.88 2 M/M	Belgium

ANNEXURE - VI

EQUIPMENT PROCURED UNDER UNDP FUNDS

S.No.	Name of Equipment	Price of Invoice
1.	Vacuum brazing die-attach equipment	172,821.00
2.	Programmable furnace	26,772.59
3.	Laser for hybrid circuits trimming and allied applications/wafer cutter	233,935.00
4.	i) Quartz tube baking and ii) Sealing equipment	6,325.00 26,564.00
5.	Microprocessor development system	50,000.00
6.	Digital storage oscilloscope	10,974.40
7.	Bevelling contouring machines	27,992.40
8.	Spin etch machine	30,695.38
9.	(i) Dynamic test modules for power devices. (ii) Press for fusion testing	86,280.00
10.	Variable frequency 3 phase AC Motors	8,000.00
11.	CAD software and hardware	231,986.00
12.	Expendable Equipment	110,078.00
13.	Spares accessories and other expenses	234,648.23
		$ 1,257,072.00

ANNEXURE - VII

EQUIPMENT PROCURED UNDER COUNTER PART FUNDS

S.No.	Name of Equipment	Price in Million Rupees
1.	Standy Power Plant(Additional capacity)	1.2
2.	High purity Nitrogen supply system from liquid Nitrogen	0.3
3.	Oscilloscope and accessories	0.2
4.	Muller Grinder	0.4
5.	Hot Probe Tester	0.1
6.	Electroplating set-up and thickness measurement	0.1
7.	Programmable furnace with controlled loading,unloading	0.8
8.	Accessories for Vacuum Systems	0.2
9.	Accessories for CAD	0.4
10.	Accessories for Mask Making	0.4
11.	Accessories for bonding	0.1
12.	Laping Machine	0.4
13.	Polishing Machine	0.45
14.	Spares for Furnaces	0.2
15.	Mask Storage, Slice Storage boxes	0.1
16.	General Repair Instruments and Tools	0.1
17.	Clean Room Monitoring Accessories	0.2
18.	Ion Implantation spares and accessories	0.6
19.	Water Treatment Plant and accessories	0.7
20.	Laminar flow benches	0.5
21.	Spcialized Measurement Systems Switching Measurements, etc.	2.0
22.	Wafer probes	0.15

23. 1000 KVA Transformer	0.26
24. 200 KVA Automatic Voltage Regulators	0.40
25. Three tubes thermco diffusion furnace	0.84
26. Multilevel stand alone computer system	1.80
27. Double side mask alligner	1.80
	14.80

ANNEXURE-VIII

CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE
PILANI (RAJASTHAN)

Note on the nature of the products and processes developed under the UNDP Project (No.IND/015/84)

It may be noted that all the products and processes developed under this programme are of a generalised nature so that they can encompass a wider cross-section of applications. The following paragraphs indicate the range of applications and the generality of the designs that have been attempted.

(i) Microprocessor Based A.C. Motor Drive for Transportation:

This has been chosen as a package system to be developed because of the highest level of complexity and the variety of combination of load and speed it provides. Once such a microprocessor based system is developed for the transportation application, the same system with some modifications in the programme can be made to suit the requirements for other applications such as Variable Speed Drives for Compressors, Crane Drives, Variable Speed A.C. Motor Drives used in the Centrifusing operations in the Sugar Industry, A.C. Motor Drives for Agricultural Pumps etc.

In addition some of the sub-systems such as Solid State Switches, Soft Starters etc. can also be used for other applications.

In fact a basic Microprocessor Based A.C. Motor Drive with its logic and control sub-system based on the new concepts being attempted on this project can be used over a fairly wide range of powers as well as frequencies.

(ii) Microchips:

Out of the 3 ASIC microchips which have been developed, the VME bus compatible A/D-C interface chip can be used with any Microprocessor Based System using Motorola 68000 CPU. As such, the application of the chip is not limited to A.C. Motor Drives but it can be used with other 68000 systems required in the process control industry and other applications also because of the features of programmability introduced in this chip.

The PWM Processor chip has a number of extra facilities and also higher speed of operation which also extends its application area to other type of A.C. Drive applications.

(iii) Power Transistors:

Darlington Power Transistors being developed under this programme can cover practically any range of applications and can be used upto about 80 KW drives.

Apart from A.C. Motor Drives it can be used for other applications such as Inverters for iced line refrigerators (ILR) uninterruptible power supplies, Solid State Switches etc.

Talking about the technology and software that has been developed under this programme which involves fine line geometry structures, it can be seen that this capability can be extended not only to other types of transistors but also to a number of other power devices with varying switching characteristics as well as current levels.

(iv) Hybrid Microcircuits: (HMC's)

In itself this technology also can cover, many applications. The circuits for the base drives for transistor upto 300 A ratings which have been developed under this programme are also generalised enough to cover other range of applications including transistor choppers, as well as base drive circuits for other applications of the power transistors in that range.

Further miniaturisation of the entire base drive circuit alongwith other components is being taken up so that a complete standard Opto-coupled base drive circuit can be developed so as to cover good number of other applications.

Apart from this a number of spin off products and processes including (a) software for silicon compilers, (b) new products

and processes such as high power resistors, new techniques for the measurement of speed and estimation of rotor current by using the information available on the stator side, giving scope to the development of new signal processing ASIC capable of deriving information in the form of pulses which can be counted and the rotor current value estimated on the basis of the pulse heights etc. have emerged out of the present UNDP programme.

It is thus seen that the entire programme is leading to a set of technologies which are general enough to be applied beyond the range of transportation drive which has been kept as the main focus from the point of view of testing of feasibility of the products and processes being developed under this programme.

HARD AND SOFT OUTPUTS

POWER SEMICONDUCTOR DEVICES
HARD OUTPUTS

CEERI has established the expertise, facilities and infrastructure to develop the design and proces capability for large-area power devices. CEERI scientists are already interacting and collaborating with one of the leading power device manufacturing organissations, namely BHEL in the field of power semiconductor devices. Exchange of technical information, visits of scientists and engineers and extending of process facilities has become a matter of routine with BHEL.

The technology output can be divided into the following groups:

1. Transfer and utilisation of technology upto the stage of actual production.

A sponsored project to CEERI by BHEL, Bangalore on the design and development of inverter grade fast switching thyristor (1700 V, 1300A) was jointly developed to the satisfaction of the sponsoring agency. Devices produced by BHEL have already been incorporated in actual circuits and user trial report is satisfactory. The device is presently under production.

2. Proposals for technology transfer in the pipeline

(a) Computer aided device design and fabrication process development of (100 A, 500V) Monolithic Power Darlington Transistor has been completed. Packaged devices have been tested for actual use in inverters for transport applications.

A close link with BHEL, Bangalore has been maintained. The objective is to develop and transfer the technology compatible with production needs by working jointly with the production agency.

(b) M/s Naina Semiconductors Ltd. are setting up a project with UPTRON to manufacture semiconductor devices, initially rectifier diodes from 1 to 30 A with a plant capacity of 100 million devices per annum. The Company has approached CEERI for consultancy service in the area of wafer diffusion and standardising the process line. An understanding has been signed between CEERI and the Company.

3. Request received from industry and users for utilisation of the technology developed.

Negotiations are in progress with Keltron Power Devices Ltd. for possible know-how transfer. The firm is interested in the TV horizontal deflection transistor.

Our linkages with industry are summarised in Table1

Hard Outputs

(Linkages with Industry)

S.No.	Name of the firm	Device	Type of interaction
1.	BHEL, Bangalore	a) Fast Switching Thyristor 1700V, 1300A.	Design and development of the thyristor done by CEERI under a sponsored project. Device commercialised by BHEL.
		b) Darlington Transistor 100A, 500V 300A, 400V	Collaboration with BHEL for possible know-how transfer.
2.	Naina Semiconductors Ltd. (a Company under formation with proposed site at Rishikesh).	Silicon Rectifier Diodes 1 to 30A upto 1000V	Consultancy service in the area of wafer diffusion and standardising the process line.
3.	Keltron Power Devices Ltd., Trichur.	Deflection Transistor (Bu-205)	Correspondence in progress for know-how transfer.

Soft Outputs

Research Publications

1. Design and Development of Monolithic Power Darlington Transistor

   Conf. Record of the 1986 IEEE-IAS Annual Meeting, Denver, Colorado, Sept. 28 - Oct. 3, 1986, pp 420-428.

2. Design Consideration and Development of Fast Switching Thyristor.

   Conf. Record of the 1986 IEEE-IAS Annual Meeting, Denver, Colorado, Sept. 28 - Oct. 3, 1986, pp. 404-412.

3. R&D in Power Semiconductor Devices, Electronics Today, July 1987.

4. Process - Induced Influence on the Minority Carrier Lifetime in Power Devices.

   5th International Symposium on Semiconductor Processing ASTM, Santa Clara, California, Feb. 3-5, 1988.

5. Monolithic Power Darlington Transistor for AC Drives National Seminar on AC Motor Drives for Transportation and Industrial Electronics, CEERI, Pilani, April 15-17, 1987.

6. 1700V, 1300A Inverter Grade Thyristor, National Seminar on AC Motor Drives for Transportation and Industrial Electronics, CEERI, Pilani, April 15-17, 1987.

7. Characterization and Transient Analysis of Monolithic Power Darlington Transistor for AC Drives Using CAD as a Tool.

   Conf. Record of the 1987 IEEE-IAS Annual Meeting, Atlanta, Georgia, Oct. 18-23, 1987.

8. Minority Carrier Lifetime as Monitor for Process Evaluation.

9. IP 830, IP 750 Glass Passivation for Mesa Grooved Poly/Nitride Coated Semiconductor Devices.

   (Papers 8 and 9 to be presented at International Conference and Intensive Tutorial Course on Semiconductor Materials, Dec. 88).

b. MONOLITHIC ICs GROUP

HARD OUTPUTS

WE HAVE FACILITIES FOR BOTH DESIGN AND PROTOTYPING

ICs DESIGNED AND PROTOTYPED:

(A)	8-BIT BINARY COUNTER	:	200 TRANSISTORS (PROTOTYPED AND TESTED)	22 PIN PACKAGE MADE AT CEERI CHIP SIZE 3x3 mm2
(B)	A CUSTOM CHIP FOR uP BASED 32-LINE TELE PHOINE EXCHANGE	:	500 TRANSISTORS (PROTOTYPES USED IN SYSTEM FOR DEMONSTRATION)	44 PIN CERAMIC LEADLESS CHIP CARRIER CHIP SIZE 3.35x3.35mm2
(C)	A VME-BUS COMPATIBLE CONTROLLER CHIP FOR MULTI CHANNEL ANALOG DATA ACQUISITION	:	800 TRANSISTORS PROTOTYPED AND TESTED	48 PIN CERAMIC DIP CHIP SIZE 4.3x4.3mm2
(D)	A CUSTOM CHIP FOR 96 LINE TELEPHONE EXCHANGE	:	600 TRANSISTORS CURRENTLY BEING PROTOTYPED	48 PIN CERAMIC DIP
(E)	A DEDICATED 16 BIT PROCESSOR FOR PWM CONTROL OF A.C. DRIVES	:	10,000 TRANSISTORS (PROTOTYPED ABROAD) UNDER GOING AN ITERATION CYCLE	CHIP SIZE 5.3x4.4mm^2 -4.7x3.4MM2
(F)	SERIAL DATA - LINK CONTROLLER	:	10,000 TRANSISTORS TO BE FABRICATED	

Publications: CSD-VLSI Design (Monolithic ICs)

1. S. Srivastava and Chandra Shekhar, "A comprehensive NMOS LSI Process development Vehicle", presented at the 2nd International Workshop on Physics of Semiconductor Devices, New Delhi, Dec. 5-10, 1983.

2. S.C. Bose, S. Srivastava, Chandra Shekhar and W.S. Khokle "Review of MOS models for use in CAD for LSI", Invited paper at the workshop on review of state of the art in CAD for LSI/VLSI, held at semiconducter complex limited, Chandigarh (India) in April 1985.

3. S.C. Bose, S. Srivastava, Chandra Shekhar & W.S. Khokle, "Accurate comutation of inversion charge in MOS structures on uniformly doped substrates", Presented at the International Conference on Microelectronics and fibre optics, CSIO, Chandigarh, Nov. 1985.

4. S.C. Bose, S. Srivastava, Chandra Shekhar and W.S. Khokle "Review of MOS models for use in computer aided design (circuit simulation) of LSI circuits" IETE Technical Review Vol. 3, No. 7, (1986).

5. Chandra Shekhar, S.De Sirkar, S.D. Deo, K.V.S.H. Rao and S. Srivastava "A VME bus compatible ADC interface chip", Microelectronics and Reliability Vol. 27, Ni. 1, pp 61-63, 1987.

6. Chandra Shekhar, K.V.S.H. Rao, S. Srivastava, A. Dumont, E. Gilson, J.L. D'Aout, J. Remy and P. Jespers". A PWM processor for Inverter Control" presented at the national seminar on AC Motor Drives for Transportation and Industrial Applications" held at CEERI, Pilani, April 15-17, 1987.

7. S.C. Bose, S. Srivastava, Chandra Shekhar, S. Gupta and S.K. Chattopadhyay mobility in MOS transistors using I-V measurements" Accepted for presentation at the "International Symposium on Electronic Devices, Circuits and Systems" IIT, Kharagpur, Dec. 15-17, 1987.

8. S.C. Bose, S. Srivastava, Chandra Shekhar and W.S. Khokle "Accuracy of conventional inversion charge modeling in scaled down MOS devies" Microelectronics Reliability, vol. 28, No. 1, pp. 15-17, 1988.

9. "Testing of ASICs in Indian Context" KVSH Rao, Chandra Shrama, S. Srivastava and Rahul Verma, National Seminar on Microprocessor based electronic systems and ASICs for Industrial Applications to be held at CEERI Pilani, Sept. 21-23, 1988.

10. "A CAD tool for PLA based finite state machine generation" S. Srivastava, Raj singh, S.C. Bose, Alpna Kansal, KVSH Rao and Chandra Shekhar to be presented at VLSI India, Dec. 15-18, 1988.

M.Tech Theses/Projects (CAD - VLSI Design)

1. "Computer aided circuit and layout design of a 16-bit multiplier chip" M.Tech thesis by Sabuson George, IIT Kharagpur (1984).
2. "Design a standard cell library for semi-custom LSI design" M.Tech thesis by Karanjkar, IIT Kharagpur (1984).
3. "Design of Micro power NMOS operational amplifier" M.Tech thesis by Ms. Padma Maganty, IT, BHU, (1984).
4. "Computer aided design, analysis and layout of VME bus compatible controller chip for A/D conversion" M.Tech Thesis by S. De. Sirkar, IIT Kharagpur, (1985).
5. "Computer aided design, analysis and layout of dynamic RAM cells and cells for a VME bus compatible LSI controller chip for A to D conversion" M.Tech thesis by S. Deo, IIT Kharagpur (1985).
6. "Computer aided design of the mask-level layout for a finite state machine controller" M.Tech.thesis by Rahul A. Muley, IIT, Kharagpur, (1986).
7. "Development of silicon compiler for finite state machines" M.Tech thesis by V. Chandramouli, IIT, Kharagpur, (1986).
8. "Studies in devices in Integrated Circuits", M.Sc. thesis by Sanjay Khendry, BITS, Pilani (1986).
9. "MOS devices in integrated circuits" M.Sc. Thesis by Sanjay Khendry, BITS, Pilani (1986).

10. "Design for Testability a study and Application to PLAs" M.Tech. thesis by Ms. Vasundhara Despande, IIT Kharagpur (1987)

11. "Numerical Modeling for small Geometry MOS devices in two dimensions" M.Tech thesis by Sandeep Suresh Aranake, IT, BHU, Varanasi (1987)

12. "Front end of PLA based FSM silicon compiler" B.Tech summer project by Alok Sharma and Alok Bhatt, IE&T, Lucknow (1988)

13. "A. functional simulator for block level design verification" M.Tch thesis subject of three students:

    (i) S Kashyap VC, Nagpur,
    (ii) M.Vaidya Nath, IIT Madras
    (iii) Selvarajan IIT, Kharagpur

14. "Study of sub-threshold conduction in small geometry MOS transistors and its bearing on MOS device design for high temperature oepration"Ph.D. work being pursued by Ms. Neeta Joshi, JRF, CEERI.

15. "Modeling studies in MOS devices for VLSI aplications" topic of Ph.D. being pursued by S.C.Bose.

Publications : (MOS Technology)

1. "Fabrication of 8-bit Binary Counter Circuit" O.P. Wadhawan, P.N. Andhare, V.K. Dwivedi, D.P. Runthala, S.S. Shekhawat, S. Johri and W.S. Khokle, Proceedings National symposium on MICCASP, Osmania Univ. 1984.

2. "On the Development of Poly-gate n-MOS Technology" O.P. Wadhawan, A. Srivastava, D.P. Runthala, S.S. Shekhawat, P.N. Andhare, V.K. Dwivedi and W.S. Khokle, Microelectron. Reliab. Vol. 25, No. 3, 1985.

3. "All Implanted n-MOS Process" V.K. Dwivedi, G.S. Virdi, S. Gupta and W.S. Khokle, Microelectronics Journal, Vol. 18, No. 1, 1987.

4. "Fabrication of n-MOS Custom Subscriber Chip for a Telephone Exchange", V.K. Dwivedi, S. Gupta, S. Johri, G.S. Virdi, O.P. Wadhawan, W.S. Khokle, Microelectronics Journal Vol. 19, No. 2, March/April, 1988.

Report - Theses (MOS Technology)

1. "Silicon Oxidation Studies for MOS Devices" M.Tech Thesis by Vinay Kumar Sawarkar, Inst. of Tech., BHU Baranasi, Dec. 1984.

2. "Silicon Gate NMOS Process" O.P. Wadhawan, CEERI technical report, 1985.

3. "A model parameter extraction programme for MOS transistors" CEERI technical report by Dr. (Mrs.) Sobha Gupta, 1986.

4. "Oxidation Techniques and Evaluation in the Processing of Silicon Devices" B.Tech Summer Project by Ehtisham Andrabi, REC, Srinagar, 1987.

5. "NMOS SUPREM Simulation and Experimental Verification" M.Tech thesis by J.C. Rastogi, IIT, Kharagpur, 1987.

Hybrid Microcircuits

Hard & Soft Outputs

HARD OUTPUTS

a) Transfer and utilisation of technology upto the stage of actual production :

Know-how of process for manufacturing hybrid microcircuits has been transferred to M/s Minicircuits Ltd. Bangalore. The firm is now in commercial production of HMCs.

b) NIL

c) The HMC Lab. at CEERI is one of the first space qualified facility in India. HMCs developed by CEERI were used in SROSS-I & SROSS-2 satellites. Three different types of HMCs have also been developed for INSAT-II project. The followings are the CEERI's HMCs customers:

1.	ISRO Satellite Centre, Bangalore	¶
		¶ Space qualified HMCs
2.	VSSC Trivandrum	¶
3.	a) Power Hybrids	¶
	b) HMCs for Sugar Industries	¶ In house
	c) HMCs for SECRAPHONE PROJECTS	¶

B. SOFT OUTPUTS

Papers Published/presented - 9.

Patents - 1.

PAPER PUBLISHED BY HMC GROUP

1. Direct Laser Beam Writing on Y-BaCuO Film for Superconducting Microelectronic Devices, Jour. of Appl. Phys., 27, (1988)

2. Via Terminating Resistor (VTR) A New Thick Film Structure, Paper presented at the Annual Conf. of ISHM India (1988).

3. Interdiffusion Phenomena and Electrical Conduction in Thick Film Segmented Resistors, Accepted in J.phys. D: Applied Phys., (1988).

4. Development of Hybrid Microcircuits for A.C. Motor Drives, National Seminar AC Motor Drives for Transportation and Industrial Applications. April 15-17, 1987, CEERI, Pilani (Raj.).

5. Development of a Thick-Film Tunable RC-Active Filter using Segmented Resistors, Int. J.Electronics, 63, 1 (1987).

6. Interactions between Thick Resistive Films and Design Criteria for Segmented Resistors, J.Phys.D:Appl, Phys., 20 664 (1987).

7. A Thick-Film Segmented-Resistor Structure for High Trimfactors, Active and Passive Electronic Components, 12, 187 (1987).

8. Line Certification/Qualification of HMCs for High reliability Applications - ISAC Experience Symposium on Thickfilm Materials and HMCs on 18-19 Dec., 1986, Bangalore.

9. Performance characteristics of a Thick-film segmented- Resistor Structure, Proc. Int. Microelectronics Conf. Japan (SHM), 497 (1986).

LIST OF INTERNAL REPORTS

1. Passivating Layers on Semiconductors.
2. Feasibility study of low cost radio receiver using integrated Circuits.
3. Thick Film Hybrid Integrated Circuits.
4. Hybrid integrated Circuits - some work being done at R&D and and production facilities in France.
5. Quality control and Evaluation of substrates for hybrid micro-circuits.
6. Packaging of hybrid integrated circuits.
7. Development of thick film technology at CEERI, Pilani.
8. Cost estimates for development of hybrid circuits and consultancy services.
9. Seam sealing and leak tests.
10. Process Document for Hybrid Micro Circuits.
11. Evaluation of Adhesives for mounting mash cloth to metal frame.
12. Toxic/Hazardous chemicals commonly used in Thick Film Fabrication.
13. Development of Computer Programe in Pascal Language Applicable to HMC Design.
14. Some studies of R-C Active Filters.
15. Development of Power HMC under UNDP Phase II Programme.
16. Regarding Capability of CEERI in Hybrid Microcircuits.

LIST OF PATENTS

1. A process for formation of stencil for solder cream printing on thick film Hybrid Circuits 633/Del/87.

HARD AND SOFT OUTPUTS
d (Electronics Systems Group)

HARD OUTPUTS

(A) PRODUCTS:

* 20 KVA AC MOTOR DRIVES USING TRANSISTOR INVERTER
* 40 KVA PWM THYRISTOR INVERTER FOR MINING LOCOMOTIVE (PARTIALLY FUNDED BY BHEL, BHOPAL)
* INVERTER USING CEERI MADE 100 AMP TRANSISTORS

(B) BY PRODUCTS:

* MICROPROCESSOR BASED PWM LOGIC
* MICROPROCESSOR BASED FEEDBACK LOGIC
* FAST SOLID STATE DC CIRCUIT BREAKER
* PROTECTION CIRCUIT
* A SINGLE PHASE TO THREE PHASE CONVERTER USING 100 AMP CEERI MAKE TRANSISTOR TO USE WITH ERIGATION PUMPS FOR RURAL APPLICATIONS.
* 300 WATT. SWITCHED MOD POWER SUPPLY INPUT FOR MATERIAL MOVEMENT APPLICATION IN INDUSTRY.
* ESTABLISHED THE BASIC INFRASTRUCTURE AND FACILITIES TO UNDERTAKE POWER ELECTRONICS PROJECT UP TO 200 KVA POWER LEVEL.

SOFT OUTPUTS

* PAPERS PUBLISHED /PRESENTED - 7
* PATENTS - 1
* RESEARCH REPORTS - 15
* POSTGRADUATE THESIS - 6
* GRADUATE TRAINING REPORT - 24

LINKAGES DEVELOPED WITH ACADEMIC INSTITUTIONS

* IIT, POWAI, BOMBAY
* IIT, ADIYAR, MADRAS
* UNIVERSITY OF WISCONSIN, MADISION USA

PUBLICATIONS

ELECTRONIC SYSTEMS GROUP

(a) Published Papers

(i) "Microprocessor based based PWM Inverter using modified regular sampling techniques". IEEE Trans. on Industry Applications (Mayy-June 1986).

(b) Presentation in Symposium/Seminars/Workshop

(i) "Microprocessor based PWM AC Drives for Electrical Vehicles" Workshop on the use of Semiconductor Devices and Electronic Subsystems for Transporation and Industrial Applications using Solid State AC Motor Drives - April 25-26, held at CEERI, Pilani.

(ii) "A New Concept for PWM Generation". National Seminar on AC Motor Drives for Industrial and Transportation Applications Feb. 10-12, 1987, CEERI Pilani.

(iii) "Evolution of High Performance Semiconductor Technology for Harh Environment"-Same conference mentioned above.

(iv) Power Electronics - An emerging technology for saving of energy"" -FICCI National Conference cum exhibition on energy saving in Industry"- 25th-26th Feb., 1985 held at New Delhi.

ANNEXURE-X

List of Engineer/Scientists Trained from within the country.

S.No.	Name of Student	Topic	University/Instt./College	Duration
Monlithic ICs Group				
1.	Sh. Soumitra Deo, Sirkar	The Computer aided design analysis and layout of VME bus compatible controller.	I.I.T. Kharagpur	5 months May-Nov.85
2.	Sh. S.D. Deo	Computer Aided design Analysis & layout of Dynamil Ram Cells for VME Compatible LSI controller chip for A/D conversion.	I.I.T. Kharagpur	6 months May-Nov.85
3.	Miss Padma Maganty	Linear MOS IC design.	B.H.U. Varanasi	6 months July-Jan.85
4.	Sh. Jagdish lal	Fabrication of Shallow Boron-doped Junction in Silicon By Ion Implantation	I.I.T. Kharagpur	5 months June-Nov.85
5.	Sh. Rahul A. Mulay	Computer Aided Design of the Mask level Laycuts for a finite State Machine Controller.	I.I.T. Kharagpur	6 months June-Dec.86
6.	Sh. N. Ramesh Babu	Microprocessor Based PWM Inverter using Area Technique.	Regional Engg. Collage, Werangal	9 months May 86-March 87
7.	Sh. K.V. Rama Rao	Microprocessor based Date Acquuisition and Control System.	Regional Engg. Collage Werangal	9 months May 86-March 87

8.	Mr. S. Satish Chandra Kr.	Reliability of Dielectric layer.	I.I.T. Kharagpur	4 months July-Nov.86
9.	Mr. Ashnarayan Singe	Theorotical supported by experiment.	I.I.T. Kharagpur	5 months June-Nov.86
10.	Mr. Deb Kumar Pal	Fabrication of MOSFET.	I.I.T. Kharagpur	5 months June-Nov.86
11.	Mr. V.Satheesh Kumar	Implementation of DMA for high speed Data transfer.	I.I.T. Kharagpur	5 months June-Nov.86
12.	Mr. Shailash Shukla	Design and Development of a Token Bus LAN Controller.	B.I.T.S. Pilani	4 months Aug.-Dec.86
13.	Mr. V. Chandramouly	Development of Silicon Compilar for Finite State Machines.	I.I.T. Kharagpur	6 months June-Dec.86
14.	Mr. Rajesh Abbi	Development of Computer simulation System for Lithography.	B.I.T.S. Pilani	4 months Aug.Dec.86
15.	Mr. Sanjay Kendry	Programme development of an n-channel MOS device.	B.I.T.S. Pilani	4 months Aug.-Dec.86
16	Sh. V.K. Namboori	Development of Unit Process for GaAs MMICs.	Delhi University	8 months Jan.-Sept.87
17	Sh. A.K. Sharma	Design and Fabrication of Passive Components for GaAs MMICs.	Delhi University	8 months Jan.-Sept87
18.	Sh. Rajesh Sukhija	ANMOS IC Process Simulation Using Suprem - II Programme.	R.E.C. Kurukshetra	2 months June-Aug.87
19	Sh. Jayant Kumar	Testing of Controller chip with Logic State Analizer.	R.E.C. Kurikshetra	2 months June-Aug.87
20.	Sh. P.Salvarajan	Functional Simulation for VLSI Design	IIT, Kanpur	6 months June-Dec.88
21.	Sh. Savarker	M.Tech. Thesis "Studies on MOS Oxides"	BHU, Varanasi	6 months June-Dec.84

22.	Sh. Anil Kumar	Testing of Controller chip with Logic State Analizer.	R.E.C. Kurukshetra	2 months June-Aug.87
23.	Sh. Denish Kumar Singh	Computer Aided Design of Microchip Element.	HBT Institute, Kanpur	2 months May-July 87
24.	Sh. J.C. Rastogi	Short Channel NMOS Simulation & Experimental Varifications.	I.I.T. Kharagpur	6 months June-Nov.87
25.	Sh. Sandeep Suresh Aranake	Numerical Modelling for small Geometry MOS Devices in Two Dimension.	I.T. BHU, Varansi	6 months May-Nov.87
26.	Sh. Denesh Bolwalkar	Data Highway for /uP based system	I.I.T. Kharagpur	6 months May-Nov.87
27.	Sh. B.L. Sharma	Conversion to 6 /uW NMOS PWM chip to 3 /uW CMOS Design.	I.I.T. Delhi	6 months May-Nov.87

Power Transistor Group

1.	Mr. Harminder Singh	Preliminary study of mask making process Automation.	MNR Engg. College Allahabad	2.5 months
2.	Mr. K.S.Krishnan	Quality Assurance	BHEL Bangalore	2 Weeks
3.	Mr. Narayanan	-do-	-do-	2 Weeks
4.	Miss Akshai Anand	Mask Making	REC Hazrat Lal Srinagar	3 months Dec.-86 March-87

Hybrid Microcircuit

1.	Sh. Saket Jain	Software development in PASCAL Language applicable to HMC Design.	MBM Engineering College	2.5 months
3.	Trainees from Minicircuits Pvt. Ltd.,	6 Nos.	Minicircuits Pvt. Ltd.	2 Week each

Power Electronics Group

1.	Sh. K.M. Sundaram	Training on 40 KVA PWM Inverter for Mining Locomotives.	B.H.E.L., Bhopal	1986 to Continue as & when required.
2.	Sh. S.K. Jain	----do----	----do----	----do----

Post Graduate Trainees

3.	Sh. R. Babu Nukala	Microprocessor based PWM Inverter using Area Technique.	R.E.C., Warangal	May, 1986 to March, 1987 (10 months).
4.	Shri D.D. Gupta	Microprocessor based UPS System.	----do----	March, 87 to Jan., 88
5.	Sh. A.M. Ghate	Microprocessor based UPS System using MC Murray Inverter.	V.R.C.E., Nagpur	July, 88 to Dec., 88 (6 months).
6.	Shri G.N. Bangale	To design and develop Microprocessor based Power Meter using MF 10 for fundamental Power Voltage current, power factor, measurements of non-sinusoidal voltage sources.	----do----	----do----

7.	Sh. D.B. Mohod	50 KVA Variable Speed Induction Motor Drive using Delta Modulation Techniques.	----do----	----do----
Under Graduate Trainees				
8.	Sh. Arun Kumar	Development of ROM based (Six Step) Logic for Voltage Source Inverter	College of Science, Sukhadia Univ., Udaipur.	May, 88 to Oct., 88 (5 months).
9.	Miss Punam Gupta	Design of Low Pas Filter.	R.E.C., Roulkela (Orisa).	May, 85 to June,
10.	Mr. M. Rafique	Design & development of MOSFET Inverter.	M.B.M. Engineering College, Jodhpur.	May, 85 to Aug., 85 (4 months).
11.	Mr. Avanindra Sharma	----do----	----do----	----do----
12.	Mr. Vineet Gupta	To study of bit up 8085 & 16 bit up MC 68000 (motorrla) and to develop certain Programme.	Delhi College of Engg. Delhi.	July, 85 to Aug., 85 (2 months).
13.	Mr. Jaswant Dabi	----do----	----do----	----do----
14.	Mr. H. Pandey	High Efficiency Inverter for start powered tube light.	M.B.M. Engineering College, Jodhpur.	May, 86 to Aug., 86 (3 months).
15.	Mr. S. Gupta	Development of three phase Hexfet Inverter.	I.I.T., Kharagpur.	May, 86 to July, 86 (3 months).
16.	Mr. S. Mitra	----do----	----do----	----do----

17.	Mr. Sachivanand	Design and fabrication of constant current source.	R.E.C., Shrinagar (J&K).	Dec, 86 to March, 87 (3 months).
18.	Mr. S. Manchanda	----do----	----do----	----do----
19.	Mr. Yogesh Gaur	A study of the effect of non-sinusoidal supply (six step) on the performance on an Induction Motor.	M.B.M. Engineering College, Jodhpur	May, 87 to July, 87 (2 months).
20.	Mr. Ajay Gupta	To design Logic for a Chopper Circuit.	College of Engineering Sewagram, Wardha.	June, 87 to July 87 (2 months).
21.	Mr. M.B. Daigavani	----do----	----do----	----do----
22.	Mr. M. Kaushal	To build diagonstics of Inverter Circuit.	----do----	----do----
23.	Mr. Manmohan Agarwal	----do----	----do----	---do----
24.	Mr. P. Saraf	Design of 60 KVA Power Supply.	Delhi College of Engineering, Delhi.	May, 88 to June, 88 (2 months).
25.	Mr. S. Varshney	To study Stepper Motors and to design and develop its Controller and draw the torque speed characteristics.	I.I.T., Kanpur	May, 88 to July, 88 (2 months).
26.	Mr. R. Sinha	A report on 0-440 V 100 Amp D.C. to D.C. Chopper.	College of Engineering Sewagram, Wardha.	June,88 to July, 88 (2 months).
27.	Mr. Vikas Biane	----do----	----do----	----do----
28.	Mr. Mohit Garg	----do----	----do----	----do----

29.	Mr. G.B. Deshpande	Design of three phase Full Wave rectified power supply filter.	----do----	----do----
30.	Mr. N.V. Deshpande	Design of 150 Watt SMPS.	----do----	----do----
31.	Mr. K.V.R. Harsha-vardhan	Solid State Temperature Controller.	B.I.T.S., Pilani.	June, 88 to July 88 (8 weeks).
32.	Mr. P. Devendra Patel	Development of Control Processing Unit Card.	----do----	----do----

ANNEXURE-XI

LINKAGE ESTABLISHED WITH INDUSTRIAL ORGANIZATIONS

CONTENTS

LINKAGES ESTABLISHED WITH INDUSTRIAL ORGANIZATIONS

A. Power Semiconductor Devices

1. BHEL: A sponsored project to CEERI by BHEL, Banglore on the design and development of inverter grade fast switching thyristor (1700V, 1300A) was jointly developed to the satisfaction of the sponsoring agency. Devices produced by BHEL, have already been incorporated in actual circuits and user trial report is satisfactory. The device is presently under production.

2. M/s Naina Semiconductors Ltd: are setting up a project with UPTRON to manufacture semiconductor devices, initially rectifier diodes from 1 to 30 A with a plant capacity of 100 million devices per annum. The Company has approached CEERI for consultancy service in the area of wafer diffusion and standardising the process line. An understanding has been signed between CEERI and the Company.

B. Monlithic IC's Group

1. C-DOT

Data Communication Controller Chip is being designed on request from C-DOT.

2. SAC (ISRO) Ahmedabad request has been received for developing ASICs for them. CEERI team has visited them from 14th to 17th Sept. for identification of ASICs. The process of identification of Chips for development is in progress.

C. Hybrid Micro Circuits (HMC's)

1. ISRO: The Institute has been recognized as the only agency to design develop and fabricate space qualified Hybrid Micro Circuit. The requirements of HMC's for ISRO is being met from this Institute.

2. Mini Circuits Pvt. Ltd.; M/s Mini Circuits Pvt. Ltd. an industrial undertaking has been estabilished based on the knowhow and consultancy provided by the Institute. The firm is manufacturing HMC's satisfacorily and it turn over is Rs. 1.5 crore (1987.88).

(Electronic Systems Group)

LINKAGES ESTABLISHED WITH PUBLIC SECTORS/MINISTRY
(PROPOSAL IN ADVANCED STAGE/MATURED)

TABLE - I

S.No.	Description of Proposal	Funding Agency	Any other Collaborative Agency	Remarks/References
1.	2.	3.	4.	5.
1.	Design of Four Seater Solar Car	Department of Non-Conventional Energy Resources, (DNES), New Delhi.	CMERI, Durgapur, CECRI, Karatudi, NAL, Bangalore	Bid against tender No. PUR/272/SEC/88 Ref. 1.
2.	Un-interruptible Power Supply (UPS) for Ice Lining Refrigerator(ILR)	WHO and Ministry of Health, Govt. of India, New Delhi		Amount sanctioned, Project started, Ref. 2.
3.	Solar Power Packs utilizing energy efficient Inverter/ Converter for consumer and other applications	Ministry of Human Resources Development (Dept. of Education), Govt. of India, New Delhi for Literacy Mission		Ref. No.D.O.No.F.[illegible]-5/88 AE 1 Dated 24th June, 1988 Ref.3
4.	Variable Frequency AC Drives for Battery Powered Road Vehicle, Narrow Gauge Battery Powered Locomotives etc.	B.H.E.L., Bhopal	B.H.E.L., Bhopal	Ref.No.BHEL News Letter Vol.1, No.22 31st May, 1986 Ref.4

LINKAGES ESTABLISHED WITH PRIVATE SECTORS (PROPOSAL IN PIPE-LINE)

TABLE - II

S.No.	Name of Industry/ Institution	Requirements	User	Remarks/Reference
1	2	3	4	5
1.	M/s Mukand Iron & Steel Works Ltd., Thane, Bombay	1) Variable FReq. AC drives for 10 KW hoist motion in cranes. Subsequently higher power rating upto 50HP V/F AC drives can be taken for development.	Various Industries general purpose cranes.	MoM dated 22/8/1988 Ref.5.
		2) Soft Starter for Bridge drive of cranes upto 10 KW for smooth running.	- do -	- do -
2.	M/s NELCO, Andheri(E) Bombay	1) 75 KVA Transistorised Un-interruptible Power Supply(UPS)	General purpose particularly where Computers are used	MoM dated 25th August, 1988. Ref. 6.
		2) Development of work on AC drives (Project to project basis).	For application in industries.	- do -
		3) uP based PWM Generation & feedback control software for variable freq. AC drives.	- do -	- do -
		4) Hybrid Micro Circuits for Transistor base drives.	- do -	- do -

3.	M/s Kirloskar Oil Engines Ltd., Pune	1) Soft Starter for 1800 KW motor.	Cement Industry	MoM dated 18th August, 1988 Ref.7.
		2) Variable frequency AC drive for 2000HP Synchronous motor.	For propeller of Ship.	- do -
		3) Solid State AC Circuit Breaker with protection facilities.	To be used with Diesel Gen. Set.	- do -
4.	M/s Walchand Nagar Industries Ltd., Walchand Nagar, Distt. Pune	1) Variable frequency AC drives for Centrifugals.	Sugar Industry	MoM dated 20th August, 1988 Ref.8.
		2) Variable frequency AC Drives.	1. Injection Water Pump control in Sugar Industry.	- do -
			2. For ID/FD Fans in cement industry.	- do -
5.	M/s Buckau Wolf India Ltd., Pune	1) Soft Starter for Pole changing motors used in Centrifugals	Centrifugals in sugar industry	MoM dated 19th Aug. 1988 Ref.9.
		2) Variable frequency AC drives for Centrifugals in Sugar Industry.	1. - do -	- do -
			2. ID/FD fans in cement industry	- do -
6.	M/s The Simbhaoli Sugar Mills Ltd., Simbhaoli	1) Soft Starter for four speed centrifugals M/cs.	Sugar Industry	Letter dated 1st March, 1988 Ref.10.

7.	M/s Naval Science & Tech. Lab. Min. of Def., R&D Organ. Vigyan Nagar, Vishakhapatnam(AP)	1) Soft Starter for 75 KW motor 2) 5 MW electrical propulsion plant for operation off DC Supply.	Coupled to propeller of ship For main propeller of ship.	Proposal vide NSTL 370-37 dated 29th April, 1987. Ref.11 Proposal vide NSTL 1870-30/Sub/letter dated 14.5.88. Ref. 11.
8.	M/s K.G. Khosla Compressors Ltd., Delhi	1) Soft Starter for 250 HP-350 HP Squirrel Cage Motors.	To be used along-with compressor coupled motors.	MoM dated 22nd April, 1988. Ref.12.
		2) Microprocessor based control for compressors	Application with compressors for optimised operation.	- do -
		3) Microprocessor based analyser for compressors.	For measurement & testing compressor.	- do -
9.	M/s Metallurgical & Engg. Consultants (India) Ltd.(Govt. of India Enterprises) Ranchi, Bihar	1) An Inverter Set to start and run a standard 3.7 KW cage motor off a 24V battery supply	For driving an oil pump.	Letter vide D.O.No. 11ER&DW/AS/P-5192, dated June 17, 1988. Ref.13.
		2) A Controller unit to run a brushless DC machine coupled to a flywheel only off 560 VDC supply.	For driving high innertia load.	- do -

MoM - Minutes of Meetings.

LINKAGES WITH INTERNATIONAL AGENCIES
(JOINT INTERNATIONAL RESEARCH PROGRAMMES)

TABLE - III

S.No.	Description of Proposal	Funding Agency	Any other Collaborative Agency	Remarks/References
1.	2.	3.	4.	5.
1.	Microprocessor Based Switched Reluctance Drives for Transportation and Industrial Applications.	British Council U.K.	1) University of Leeds, U.K. 2) University of Nothingham	Letter dated 31st March, 1987 Ref. DEL/887/13. REf.14.
2.	100 KVA Variable Speed AC Motor Drive using GTO's for Pumping Application in Petroleum and Chemical Industry	F.F.A., Germany	University of Wuppertal, Germany	Letter dated 22nd April, 1988 Ref. 15
3.	Development of Medium Power(100HP) Variable Speed AC Motor Drives using State of Artfrom Semiconductor Switches Motors and Microprocessor Based Controls for Industrial and Transportation Application.	INDO-US Science agreement for support of research from US Held Rupee Funds.	University of Mousouri, Columbia, U.S.A.	MoM dated 31/05/1987 Ref.16

ANNEXURE-XII

CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE
PILANI (RAJASTHAN)

INTERNATIONAL COLLABORATIONS

1. UNDP Project "Advanced Technology in Semiconductor Devices" (1977-82)

In this project UNDP provided an inputs, of US $ 2,259,778 [equipment component of US $ 1,864,919,38 m/m of international consultants and 25 fellowship trainings]. The project has resulted iln the capability building in the Semicondutor Devices Area.

2. UNDP Project: Semiconductor Devices and Electronilcs Sub-systems for Transportation - 1984-88.

In the project UNDP provided an input of US $ 1687,335 (equipment component of US $ 1257, 072, 23.7 m/m of international consultant and 18 fellowship trainings).

The project has resulted in the development of following:

i) Design and development of a batch of VME bus compatible integrated circuit.

ii) Desing and development of a batch of 17 100 Amp.transistor. (300 amp. transistor in process).

iii) Design and development of a batch hybrid microcircuits for 100 Amp. and 300 Amp. transistor inverters.

iv) 20 KVA Electronics sub-systems for transportation.

3. CEERI - UCL Belgium:

Collaborative Research for the design & development of ASICs. (1988-90)

The collaborative project will be carried out jointly by the personnel of CEERI AND UCL Belgium. And under the programme, there is a provision for CEERI personnel to visit UCL and UCL to visit CEERI and work jointly for design and development of advanced ASICs.

4. CEERIKFA Collaborartive Project Development of GaAs MESFET'ss for Communication (1985-88)

This project envisages the standardisation of different processing steps involved in Gallium Arsenide MESFET technology. The project will be carried out jointly by CEERI and ITH Darmstadt, FRG. The collaboration provides for exchange & 4 Scientists from each side.

5. Collaborative Research Programme between CEERI, Pilani and Power Electronics Research Centre, University of Misscouri Columbia USA (2 years)

The Collaborative Researh work for the development of 100 HP AC motor drive for transportation & industrial applications, has been agreed to be carried out. The proposal envisages exchange of scientists and dev. of two models of the design one at CEERI and the other at Power Electronics Research Centre, Univ. of Misscouri, Columbia, USA.

The Collaborative arrangements are being worked out.

6. CEERI (CSIR) KFA

(1) R&D Cooperation between CEERI and Laboratory for Electrical Machines and Drives, University of Wuppertal, West Germany.

The Collaborative Research Work envisages Development of 100 KVA variable AC motor drive using Gate Turn off thyristers. for pumping applications in petroleum and chemical industries.

The collaborative arrangements are being worked out.

7. Collaborative Research Programme between CEERI and School of studies in Electrical & Electronics Engg. Univ. of Bradford. U.K. under MoU on S&T between UK and India (1983-86)

This project is being a carried out jointly by CEERI, Pilani IIT Delhi and IIT Kharagpur. The CEERI is carrying out (1) Test Structures and Measurement Techniques related to contact resistance in MoS LSI (ii) Characterisation and evaluation of thin diellectric films.

The assistance to CEERI for this work is of the ordr of Rs. 8.5 lakhs.

9. Collaboration between CEERI and University of California, Berkely in the area of Electron Microscopy and its applications to semiconductor Devices (1981-87)

The project was carried out at CEERI, Pilani and there was close interaction between CEERI, Pilani and Electronics Res. lab. College of Engg. univ. of California, Berkely whose Director Dr. D.J. Anglakos was the co-principal investigator. There were number of exchange visits between the two organisation.

10. Collaborative Research Programme between CEERI KFA (ITH, FRG) (4 years)

It is proposed to do advanced research in CAD tools and VLSI design in collaboration with ITH, Darmstadt, the proposal has been approved and two scientists for ITH Dermsladt visited CEERI during Sept.-Oct.,19(8.

11. Collaborative Research Programme on Dev. under MoU between UK and India (2 1/2 years)

The proposal envisage design and development of 10 KVA microprocessor based switched reluctance motor drive in British University and 30 KVA switched reluctance motor drive at CEERI.

The proposal is under active consideration.

12. Collaborative Research Programme on advanced ion-implantation Techniques for ASIC processing under Mou between UK and India (3 years)

The proposal envisages dev. of advanced ion implantation techniques for VLSI in collaboration with University/Institute in U.K.

The proposal is under active consideration.

ANNEXURE XI

List of Seminars/Symposia/Workshops etc.

S.No.	Title of Symposium/Seminar Workshop/Get-together	Period	No. of Participants
1.	First National Seminar on "Microlithography	March 11-12,1986	55
2.	The use of Semiconductor Devices and Electonic sub-systems for Transportation & Industrial Applications using Solid State A.C.Motor Drives.	April 25-26,1986	25
3.	National Seminar on "A.C. Motor Drives for Transportation and Industrial Applications".	April 15-17,1987	40
4.	National Seminar on "Process Induced Material Interactions in Electron Devices"	Sept. 21-23,1987	25
5.	National Seminar on "Microprocessor Based Electronic Systems and Application Sepecific Integrated Circuits (ASICS) for Industrial Applications	Sept. 21-23,1988	40
6.	Fifth International Workshop on Physics of Semiconductor Devices	Dec. 1989	400 expected
7.	International Conference on Power Electronics	Dec.,1989	400 expected

ANNEXURE-XIV

CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE
PILANI (RAJASTHAN)

ACTION TAKEN BY CEERI ON THE RECOMMENDATIONS OF UNDP CONSULTANTS

(16th February, 1988)

CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE PILANI (RAJASTHAN)

I. Recommendations relating organisation matters regarding UNDP Project No.IND/84/015

Prof. K.C. Saraswat,
University of Stanford,
U.S.A.

Suggestion/Recommendation	Action taken
1. Better communication with Delhi and outside world should be established at an early date to facilitate better and faster flow of information.	CEERI, Pilani & CEERI Centre, Delhi are now well linked through a dedicated High Frequency Link and the facility for Voice Communication established at a cost exceeding Rs.3.5 lakhs is now being expanded to cover digital communications. (All the above from CSIR grant)
2. In order to have quick transport of equipment and scientists working on the project, an airconditioned vehicle should be procured.	One airconditioned minibus was specially approved by DGSIR and the same has been procured. Similarly another staff car has been procured and fitted with airconditioner for use in summer months.
3. Improvement in the clean rooms and additions.	Clean rooms have been rennovated to give class 1000 cleanliness in some of the rooms. Building extensions for installation of an ion-implanter, multi-layer Hybrid microcircuits and VLSI Design Centre are under construction as per CSIR approval.

4. Electric supply stability	Since RSEB power supply is erratic, dedicated Diesel Generators and UPS are being used for all sophisticated equipments used in the VLSI laboratory (RSEB has agreed to instal a new line for feeding Pilani, including CEERI laboratory. This would improve RSEB supply also).
5. Purchase procedure to be improved ensure quick procurement.	Action taken and monthly being reviewed to remove bottlenecks. Problems with DGTD and other departments are taken up at higher level through DGSIR.
6. Better interaction between CEERI Scientists and rest of the world through participation in International Seminars/Symposia/Workshops.	Whereas during study tours as well as during fellowships maximum advantage is taken of the visits for attending international seminars etc, there are limitations on the funds available from CSIR, particularly during the current year because of draught situation and embargo put by Ministry of Finance.

UNDP PROJECT

II. Major Recommendations of UNDP Consultants and Action taken by CEERI

A. LSI/VLSI TECHNOLOGY

Observation/Recommendation	Action taken/in progress
Prof. P. Jespers, Catholic University, Lovain, Belgium.	
(a) Undoubtedly, the strength of CEERI lies in its interdisciplinary character. Whereas semiconductor houses such as SCL are geared rather on the production of high volume ICs, CEERI may exploit its expertise for the benefit of companies producing goods in which the added value of custom ICs opens new markets, like in transportation, industrial electronics, and some telecommunication problems (teletext).	Some ASICS are identified e.g. Telecommunications chip for CDOT. More are being identified for Sugar & Paper Industry. ASIC chip for 96 line Electronic Telephone Exchange has been taken up.
(b) In order to successfully bridge the gap between IC designers and system scientists, it may be highly desirable furthermore to enhance CEERI's CAD tools rapidly.	Two Micro Vax work stations procured through CSIR funds. VLSI design centre proposal was sent to DOE & sanction has been obtained. Building work for this is nearing completion and equipment is ordered. (First Training programme on VLSI is being planned in July, 1988)
(c) Long term cooperation between CEERI, Pilani and UCL, Belgium is recommended in the area of VLSI technology.	Proposal prepared and further action taken duing the visit of Project Director and followed up with CSIR. Scientists from both sides identified for further work on VLSI chips. (Record note of discussions between Director, CEERI and Director, Microelectronics Centre of UCL, Belgium signed during the former's visit is attached at Annex-A.)

B. Power Semiconductor Devices/Darlington Power Transistors

Dr. P. Rai-Chaudhury

Suggestion/Recommendation	Action taken
1. Significant progress made on the 100A Darlington Transistor, both in Design as well as processing. But following specific recommendations are made for improvement.	
(i) Super Q-system for D.I. water	Implemented
(ii) Mask Aligner to handle large Diameter wafers	Implemented
(iii) Assured source of Epitaxial Silicon wafers	Implemented
(iv) Procurement and commissioning of the Spin Etcher & Spreading resistance probe	Spin Etcher installed, other equipments are still to be properly installed by the suppliers (UNDP & CEERI are pursuing these cases).
(v) Commissioning of Denton Furnace	

2. Dr. Roulston

(i) CAD Training to be intensified	Procurement completed
(ii) BIPOLE & WATAND programmes from University of Waterloo could be obtained	Training continued

3. Prof. H.B. Assalitt

As a whole present & future facilities (being created) appear to be satisfactory

However

(i) More space is required in some areas - Photomasking, alloying etc.	Although because of resource limitation of CSIR, no major construction work could be undertaken, construction work has been initiated for (i) VLSI Design Centre, (ii) Extension to HMC Lab. and (iii) Ion Implantation facility.
(ii) Mask Aligner, Cold Weld press with dies & a Wire Bonder* may be added	* Next Phase
(iii) Quality of D.I. Water and its distribution to be streamlined	Implemented
(iv) More characterisation and testing of Transistors to be carried out	Implemented
(v) Life time control through irradiation using Electrons	This needs very large investment. It can be set up at BHEL as part of DOE funded Power Electronics Centre as National facility.

(vi) To improve switching speed of power transistor, bypass diode might have to be separated.	For 100A. done upto mask stage for 300A: it is being done.
(vii) Possibility of taking up work for GTO Thyristors after completing 300A Transistor	Being taken up in next phase.

3. Dr. H. Runge (Dec.1985)

CEERI is in an excellent position to develop 'state of art' power devices High priority should be given to 300Amp. Darlington transistor before further research is undertaken in this area. By that time it will become clear whether GTO or the Sith or any other device will be more interesting for development.	Being considered in the next phase.

4. Dr. Roulston (2nd visit)

(i) Extension of Bipole results to 300 Amp. Devices	Implemented
(ii) Simulation of RBSoA conditions on WATAND.	Implemented
(iii) Utility of emitter ballasting to be studied	being done by March/April, 1988
(iv) Study of temperature distribution under static conditions using Thermal WATAND	By March, 1988

4. **Dr. H.B. Assalitt (May 1987 visit)**

(i) Availability of packages for 100 & 300A Transistors	FPO orders placed
(ii) Satisfactory Alloying process to be evolved	work in progress

C. ELECTRONIC SYSTEMS
(MICROPROCESSOR BASED AC MOTOR DRIVES)

Suggestion/Recommendation	Action taken/being taken
1. Dr. K. Matsuse	
(i) Theoretical study of acoustic noise from induction motor & inverter to be studied. One or two scientists to be added to the group to undertake this work, since with the limited staff in this group it would not be possible to undertake this extra study.	Action taken. Two posts are advertised, one being readvetised for strengthening this group for this as well as other tasks on UNDP Project.
(ii) Joint collaborative effort to be proposed with Japanese Universities in the emerging area of A.C. motor drives for Transportation. (Dr. K.Matsuse ready for another visit)	Being considered (No communication received from Japan)
2. Dr. Richard Hoft	
(i) Detailed measurements on machine parameters with 50 Hz sinusoidal supply	Implemented
(ii) Measurement of harmonic voltages and currents on no load and full load at 5 Hz, 20 Hz & 50 Hz and comparison with theoretical values	Implemented
(iii) Distortion minimisation of PWM strategy is recommended for the optimum PWM strategy for Inverter - motor drive.	Implemented

(iv) Addition of two engineers to the Power Electronics Group.	Post advertised
(v) Purchase of following additional equipment	
(a) High current Tektrix Current Probe	FPO under process
(b) Tektronix Digital storage Oscilloscope with Multiplier	Procured
(c) Oscilloscope Camera (for recording waveforms)	Being included in the next year's budget (depending on resources being made available by CSIR).

3. Dr. T.A. Lipo

(i) Detailed studies on PWM techniques planned by the group relevant to the project and are at international level in this area.	Noted
(ii) Simulation software (ASCL) to be procured.	No action because of 'no funds.'
(iii) Final objective to be clearly defined, not necessarily to be restricted to Electric Vehicle programme. (e.g. spindle drives, dynamometer, machine tool devices etc.)	Work being extended to other types of A.C. Motor Drives (e.g. compressor drives for airconditioners etc. are taken up for development).
(iv) Addition of at least one engineer for timely completion of the project PERT chart to be prepared.	Action taken, post is readvertised. Bar Chart prepared and revised, approved by TPR in Jan. 1987.

5. It was, therefore, agreed that steps should be taken by both the organisations to process the proposals for approval of appropriate authorities so that some Application Specific Integrated Circuits of common interest to both the countries can be developed using the limited silicon foundry facilities with suitable augmentation for meeting the objectives.

6. Major milestones and phases of the research work to be carried out under this programme were also discussed and the draft proposal was suitably modified.

(copies of both proposals are attached for ready reference)

(Prof. P. Jespers)
Laboratoire de Microélectronique
Université Catholique de Louvain
1348 Louvain-la Neuve, Belgique

(Dr. G.N. Acharya)
Director, Central Electronics
Engineering Research Institute,
Pilani Rajasthan, INDIA 333031

Record Note on the Discussions regarding collaborative Research Programme for the Design and Fabrication of Industrial ASICS (Application Specific Integrated Circuits) between the Central Electronics Engineering Research Institute (CEERI), Pilani, India and Laboratoire de Microelectronique, Université Catholique de Louvain (UCL), Belgium.

June (29-30, 1987)

1. As a follow up of the recommendations made in the joint note prepared at CEERI in January 1987 during the visit of Prof. P. Jespers as UNDP consultant, a detailed proposal for the above collaborative programme was prepared by CEERI and sent to UCL, Belgium. This was discussed in detail with Prof. P. Jespers and his colleagues by Dr. G.N. Acharya, Director CEERI, during his studytour under the current UNDP project (copy attached).

2. Simultaneously draft proposal (for providing counterpart support) for Cooperative Research Programme (Convention de Coopération) in the standard proforma to be governed by the standard terms and conditions of UCL (as per conditions Generales) was prepared by Prof. P. Jespers and his colleagues. This was also discussed.

3. Main objectives of the proposal were discussed with Mrs Delcampe, Director of Cooperative Programmes (UCL) and Prof. P. Macq, Rector of the University. Considering the long terme significance and importance of the proposed collaborative R&D programme, both of them agreed in principle to support the proposal.

4. It was noted that recently the Department of Electronics of the government of India have sanctioned approximately $ 1 million dollars equivalent Indian money for setting up a VLSI Design Centre at CEERI. This may be able to provide strong support to the proposed collaborative Research programme.

ANNEXURE - XV

ACTION TAKEN ON THE MAIN RECOMMENDATIONS OF THE PAC

First PAC meeting held on 10.10.85

S.No.	Main Recommendation	Action taken and remarks
1.	Workshop may be held for familiarising the users about facilities & expertise available at CEERI, for taking up the results to production stage and for planning a larger project in a subsequent phase.	Workshop on the use of Semiconductor Devices and Electronic Subsystems for Transportation and Industrial Applications using Solid State AC Motor Drives was held during April 25-26, 1986.
2.	Dr. Kamal Hussein indicated: Potential industries may be identified for productionisation.	Action on this has been initiated and SCL has indicated their interest in the VME bus compatible interface chip for productionisation and BHEL has shown interest in manufacture of the PWM Solid State A.C. Drives for Electric Vehicles.
3.	CAD and simulation facilities should be extended to meet the requirements of the project.	Order has been placed through UNDP for CAD software and associated items (worth $ 180,000 approximately) so that the same can be run on the VAX 11/730 computer available at CEERI. The equipment has been received partly.
4.	Procurement of a suitable computer for simulation and design work for VLSI.	One VAX 730 and Micro VAX II computers have been procured under counter part funds.
5.	Development of GTO's be examined.	In a brainstorming session with UNDP consultants and CEERI scientists, the matter was thoroughly discussed and it was decided that a modified transistor design with improved surge current capabilities would be a better proposition in line with the objectives

		of the project. Furthermore, it was noted that transistor inverters are more economical and more efficient because of the lower forward drop of the transistors. Improvement in surge current capability with larger area for Darlington Transistors would be a better development objective at present. Based on these concepts the Darlington Transistors have been developed.
6.	Recruitment of additional staff for the project.	3 Scientists have been redeployed from other projects and 8 New Scientist have joined the project some of the Scientist from recent recruitments are likely to join.

Second PAC meeting held on 9th January, 1986

Recommendation		Action
1. Linkages.	i)	At the request of DOE note on the design of the signal processing microchip was sent to them for exploring possibility of productionization of the same by SCL. SCL is exploring market possibilities for this chip.
	ii)	Transfer of know-how to BHEL for the PWM AC drive system started. They have shown interest in manufacturing the microprocessor based version also whenever it is ready.
	iii)	BHEL has shown positive interest in power devices particularly 100 Amp. Darlington transistor developed by CEERI and has agreed to provide packaging facilites.
	iv)	More linkages are getting established with NELCO Mukand iron & Steel. Kirloskar KG Khola Compressor Ltd.
2. Dialogue with Railways on AC motor drives.		This has been started & specific requirements are being identified.

Third PAC meeting held on April 25th, 1936

Dr. Kamal Hussein mentioned that the dialogues with the Industry and users must be kept alive so that they are kept well informed of R&D activities and the achievements and results which they can fruitfully use. He mentioned that some concrete joint proposals should emerge. Involving active participation of CEERI and Industry.

A National Seminar on "AC Motor Drives for Transportation and Industrial Applications" was organised during April 15-17, 1987.

Linkage has been established with industries and collaborative R&D proposals are likely to emerge. (As per Tables attached).

Fourth PAC meeting held on 17th February, 1988

Preparation of draft terminal report by August, 1988	Prepared and submitted
Project Evaluation Sept. 1988	Completed
Final Tripartite Review Oct.1988	Completed
Proposal for future assistance	A detailed proposal for design and development of ASIC's for process industries has been prepared and submitted.