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17383

DP/ID/SER.A/1175
22 March 1989
ORIGINAL: ENGLISH

QUALIFICATION AND SURVEILLANCE LABORATORY FOR CONSUMER ELECTRONIC PRODUCTS

DP/CPR/85/087/11-01

THE PEOPLE'S REPUBLIC OF CHINA

Technical report: Testing of large-scale integrated circuits*

Prepared for the Government
of the People's Republic of China
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

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United Nations Industrial Development Organization
Vienna

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* This document has not been edited.

V.89 53661

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INTRODUCTION

During the period Jan. 2 through Feb. 1, 1989, I traveled to China (PRC) to conduct a seminar on at CEPREI (Chinese Electronic Products Reliability and Environmental Testing Research Institute) in Guangzhou. I arrived in Guangzhou on Jan. 6 and spent two days with the management of the Institute planning the seminar lectures and the follow on support work in their testing laboratory.

The subject of the seminar was "The Testing of LSI Integrated Circuits". During the 12 days of lecture, I covered a broad range of topics related to LSI testing. As requested, I had collected literature and specifications on commercially available IC testers and brought it with me for use in the seminar. In addition, I brought copies of numerous technical papers and commercial specifications to illustrate the lectures.

The lectures occupied 12 days, following which I spent 3 days in the CEPREI test laboratory assisting them to solve some problems with their IC tester. The interpreters during the lectures were engineers from The Institute

At the beginning and end of the trip, I had a meeting in Beijing with a UN representative. Travel to and from China from San Diego was by United Airlines. Travel within China between Beijing and Guangzhou was by CAAC.

The local arrangements in China were made by various agencies associated with the program. The Hotel accommodations were: (1) Beijing, Friendship Hotel (marginal), (2) Guangzhou, Bei Yun Hotel (barely satisfactory), (3) Beijing, Kunlun Hotel (excellent).

AGENDA

The following pages are a reproduction of the lecture notes given to the attendees.

Overview and Introductory Comments

The primary purpose of my lectures will be to impart to you the concept that the testing to be performed should be keyed to the purpose for which the tests are being performed and the problems which might be encountered or need to be uncovered. To follow this philosophy, you should not adopt a rigid test schedule but should take a flexible approach. Tests keyed to detect problems which experience and the advances in technology show no longer pose a risk, should be dropped or severely reduced, while tests keyed to newly emerging problems should be instituted.

If this philosophy is followed, there can be several significant benefits:

(1) The available testing resources can be more efficiently utilized and, as a result, more part types can be qualified and monitored with the given resources.

(2) A more effective job of qualification can be done by obsoleting old tests no longer needed and diverting the manpower and facilities to perform new tests necessitated by more advanced devices and processes.

Rigid test plans and sample sizes such as are defined in MIL 883 and IECQ can be used as useful guides and starting points but should be modified and supplemented using experience and engineering judgement.

I will present my view point of the various purposes for which testing is performed and show the tests which might be performed and some of the problems which might be addressed by each.

To effectively follow the flexible philosophy which I advocate, it is necessary for your staff to follow closely the advances in the LSI device art and the developments in Reliability Engineering. This can best be done by having staff members attend certain key conferences at which this technology is described such as the ISSCC (Feb.), IRPS (April), and ITC (Sept). In addition, you should subscribe to key technical journals such as IEEE Transactions on Reliability, Components Materials & Hybrids, and Solid State Devices, and commercial journals such as Evaluation Engineering and Electronic Test.

In addition, I will address the subject of setting up a component reliability database. This will be done by analyzing the purpose for which the data base will be kept and showing how the various files and records of the data base might be organized.

An introduction to the technical English used in discussing the multiple aspects of IC testing was given. This emphasized the terminology relating to reliability and quality issues.

The following is a copy of the lecture notes used. They were prepared in outline form to assist the Chinese speaking audience in following the lectures.

Day 1

1.0 TESTS PERFORMED DETERMINED BY PURPOSE OF TEST

1.1 QUALIFICATION TESTING

PURPOSE: TO IDENTIFY FLAWS IN THE DEVICE AND PACKAGE DESIGN AND MANUFACTURING PROCESSES WHICH PREVENT THE PART FROM MEETING THE MECHANICAL, ELECTRICAL, RELIABILITY, OR QUALITY SPECIFICATIONS WHEN USED IN AN APPLICATION.

1.2 INCOMING INSPECTION TO PURCHASE SPECIFICATION

PURPOSE; TO DETERMINE THAT ANY LOT OF PARTS MEETS THE ELECTRICAL AND MECHANICAL ASPECTS OF THE PURCHASE SPECIFICATION.

1.3 EVALUATION OF QUALIFICATION RESTRICTIONS

PURPOSE: TO ASSURE THAT A LOT OF PARTS ADHERES TO ANY RESTRICTIONS WHICH WERE PLACED ON THE CONFIGURATION OF THE PART AS PART OF THE QUALIFICATION PROCESS.

1.4 RELIABILITY EVALUATION

PURPOSE: TO IDENTIFY THE INHERENT RELIABILITY OF A POPULATION OF PARTS IN TERMS OF ITS MTBF AND MTBE.

1.5 INCOMING QUALITY EVALUATION

PURPOSE: TO IDENTIFY THE INCOMING LOT DEFECT LEVEL IN TERMS OF PPM DEFECTS USING ALL AVAILABLE DATA.

1.6 FAILURE ANALYSIS

PURPOSE: TO IDENTIFY THE MODE OF FAILURE OF A FAILED PART, AND USING THE RESULTS, IDENTIFY THE PHYSICAL LOCATION OF THE FAILURE FOR USE IS SUBSEQUENT AUTOPSY TO IDENTIFY THE FAILURE MECHANISM.

Day 2

2.0 PERFORM QUALIFICATION TESTING

2.1 ELECTRICAL PARAMETRIC & FUNCTIONAL

2.1.1 FUNCTIONAL
TEST WITH RELAXED VOLTAGE AND TIMING

LOGIC
COMPLETE VECTOR SET NEEDED

MEMORY
ADDRESS UNIQUENESS PATTERN

2.1.2 DC PARAMETRIC

2.1.2.1 CONTINUITY
WIRE BOND INTEGRITY
TEST SOCKET CONTACT

2.1.2.2 LEAKAGE
TEST AT TEMPERATURE
INPUT DEVICE INTEGRITY
CONTAMINATION FREE PROCESS
NO ESD DAMAGE

2.1.2.3 POWER SUPPLY DRAIN (ICC)
PROCESS WITHIN CONTROL LIMITS
CORRECT DEVICE SHIPPED
- CMOS and DYNAMIC LOGIC NMOS REQUIRE DYNAMIC OPERATION
- WORST CASE AT LOW TEMPERATURE

2.1.2.4 OUTPUT LEVELS (VOH & VOL)
PROCESS WITHIN CONTROL LIMITS
- SIMPLE PATTERN OR VECTOR
- WORST CASE INPUT LEVELS
- WORST CASE VCC (VEE)

2.1.3 FUNCTIONAL
TEST WITH RELAXED VOLTAGE AND TIMING

2.1.3.1 LOGIC
COMPLETE VECTOR SET NEEDED

2.1.3.2 MEMORY
ADDRESS UNIQUENESS PATTERN

2.1.4 AC PARAMETRIC
TEST WITH WORST CASE VOLTAGE, TIMING, AND TEMPERATURE

2.1.4.1 LOGIC
IDENTIFY MAXIMUM DELAY PATH
GENERATE VECTORS TO EXERCISE PATH
MEASURE DELAY

2.1.4.2 MEMORY
ADDRESS UNIQUENESS PATTERN
WORST CASE DISTURB PATTERN

2.2 MECHANICAL DIMENSIONAL

2.2.1 LEAD DIMENSIONS
CRITICAL ON THROUGH HOLE PARTS
LESS CRITICAL ON SURFACE MOUNT PARTS

2.2.2 LEAD PLACEMENT
CRITICAL ON ALL PARTS
INFLUENCES MANUFACTURING ASSEMBLY YIELD
SURFACE MOUNT - CONTACT INTEGRITY AND SOLDER BRIDGING
THROUGH HOLE - LEAD CRUNCHING

2.2.2.1 SURFACE MOUNT
CO-PLANARITY
CONTACT PATTERN

2.2.2.2 THROUGH HOLE
LEAD ANGLE
BENT LEADS

2.3 LEAD FRAME MATERIAL & COATING

2.3.1 LEAD MATERIAL CHARACTERISTICS
HARDNESS CONTROL RESISTANCE TO BENDING

2.3.1.1 ALLOY 42 HARD ENOUGH TO RESIST BENDING

2.3.1.2 COPPER ALLOY HARDNESS DEPENDENT ON HEAT TREATING
HARDNESS MUST BE CHECKED

2.3.2 LEAD COATING INFLUENCE SOLDERABILITY
MUST BE CHECKED FOR SOLDERABILITY
OFTEN TENDENCY TO FORM SURFACE CORROSION WHICH INHIBIT SOLDERABILITY
MUST BE CAUTIOUS OF LOTS OF OLD MATERIAL, GREATER THAN 6 MONTHS OLD

2.3.2.1 TIN PLATING
UNIFORM COATING BUT NOT COMMON TODAY

2.3.2.2 SOLDER
PLATED
UNIFORM THICKNESS, MUST CHECK THICKNESS
HOT DIPPED
OFTEN EXCESSIVE BUILD UP, CAUSES PROBLEMS
THICKNESS MUST BE CHECKED

2.3.2.3 LEAD COATING THICKNESS EFFECT INSERTABILITY
EXCESSIVE BUILD UP CAN MAKE DIFFICULT TO INSERT
EXCESSIVE BUILD UP OF SOLDER CAN DAMAGE SOCKET
SHOULD NOT ACCEPT SOLDER DIPPED PARTS FOR APPLICATIONS WHICH MUST BE SOCKETED.
THE FIRST INSERTION IS OK, SOCKET CONTACT BECOMES BENT AND NEXT INSERTION MAY NOT BE GOOD.

Day 3

2.4 PACKAGE INTEGRITY TESTS

2.4.1 THERMAL STRESS
DETERMINES THERMAL MATCH OF PACKAGE COMPONENTS AND DIE

2.4.1.1 THERMAL SHOCK (LIQUID TO LIQUID)

2.4.1.2 TEMPERATURE CYCLE (AIR TO AIR)

2.4.1.3 SOLDER SHOCK (THROUGH HOLE)

2.4.1.4 SOLDER REFLOW (SURFACE MOUNT)

2.4.2 LEAD BEND TESTS
IDENTIFIES BRITTLE LEADS

2.4.3 TORQUE TEST
FOR CDIP PACKAGE
MEASURES STRENGTH OF SEALING GLASS
CRITICAL WITH VITREOUS GLASSES
APPLY FIXED TORQUE, MEASURE HERMETICITY

2.4.4 HERMETICITY
CAVITY PACKAGE

FINE LEAK
He LEAK RATE 10exp-7
GROSS LEAK
BUBBLE TEST

2.4.5 AUTOMATIC INSERTION
MEASURES ABILITY OF PACKAGE TO WITHSTAND SHOCK OF AUTOMATIC INSERTION
AUTO-INSERT PARTS, THEN MEASURE HERMETICITY

2.4.6 DIE ATTACH INTEGRITY
DETECT VOIDS IN DIE ATTACH
CAUSE LOCAL HIGH THERMAL RESISTANCE AND HOT SPOTS
UNEVEN STRESS CAN CAUSE DIE CRACKING
2.4.6.1 THERMAL SIGNATURE
2.4.6.2 XRAY
2.4.6.3 DIE SHEAR

Day 4

2.5 ENVIRONMENTAL STRESS TESTS

2.5.1 HIGH TEMP DYNAMIC OPERATING LIFE (HTDOL)

2.5.2 HIGH TEMP STEADY STATE LIFE (HTSSL)

2.5.3 HIGH TEMP STORAGE (HTS)

2.5.4 PRESSURE COOKER (PC)

2.5.5 BIASED TEMPERATURE HUMIDITY (BTH)
2.5.5.1 85/85
2.5.5.2 BPC
2.5.5.3 HAST
2.5.5.4 PCTH

2.6 DIE RELATED TESTS

2.6.1 LTDOL, LOW TEMPERATURE DYNAMIC OPERATING LIFE
TEST FOR HOT CARRIER INJECTION

2.6.2 ALPHA PARTICLE SENSITIVITY TESTS
EVALUATES MEMORY SUSCEPTIBILITY TO SOFT ERRORS

2.6.3 PASSIVATION INTEGRITY TESTS
INDICATES POTENTIAL MOISTURE CORROSION PROBLEMS
ACID ETCH TECHNIQUE
SODIUM CONTAMINATION TECHNIQUE FOR MEMORY

2.6.4 ESD

2.6.5 CHARGED HUMAN MODEL
SIMULATES HUMAN HANDLING PROBLEMS
MIL 883 STANDARD TEST METHOD
1500 OHM, 100 pF

2.6.6 CHARGED DEVICE MODEL
SIMULATES MACHINE HANDLING PROBLEMS
NOT STANDARDIZED
0 OHM, 30 pF

2.7 PURPOSE OF VARIOUS TESTS
EACH TEST KEYED TO UNCOVER SPECIFIC DEVICE OR PROCESS FLAWS

HTOL
LTDOL
HTS
BTH
PC
THERMAL STRESS
HERMITICITY
TORQUE
ESD

Day 5

3.0 TEST TO PURCHASE SPECIFICATION
IDENTIFY DAMAGED PARTS
TEST CORRELATION PROBLEMS
TEST ESCAPES
EARLY LIFE FAILURES
LTPD SAMPLE TEST PREFERABLE TO 100% TEST

3.1 ELECTRICAL FUNCTIONAL & PARAMETRIC
IF POSSIBLE, TEST AT WORST CASE TEMPERATURE
BIN REJECTS FOR REJECT MODE
USE TEMPERATURE ADJUSTED TO COMPENSATE FOR OPERATIONAL JUNCTION HEATING

3.1.1 DC PARAMETRIC

3.1.1.1 CONTINUITY
RETEST CONTINUITY REJECTS

3.1.1.2 LEAKAGE
POWER SUPPLY CURRENT
USE TEMPERATURE CORRELATED TEST LIMIT

3.1.1.3 OUTPUT LEVELS, VOH, VOL
TEST WITH SPECIFICATION LOAD

3.1.2 FUNCTIONAL

3.1.2.1 MEMORY, ALGORITHMIC PATTERN TEST
DISTURB REFRESH TEST

3.1.2.2 LOGIC, VECTOR STREAM OR SCAN LOGIC REGISTER

3.1.3 AC PARAMETRIC

3.1.3.1 MEMORY, DISTURB PATTERN

3.1.3.2 LOGIC, FULL VECTOR SET PLUS MAXIMUM PATH DELAY

3.1.4 MECHANICAL DIMENSIONAL

3.1.4.1 BODY DIMENSION
CHECK ONLY OCCASIONALLY

3.1.4.2 LEAD DIMENSION & PLACEMENT
SAMPLE TEST EVERY LOT FOR BENT LEADS

4.0 EVALUATE TO QUALIFICATION RESTRICTIONS
TO INSURE THAT MANUFACTURER IS SHIPPING PART CONFIGURATION ORIGINALLY AGREED TO
NOT APPLICABLE TO MANY PARTS, COMMODITY PARTS
APPLY TO MEMORY, MICROPROCESSOR, GATE ARRAYS, CRITICAL PARTS

4.1 PACKAGE MARKINGS
VERIFY THAT MARKING CORRECT AND COMPLETE
MAINTAIN BOOK OF REQUIRED AND APPROVED MARKINGS

4.2 DEVICE CONFIGURATION

4.3 DIE REVISION LEVEL
CHECK PACKAGE MARKING
OCCASIONALLY OPEN PACKAGE AND CHECK DIE REVISION

4.4 PACKAGE MATERIALS AND DESIGN REVISION

4.4.1 LEAD FRAME MATERIAL
USE MAGNET TEST FOR A-42

4.4.2 LEAD COATING
USE VISUAL OBSERVATION AND BETA-SCOPE

4.4.3 MOLDING COMPOUND
CHECK PACKAGE MARKING

4.4.4 DIE ATTACH MATERIAL & PROCESS
OCCASIONAL DESTRUCTIVE PHYSICAL ANALYSIS (DPA) TO CHECK
ONLY FOR PARTS WHERE CRITICAL

Day 6

5.0 EVALUATE RELIABILITY
RELIABILITY IS STATISTICAL PROPERTY OF A POPULATION OF PARTS
RELIABILITY WHICH IS VERIFIED IS DEPENDENT ON DATA AVAILABLE
USER AND MANUFACTURER CONTRIBUTE DATA

5.1 USE ACCELERATED TEST METHODS
PERFORM FAILURE ANALYSIS OF ALL FAILURES
DETERMINE FAILURE MECHANISM

5.2 TEMPERATURE ACCELERATION (ACCELERATION TABLE)
ARRHENIUS MODEL
RATE OF OCCURRENCE OF CHEMICAL REACTIONS
DEPENDENT ON EXP. OF 1/TEMPERATURE AND ACTIVATION ENERGY

5.3 VOLTAGE ACCELERATION
CROOKS MODEL
TIME DEPENDENT VOLTAGE BREAKDOWN
FUNCTION OF VOLTAGE STRESS ON DIELECTRIC (MV/Cm)
DEPENDENT ON EXP. OF VOLTAGE IN EXCESS OF NORMAL OPERATING VOLTAGE

5.4 COLLECT DATA AT VARIOUS TIMES DURING TEST

5.4.1 EARLY READ POINT, 168 HOURS
DETERMINE INFANT MORTALITY

5.4.2 LATER READ POINTS, 500, 1000, 2000, 5000 HOURS
DETERMINE ADULT LIFE FAILURE RATE

5.5 SET UP RELIABILITY MONITOR PROGRAM

5.5.1 WEEKLY SAMPLES FROM PRODUCTION, TEST TO 168 HOURS

5.5.2 CONTINUE PORTION OF PARTS TO 1000 HOURS (1/6)

5.5.3 CONTINUE PORTION TO 2000 HOURS (1/3)

5.5.4 CONTINUE PORTION TO 5000 HOURS (1/3)

5.6 USE STATISTICAL TECHNIQUES TO EVALUATE DATA (THORNDYKE CHART)

5.6.1 USE CHI SQUARED STATISTICAL TABLES (EVENT TIME/MTBF RATIO TABLE)

5.6.2 DETERMINE CONFIDENCE LEVEL DESIRED
60% AND 90% COMMONLY USED

5.6.3 RELIABILITY VERIFIED NORMALLY LIMITED BY DATA AVAILABLE

5.6.4 CALCULATE EFFECTIVE TEST HOURS
CLOCK HOURS TIMES ACCELERATION FACTOR

5.6.5 ACCELERATION FACTOR DEPENDENT ON FAILURE MECHANISM(S)
ACTIVATION ENERGY

5.6.6 IF NO FAILURES, MUST ASSUME FAILURE MECHANISM AND ACTIVATION ENERGY (Ea)
LOW Ea MOST PESSIMISTIC
RESULTS IN LOWER ACCELERATION FACTOR
REDUCED EFFECTIVE TEST HOURS

5.6.7 IF ONE FAILURE MECHANISM, COMBINE DATA AND CALCULATE FAILURE RATE

5.6.8 IF MULTIPLE FAILURE MECHANISMS, CALCULATE FAILURE RATE FOR INDIVIDUAL MECHANISMS AND SUM RESULTS

5.6.9 CANNOT USE AVERAGE ACTIVATION ENERGY

5.7 REVIEW VENDOR'S RELIABILITY MONITOR DATA

5.7.1 CHECK TEST DATA

5.7.1.1 SAMPLE SIZE
5.7.1.2 TEST TIME
5.7.1.3 NUMBER OF FAILURES
5.7.1.4 FAILURE ANALYSIS RESULTS
5.7.1.5 LOOK FOR CHANGED SAMPLE SIZE WITH NO EXPLANATION
5.7.1.6 CHECK PRE-CONDITIONING OF TEST LOT
5.7.1.7 CHECK RELIABILITY CALCULATIONS
5.7.1.8 ASSUMED ACTIVATION ENERGY
5.7.1.9 ACCELERATION FACTOR(S)
5.7.1.10 METHOD OF ACCOMMODATING MULTIPLE FAILURE MECHANISMS
5.7.1.11 CONFIDENCE FACTOR ASSUMED
5.7.1.12 TEMPERATURE FOR RELIABILITY CALCULATION
5.7.1.13 WERE CALCULATIONS COMPENSATED FOR JUNCTION TEMPERATURE RISE

5.8 REVIEW MANUFACTURERS BURN-IN EFFECTIVENESS MONITOR PROGRAM

5.8.1 PERIODICALLY SUBJECT LOT TO SECOND B-I CYCLE

5.8.2 IF ADDITIONAL FAILURES DETECTED, B-I CYCLE NOT EFFECTIVE

5.8.3 PLOT FAILURES ON FAILURE DISTRIBUTION PAPER
LOG NORMAL
WEIBULL

5.8.4 IDENTIFY SEPARATE FAILURE POPULATIONS

5.9 BURN IN & INFANT MORTALITY

5.9.1 CALCULATED FROM FIRST READ DATA POINT (168 HRS)

5.9.2 STATED AS PERCENTAGE OF POPULATION

5.9.3 SHOULD BE LESS THAN 0.1% FOR BURNED-IN PARTS

5.9.4 DETERMINED BY BURN-IN FALL OUT FOR RAW PARTS

5.9.5 BURN-IN FALL OUT GREATER THAN 0.5% INDICATES PROBLEM WITH PROCESS

5.10 ADULT LIFE RELIABILITY
CALCULATE VERIFIED FAILURE RATE FOR (1) TOTAL TEST TIME AND (2) FOR TEST TIME AFTER FIRST READ POINT.

5.11 MEMORY SOFT ERROR RATE
DETERMINE REQUIREMENTS FOR OPERATING VOLTAGE AND FREQUENCY

5.11.1 REQUIRES REAL TIME ERROR DATA WITH PARTS OPERATED WITHIN SPECIFICATION LIMITS

5.11.2 ACCELERATE SLIGHTLY BY OPERATING AT MINIMUM SPEC. VCC

5.11.3 ACCELERATE BY OPERATING AT HIGHEST POSSIBLE FREQUENCY

5.12 MEASURE MEMORY DEVICE ALPHA PARTICLE SENSITIVITY

5.12.1 REQUIRES UNCOATED PARTS

5.12.2 ACCELERATED ALPHA PARTICLE SOURCE AND SPEC

5.12.3 ONLY NECESSARY IF REAL TIME SER DATA INDICATES PROBLEM

5.12.4 REQUIRES SPECIALIZED TEST EQUIPMENT

5.13 MONITOR FIELD FAILURE DATA

5.13.1 ATTEMPT TO COLLECT FIELD FAILURE PARTS

5.13.2 GET DATA ON OPERATING CONDITIONS, TIME OF FAILURE, SIZE OF FIELD POPULATION

6.0 EVALUATE QUALITY LEVEL
DEFECT LEVEL
UNIFORMITY
IDENTIFY NEEDS OF USER FACTORIES

6.1 ESTABLISH DEFECT LEVEL MONITOR PROGRAM
SEPARATE MECHANICAL AND ELECTRICAL DATA

6.1.1 REVIEW SUPPLIER'S QUALITY MONITOR DATA
LTPD OR AQL SAMPLE PLAN

6.1.2 DETERMINE PURPOSE FOR PROGRAM

6.1.3 REVIEW DATA FOR SIGNIFICANCE

6.2 PROCESS UNIFORMITY TEST PROGRAM (SPC TEST SPECIFICATION)
TEST PROCESS VARIABLE PARAMETERS
READ AND RECORD VARIABLES DATA

6.2.1 LEAKAGE

6.2.2 ICC

6.2.3 MOS INPUT BV

6.2.4 TIME DELAY

6.3 PERFORM INCOMING LOT SAMPLE INSPECTION

6.3.1 LTPD SAMPLE PLAN

6.3.2 LEAD POSITION

6.3.3 ELECTRICAL TEST

6.4 ANALYZE REJECTS
IDENTIFY PROBLEM

6.4.1 TEST ESCAPES

6.4.2 TEST CORRELATION PROBLEM

6.4.3 ESD DAMAGE

6.4.4 INFANT MORTALITY

6.4.5 LEADS BENT FROM MANUAL HANDLING

6.4.6 MACHINE HANDLING PROBLEMS

6.5 MONITOR USERS TEST REJECT DATA

6.5.1 COLLECT FACTORY REJECT DATA

6.5.2 FIELD FAILURE DATA

6.5.3 ANALYZE FIELD DATA

Day 7

7.0 FAILURE ANALYSIS TESTING

7.1 DETERMINE FAILURE MODE
LEAKAGE
DEAD IC
LOW ICC
HIGH ICC
OUTPUT LEVEL
CRITICAL FOR ECL

7.1.1 FOR MEMORY: ROW, COLUMN, CELL OR LARGER GROUP

7.1.2 FOR LOGIC: STUCK AT, COUPLED, OR OPEN FAULT

7.1.3 FOR ANALOG: GAIN, OFFSET, OR OTHER

7.2 ISOLATE PHYSICAL LOCATION OF FAULT
CELL MAP & BIT MAPPED GRAPHICS (MEMORY)
FAULT VECTOR ANALYSIS (LOGIC)
?? (ANALOG)

7.3 IDENTIFY FAILURE MECHANISM

7.3.1 CONTAMINATION

7.3.1.1 LEAKAGE
7.3.1.2 THRESHOLD SHIFT

7.3.2 JUNCTION FAULT OR BREAKDOWN

7.3.3 OXIDE BREAKDOWN

7.3.4 METAL MIGRATION

7.3.5 CHARGE TRAPPING
THRESHOLD SHIFT

7.3.6 CORROSION
7.3.6.1 ELECTROLYTIC
7.3.6.2 CHEMICAL

7.3.7 PACKAGE AND INTERCONNECT FAILURE

7.4 IDENTIFY CAUSE OF FAILURE

7.4.1 ESD

7.4.1.1 RUPTURED OXIDE

7.4.1.2 DESTROYED METAL

7.4.1.3 CHARGE INJECTION

7.4.2 EOS

7.4.2.1 ESD ON POWER TERMINALS
7.4.2.2 INTERNAL AVALANCHE BREAKDOWN

7.4.3 TEMPERATURE ACCELERATED ARRHENIUS FAILURE

7.4.3.1 CONTAMINATION
7.4.3.2 METAL MIGRATION
7.4.3.3 CHARGE LEAKAGE (EPROM)
7.4.3.4 OXIDE BREAKDOWN
7.4.3.5 Au/Si INTERMETALIC GROWTH

7.4.4 VOLTAGE ACCELERATED
TIME DEPENDENT DIELECTRIC BREAKDOWN

7.4.5 METAL CORROSION

7.4.5.1 CHEMICAL
7.4.5.2 ELECTROLYTIC

Day 8

8.0 FUNCTIONALITY TESTING
BECOMING INCREASINGLY DIFFICULT AS DEVICE SIZES INCREASE.
PROBLEMS WITH FAULT COVERAGE AND TEST TIME

8.1 MEMORY DEVICES (JEDEC 21-B TEST MODE) (MEMORY TEST ARTICLE)
TEST TIME PRIMARY PROBLEM
SITUATION IMPROVED BY USE OF BUILT IN TEST MODE CIRCUITRY
CONTROLLED AS DEFINED IN JEDEC STD. 21-B, BUILT IN TEST MODE CONTROL.

8.2 LOGIC DEVICES (IEEE P1149 MINUTES 'SCAN REGISTER ARTICLE)
FAULT COVERAGE PRIMARY PROBLEM
SITUATION IMPROVED BY BUILT IN SCAN REGISTERS AND IMPLEMENTATION OF IEEE P1149 TESTABILITY STANDARD

9.0 TESTING FOR VARIABLES OR ATTRIBUTES

9.1 VARIABLES TESTING, QUALIFICATION TESTING
TEST USING PMU, TMU, OR ITERATIVE SEARCH ROUTINE

9.1.1 LEAKAGE

9.1.2 OUTPUT LEVEL

9.1.1.1 OUTPUT TIME DELAY

9.1.1.2 CRITICAL INPUT TIME

9.1.1.3 STATISTICAL PROCESS CONTROL TESTING

9.2 ATTRIBUTES TESTING, NORMAL INSPECTION

9.2.1 LOGIC TRUE/FALSE AT TIME
9.2.2 LEAKAGE OR CURRENT OUTSIDE DEFINED LIMIT(S)

9.2.3 VOLTAGE OUTSIDE DEFINED LIMIT(S)

Day 9

10.0 TESTER CALIBRATION
BUILT IN TEST STANDARDS, VOLTAGE AND TIME
SOFTWARE CALIBRATION PROGRAMS
CALIBRATION NORMALLY FULLY AUTOMATIC

10.1 FREQUENCY OF CALIBRATION

10.1.1 PERIODIC FULL CALIBRATION
WEEKLY OR AS NEEDED

10.1.2 FULL CALIBRATION AFTER SHUTDOWN
ALLOW FULL WARMUP BEFORE CALIBRATION

10.1.3 DAILY QUICK CHECK OF CALIBRATION

10.2 PMU
10.2.1 VOLTAGE
10.2.2 CURRENT

10.3 TMU
10.3.1 TIME DELAY
10.3.2 FREQUENCY

10.4 PIN ELECTRONICS

10.4.1 INPUT VOLTAGE
STABLE SIGNAL LEVEL

10.4.2 INPUT TIME
TIME FOR CROSSING SPECIFIC VOLTAGE LEVEL

10.4.3 TRANSITION TIME

10.4.4 SENSOR VOLTAGE
REFERENCE VOLTAGE INTO HIGH SPEED COMPARATOR

10.4.5 SENSOR TIME

10.4.5.1 EDGE STROBE
10.4.5.2 WINDOW STROBE

10.5 PROBLEMS WITH CALIBRATION

10.5.1 INPUT SIGNAL CORNER WAVEFORM

OVERSHOOT AND OTHER SIGNAL DISTORTIONS

10.5.2 VOLTAGE LEVEL FOR TIME DEFINITION
NOT ALWAYS MATCH DEVICE SPECIFICATION

10.5.3 COUPLING BETWEEN PE CHANNELS CAUSES TIME DISTORTION

10.5.4 DUT CAPACITY LOADS DRIVER
INCREASES TRANSITION TIME

10.5.5 TRANSMISSION LINES HAVE REFLECTIONS
REQUIRE CAREFUL IMPEDANCE MATCHING
DRIVERS NORMALLY SERIES TERMINATED

10.5.6 DUT CANNOT DRIVE TRANSMISSION LINE
SERIOUS REFLECTION PROBLEMS
NEED SENSOR AT DUT WITHOUT TRANSMISSION LINE

10.5.7 DUT OUTPUT LOAD LOADS DRIVER IMPEDANCE
CAUSES LEVEL ATTENUATION

10.5.8 SENSOR CAPACITY LOADS DUT OUTPUT
ALTERS OUTPUT TRANSITION TIME

Day 10

On this day, we reviewed, in detail, the specifications of a number of IC testers which are currently available on the marker. These specifications and other literature were left with CEPREI for their reference.

Day 11

11.0 COMPONENT RELIABILITY & QUALITY DATA BASE
USING RELATIONAL DATA BASE SYSTEM, ESTABLISH RECORDS FOR VARIOUS ASPECTS OF DEVICE INFORMATION.

11.1 DEVICE RECORD WITH KEY DEVICE ATTRIBUTES

PART NUMBER
MANUFACTURER
REVISION LEVEL
INDUSTRY PART DESIGNATOR
PART CLASS DESIGNATOR
PROCESS DESIGNATOR

11.2 INCOMING LOT RECORD WITH KEY LOT ATTRIBUTES

LOT DESIGNATOR
DEVICE DESIGNATOR
PART NUMBER
MANUFACTURER
TIME OF MANUFACTURE
LOT SIZE
LOT YIELD OR SAMPLE TEST RESULTS

11.3 MANUFACTURING LOT YIELD

LOT DESIGNATOR
LOT SIZE
REJECT NUMBER

11.4 FIELD FAILURE RECORD

FAILURE DESIGNATOR
PART NUMBER
MANUFACTURER
APPLICATION CODE
ORIGINAL RECEIVING LOT DESIGNATOR
TIME OF FAILURE
FAILURE ANALYSIS RESULT

11.5 RELIABILITY TEST RECORD WITH KEY TEST INFORMATION

TEST LOT IDENTIFIER
LOT NUMBER
PART NUMBER
MANUFACTURER
REVISION LEVEL
TEST LOT SIZE
TEST HOURS
TEST CONDITIONS
TEMPERATURE
VOLTAGE
TEST TYPE
NUMBER OF FAILURES

11.6 FAILURE INFORMATION RECORD

11.6.1 TEST LOT IDENTIFIER
LOT NUMBER
PART NUMBER
MANUFACTURER
REVISION LEVEL
11.6.2 FAILURE MODE
11.6.3 FAILURE MECHANISM
11.6.4 TIME OF FAILURE
11.6.5 DESIGNATED ACCELERATION CONSTANTS
11.6.5.1 TEMPERATURE
11.6.5.2 VOLTAGE
11.6.5.3 HUMIDITY

Day 12

On the last day, I described the broad aspects of Component Engineering as it is practiced in the USA.

COMPONENT ENGINEERING is a series of engineering disciplines related to the use, selection, evaluation, specification, vendor selection, qualification, reliability, and quality of electronic components

USER RELATED COMPONENT ENGINEERING CONSULTATION TASKS

COMPONENT SELECTION

To select the most cost effective components to satisfy the needs of your system design.

COMPONENT SPECIFICATIONS

To write specifications which adequately define to Engineering, Purchasing, and the Vendors the electrical and mechanical properties of the components which you need.

COMPONENT QUALIFICATION

To develop and implement the criteria to be used to approve any vendor as a supplier of parts for use in your systems.

COMPONENT QUALITY

To establish criteria for acceptability and incoming defect levels which will insure high production yield with regard to purchased components.

COMPONENT TEST AND INSPECTION

To develop methods for test and inspection to insure that the parts which you purchase meet the specifications and will satisfy your system requirements and which are consistent with your resources.

VENDOR SELECTION

To evaluate the characteristics, reliability, and quality of a Vendor as a potential supplier of purchased components.

VENDOR QUALIFICATION

To develop and implement standards and criteria for approving a specific vendor as a supplier of a part or family of parts relying heavily on vendor supplied data.

VENDOR INTERFACE

To interface directly with Vendor Sales and Engineering representatives to assist Design Engineering is making the best possible choice of components for a specific design requirement.

SYSTEM WORST CASE DESIGN

To assist the System Design Engineers in developing satisfactory design rules to insure that all components will fulfill their requirement in the system to end of life.

SYSTEM DESIGN REVIEW

To lead a team of Engineers in performing an exhaustive design review of all products before release to insure that the system will meet the performance and reliability goals before the system is released to production.

RELIABILITY PREDICTION

To perform a reliability analysis of a system to predict its failure rates based on known or predictable failure rate characteristics of the components.

FAILURE ANALYSIS

To perform tests to determine the mode of failure of failed parts and to work with a failure analysis laboratory to identify the mechanism of the failure.

COMPONENT DATABASE DESIGN AND IMPLEMENTATION

To work with MIS and other interested parties to design and implement a computerized relational data base which allows you to maintain complete and accessible records of all components used in your systems and the qualified suppliers for each one.

COMPONENT DOCUMENTATION SYSTEMS

To assist in developing a documentation system which satisfies your needs for generating and controlling the documents which are needed to describe and control your components.

MANUFACTURER RELATED COMPONENT ENGINEERING CONSULTATION TASKS

DEVICE FUNCTIONAL CHARACTERISTICS

To assist in producing marketable devices by providing guidance regarding the functional characteristics which are needed by various classes of customer. To perform a design review of your functional specifications to insure that needed features have not been overlooked.

DEVICE SPECIFICATIONS

To guide in preparing device performance specifications to insure that all parameters which are essential to the control of the device are properly specified.

DEVICE QUALIFICATION TESTING

To assist in developing a qualification test plan which will confirm that the devices produced meet the defined reliability goals, and to present this information to customers in a way that will allow them to develop confidence in you as a Vendor.

ONGOING RELIABILITY MONITORING PROGRAMS

To assist in developing an ongoing reliability monitor test program which will monitor your product and provide reliability backup data for your customers.

FACTORY QUALITY & RELIABILITY PROGRAM REVIEW

To review the ongoing factory reliability and quality programs and the interface with these programs provided to customers with the idea of making recommendations which will improve the Vendor/Customer relationship.

CUSTOMER MARKETING INTERFACE

To assist in presenting your products and their characteristics to your customers in a convincing way.

CUSTOMER APPLICATION SUPPORT

To assist in interpreting the customers needs and problems so that you can most effectively satisfy his requirements.

OBSERVATIONS

The Chinese Engineers seem to be technically isolated. They do not seem to have access to the current literature on ICs and their reliability and quality. I could never iddentify as member of the IEEE which is the primary channel of communication on these subjects. Their isolation has prevented them from having a good grasp of current technical English. This caused some problems in communication during the lectures.

I received a strong impression that they do not understand the full seriousness of the problems associated with ESD. They profess to understand, but their actions belie this. I saw no positive steps to control ESD. There was an occasional ground strap, but I never saw an operator or engineer connect to it. It may be that the devices with which they have worked to date are rugged and are immune to ESD. This will not be so as they go to LSI devices. They are bound to have trouble in the future if no changes are made.

Following the lectures, I spent several days in the CEPREI test laboratory assisting them with several problems relating to their Gen Rad 1732 IC tester. The problems proved to be related to calibration. Calibration is done on a 6 month schedule by another department. When it was checked, the machine proved to be out of calibration on one parameter which is not adjustable. The only solution is to repair the board in question. This sort of problem presents them with significant difficulty as they do not seem to have adequate communication with the manufacturer. Another problem was that they had experienced failures while following calibration procedures. In addition, it is possible that they do not have an adequate budget for proper maintenance of the equipment. I received the impression that they do not fully understand the specifications and subtle characteristics of the testers. This problem will be exacerbated when they acquire testers which are capable of testing LSI devices. Dramatic changes in training and in calibration and maintenance organization and procedures will be required if they are to be successful in using the new testers.

RECOMMENDATIONS

As a result of my tour of the facilities and the time spent lecturing and in the test laboratory, I have made several recommendations for enhancements and changes which I believe can improve their operations. They are:

(1) The Institute seems to be technically isolated from the rest of the world. This system could be greatly improved by giving them an IEEE membership. The technical journals provided by that organization could greatly enhance there knowledge of the current state of the electronic art.

In addition, there are three technical conferences sponsored by the IEEE to which they should send a representative. They are: (1) International Solid State Circuits Conference (ISSCC) Feb., (2) International Reliability Physics Symposium (IRPS) April, (3) International Test Conference (ITC) August or September. If a representative can not be sent to the conferences, copies of the proceedings should be obtained.

(2) An attempt should be made to obtain subscription to several of the commercial technical magazines published in America.

(3) The Institute needs a regular Consulting technical contact in America. This would be someone who can obtain literature, contact manufacturers, and act as a general contact and communication link for them with the electronics industry. This would not be expensive or time consuming but would require a minor budget to support communication costs.

(4) Perform calibration of all IC testers on a monthly schedule and keep written records of the state of calibration of the machine at each calibration. This can be used to extend or shorten the calibration interval as needed. In addition, the operations personnel should obtain a copy of the calibration tapes and perform weekly checks of the calibration to improve their confidence that the machine is satisfactory.

(5) The testers should be allowed to warm up for 30 minutes at the beginning of each test session to allow it to stabilize. The testers should not be turned of during their extended lunch hour of 2.5 hours.

(6) Their program of maintainance and calibration of the Automatic Test Equippment should be reviewed with the goal of insuring that an adequate budget is provided and that the organizational structure meets the needs of the equipment. In addition, the training of the operational and maintainance staff should be reviewed and possibily supplemented.

(7) A strict ESD program should be instituted at CEPREI. The people did not seem to have much of an appreciation of the seriousness of the ESD problem. I observed operators wearing rubber soled sandals testing ICs with no grounding straps. They should institute strict ESD control in all operations of the Institute where ICs or other ESD sensitive devices are handled. This is not just in the test laboratory but in the area where life test boards are loaded and unloaded.

(8) They use distilled water in their temperature/humidity test chambers. This is transferred manually in plastic buckets from the still to the equipment. There is a substantial chance for human error in this system. A load of tap water could invalidate a test run and contaminate the equipment. They should switch over to a piped system using appropriate plastic pipe.

Appendix A

ATTENDEES

The attendees to the seminar are as follows:

罗爱光	Luo Ai Guang	CEPREI
黄鹏	HUANG Peng	CEPREI
古关华	Gu Guanghua	CEPREI
孔学东	Kong Xuedong	CEPREI
仲里	ZHong Li	CESI
惠志刚	HUI ZHI GANG	208#, WUXi
熊锦涛	XIONG JIN TAO	MICROELECTRONIC COMPANY, WUXi
姜大勇	Jiang Dayong	CEPREI
徐爱斌	Xu Ai Bing	CEPREI
倪树麟	Ni shulun	CESI
謝文苗	Xie Wen Miao	CESI
齐建华	Qi Jian Hua	CESI
张利香	zhang Li Xiang	CESI
焦慧芳	Jiao Hui Fang	CEPREI
张文锋	Zhang Wenfeng	CEPREI
梁琼崇	LIANG QIONGCHONG	CEPREI

Seminar attendees (cont.)

刘明河	Liu Minghe	CEPREI
史晓峰	Shi Xiaofeng	CESI
严士方	Yen Si Fang	105# WUXI
章海良	Zhang Hailiang	CEPREI
赵建忠	Zhao Jian Zhong	28# SUZHOU
肖金生	Xiao Jin Sheng	CEPREI
殷燕华	Ying Yian hua	CEPREI
叶维略	ye vie jou	CEPREI
钟勤	Zhong Ching	CEPREI
王国强	Wang Guo Qiang	CESI
邢萍珍	Xing Ping Zhen	CEPREI
刘发	Liu Fa	CEPREI.
李任	Li Ren.	ROWA TV FACTORY, GUANGZHOU