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UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION
Vienna International Centre, P.O. Box 300, 1400 Vienna, Austria
Tel: (+43-1) 26026-0 · www.unido.org · unido@unido.org

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MICROPROCESSOR APPLICATION ENGINEERING PROGRAMME

DP/IND/84/030

INDIA

Technical report: Standardization of interfaces*

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of Andrew M. Norton, expert in microprocessor hardware and software development

Backstopping officer: V. Smirnov, Engineering Industries Branch

United Nations Industrial Development Organization
Vienna

* This document has not been edited.

ABSTRACT

This report describes the experts mission to India during the period mid-May to mid-July 1988. The visit focused on the Southern Regional Centre of the Microprocessor Applications Engineering Programme based at Indian Telephone Industries in Bangalore. The experts activities mainly consisted of technical lectures, project reviews, discussions and meetings with MAEP personnel.

Technical presentations included a lecture series on Microcomputer Bus Standards, System Design Engineering and an Introduction to Programmable Logic Devices. Project reviews emphasized system design engineering principles and modular hardware/software design. Training activities were reviewed and future proposed projects were discussed.

The report reviews activities at the Southern Regional MAEP Centre and details recommendations, observations and conclusions of the expert.

LIST OF CONTENTS

LIST OF APPENDICES

1. INTRODUCTION

The objectives of the mission as outlined in Job Description DP/IND/84/030/11-08/J13315 included participation in hardware and software project discussions at the New Delhi and Bangalore MAEP centres and to impart training to the Bangalore MAEP centre on design methodology.

Specific Duties of the expert were to include:

1.1 Apprise himself of the current status of microprocessor applications in the Indian industry.

1.2 Apprise himself of the objectives, status and results of various system engineering development projects going on in various centres.

1.3 Help project personnel in hardware and software development for various projects.

1.4 Train project personnel as well as centres on new methodologies for microprocessor based systems engineering.

1.5 Preparation of a final report, setting out the findings of his mission and recommendations to the Government on further action which might be taken.

It was indicated by UNIDO Vienna that modifications to these objectives would be made after meeting with the Chief MAEP Co-ordinator in India. Upon arrival in New Delhi and discussion with Dr. Krishna Kant, Chief Project Coordinator for MAEP, it was agreed that mission activities would be concentrated at the Southern Regional MAEP Centre, based at the Indian Telephone Industries in Bangalore.

This report focuses solely on the work at the Southern Regional MAEP Centre. Relevant mission activities for the period mid-May to mid-July are detailed in Appendix I "Itinerary".

2. RECOMMENDATIONS

While the Microprocessor Applications Engineering Programme has achieved its objectives, a second phase MAEP should be put in place when this first phase terminates in 1990. Specific recommendations with regards to the southern regional centre are:

2.1 Regional MAEP project coordination must be considered a full time position. While there are obvious and important advantages to placing MAEP centres within industry, the host organization should insure that the project coordinator devotes a minimum 50% of his time for MAEP coordination.

2.2 The Southern Regional MAEP Centre should be assigned the status of a separate department within the Indian Telephone Industries. The project coordinator should be given all facilities to permit him to work autonomously.

2.3 The MAEP project coordinator should schedule weekly design reviews with the senior technical staff to critically evaluate and manage each design project.

2.4 Excellent CAD technology exists within Indian Telephone Industries where the southern regional centre is based. In spite of these available facilities, inadequate services are provided to the MAEP centre. This situation should be remedied to permit this MAEP centre to take full advantage of these facilities.

2.5 Additional UNIDO expert assistance in system design engineering and software design engineering with emphasis on computer communication network design, implementation and applications would be of great benefit to this centre.

2.6 Engineering design documentation procedures for each pro should be established starting with a requirements analysis functional description and resulting in a working design docum detailing the hardware and software design. This working document would then provide a guideline for implementation procedures.

2.7 Intensive courses given by regional centres should be scheduled when possible to be coincident with expert missions in order to include expert participation in lectures. Further, the expert should be advised prior to mission of lecture topics by the project coordinators at the centres he will be visiting.

2.8 Programmable Logic Device technology (PALs, PLAs, PROMs) is not currently being used in microprocessor and digital design. This technology could greatly ennance digital design interface techniques and should be introduced.

2.9 UNIDO in coordination with the local UNDP office should insure that contact is established between the expert and MAEP project coordinators well in advance to the start of missions. This would prepare the expert more completely and permit selection/preparation of appropriate technical information.

3. ACTIVITIES OF THE EXPERT DURING MISSION

The itinerary outlined by the Chief Project Co-ordinator, Dr. Krishna Kant focused entirely on the Southern Regional MAEP Centre at the Indian Telephone Industries in Bangalore. Upon meeting with the Bangalore Project Co-ordinator, S. Rajaram, two main fields of activity were outlined for the expert.

3.1 Lecture Series

A series of lectures covering "Microcomputer Bus Standards" would be given for project personnel covering two standard microcomputer buses, the Intel MULTIBUS (IEEE 796) and the VME bus (IEEE 1014). A detailed outline summarizing the main topics of the lectures is included in appendix II. In addition, short lectures were given on System Design Engineering principles and an introduction to Programmable Logic Devices.

3.2 Project Discussions and Design Reviews

Expert input on current and future design projects involved system design, microcomputer bus interfacing, microprocessor and component selection, interface design, hardware and software organization. Current projects involving expert input were:

3.2.1 A Local Area Network communications board for the PC bus based on the IEEE 802.4 Token Bus standard

3.2.2 An intelligent Multiplexer/Demultiplexer using statistical multiplexer techniques.

3.2.3 A Local Area Network communications board for the VME bus running under the UNIX operating system

A system design philosophy was emphasized by the expert utilizing a "top down" approach identifying system functions and strategies prior to implementation. The expert worked with project personnel detailing each step in the system design process as well as providing guidelines for implementation.

3.3 Other Activities

Other activities included:

3.3.1 Discussions with DOE coordinators regarding centre activities

3.3.2 Discussions with Southern Regional Centre Project Coordinator

3.3.3 Detailed individual and group discussions with MAEP project personnel

4. SOUTHERN REGIONAL MAEP CENTRE - BANGALORE

The MAEP Southern Regional Centre is based at the Indian Telephone Industries in Bangalore. The centre is principally involved in the design, development and manufacture of communication systems as well as CAD/VLSI design. Current MAEP research and development efforts are focused on local area networks, statistical multiplexers and knowledge base systems.

MAEP staff include a Project Co-ordinator, a Senior Engineer, two Executive Engineers, two Assistant Executive Engineers and a Senior Technical Assistant. The centre is planning for the addition of five project engineers, two technicians and an administrative assistant. Mr. S. Rajaram is the regional centre Project Co-ordinator with three main areas of responsibility: MAEP Co-ordinator, CAD Research and Development, and Intelligent Computer Systems (commercial wing of the CAD PCB/VLSI group) manager. Mr. Chidambara, the Senior Engineer, functions as the second level supervisor providing techno-administrative support.

The current equipment position at this centre is quite sufficient for the design and development of microprocessor based systems. Equipment at the centre is detailed in Appendix V.

A new infrastructure is being built to house MAEP labs, equipment and personnel and is expected to be completed by August 1988. This building will include a computer lab, general lab, small library, staff room, seminar hall and administrative office.

4.1 Training Courses

4.1.1 Current

Upon arrival by the expert, centre personnel were involved in sponsoring a 2 week intensive course detailing microprocessor principles and applications in modern communication systems. The course was intended for engineers associated with telecommunication systems. It was given during the period 19 May - 1 June 1988 with course contents detailed in Appendix III. Nine lab sessions using the Intel 8086 and Motorola 68000 trainer kits and Intel series IV Microcomputer Development Systems were conducted providing hands-on microprocessor experience to the participants.

4.1.2 Future

An intensive course on microprocessors and communication systems for developing countries is being planned for Feb or March 1989. Announcements are being sent to cultural and educational attaches of embassies and international agencies.

Responses to the initial course announcements have indicated a high degree of interest.

Unfortunately, there are currently no subsidies or financial assistance available for this program. It is understood that UNDP generally needs to be notified 12 - 18 months in advance, in order to provide any type of sponsorship. The general feeling is that it will prove difficult for engineers from other developing countries to come to India for training without some form of assistance.

4.2 Completed Projects

The following three projects were completed prior to the arrival of the expert:

4.2.1 Design & Development of an intelligent controller for Satellite Data Communication Network.

4.2.2 Fail Safe controller for electronic switching systems

4.2.3 Microprocessor based CAD system for VLSI design.

4.3 Reviews of Current MAEP Projects

4.3.1 General

Working with project personnel, the expert emphasized a system design engineering approach for all current and future projects. Using the "top down" design approach, total system function was identified and partitioned into subfunctions associated with specific tasks. Each level of partitioning involved increased detail which resulted in defining the implementation methods. This systematic design method conceptually integrating interconnected modular subsystems results in systems that are easier to design, document, debug and modify. The expert further emphasized the need for system design documentation detailing:

1. Requirements Analysis
2. Functional Description
3. Software Design
4. Hardware Design
5. System Integration

The expert also emphasized the need for "top down" design at the software design stage as well as structured programming techniques and improvement of programming style to enhance software maintainance and documentation.

4.3.2 Local Area Network Communications board for PC bus

The main objective of this project is to realize a Local Area Network providing communication between independent computing entities such as microcomputers, printers and workstations. A prototype board providing Local Area Network communications based on the ARCNET local area network has been developed for the PC bus. ARCNET uses a modified token bus architecture based on the IEEE 802.4 communications standard.

The hardware design for the prototype has been completed and the expert suggested minor changes permitting additional user flexibility and improving noise characteristics. The design is based on a VLSI communications device (COM 9026 LANC) for controlling network operations. Hardware testing has been limited to the interface between the system CPU and the LANC. Testing of the network itself will proceed when network transceiver components have been received.

Software test routines have been developed in order to test the system hardware. Once the remaining components are received and hardware operation is verified, the board will be released for printed circuit board layout and fabrication. Since PCB fabrication lead times range from 1 - 3 months, hardware verification should be carried out as soon as possible.

The expert aided project personnel in producing a requirements document and the beginning of a functional description document. The first system utilities to be developed are electronic mail and remote file transfer. The expert was able to offer specific advice and stressed the need for a software design document detailing the functional modules required, memory management schemes, parameter passing conventions and data formats.

The anticipated completion date of this project is March 1989. A draft copy of the specification and block diagram of the LAN communications board has been included in this report.

4.3.3 Statistical Multiplexer

This project involves the development of an intelligent data multiplexer/demultiplexer to enable full duplex data communication between up to 8 asynchronous ports over a single high speed synchronous link using statistical multiplexer techniques. The statistical multiplexer (stat mux) must provide error detection and recovery features, data buffering and dynamic memory allocation on a per channel basis. The data link protocol selected for the synchronous link is X.25 level 2. The X.25 communications standard is the interface approved by CCITT defining the interconnection of data terminal equipment and data

PRELIMINARY SPECIFICATIONS FOR LAN-COMM BOARD

1. Scope :- Development of a local area network to provide communications between IBM PC compatibles. The local area network provides Arcnet features which are a subset of I.E.E.E 802.4 standards for token bus architecture.

The hardware is based on a VLSI communications controller, the S.M.C COM 9026 local area network controller. Interface to the communication media is provided by S.M.C transceiver and Hybrid driver/ receiver. The board functions as a slave device to the system CPU with access provided through memory or I/O mapping at switch selectable base address location.

System software will be provided to implement electronic mail and file transfer from remote network PC's. Menu driven software which are user friendly are developed using 'C' programming language.

2. **Specifications**

2.1 Network characteristics

Data rate	- 2.5 mbit
Media access	- Token passing scheme based on I.E.E.E 802.4
Topology	- Bus structure
Transmission	- Base band
Nodes/network segment	- 255
Data packet size	- 508 bytes

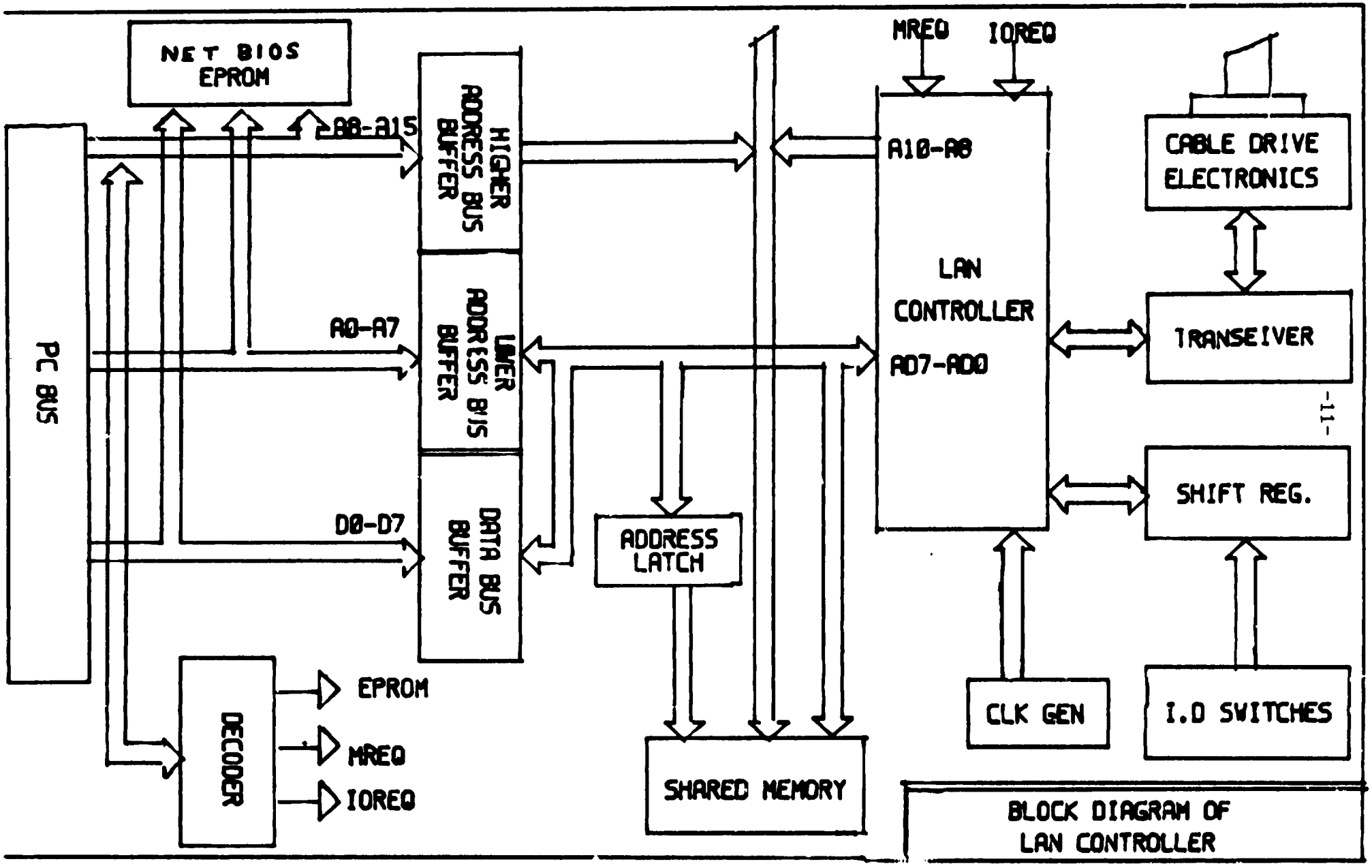
Reconfiguration as nodes are added or deleted from network
CRC check and generation
MAX length of bus/segment - 1000 feet.

2.2 Hardware characteristics

Strappable interrupt selection
Memory mapping or I/O mapping selectable
Switch selectable base address
Switch selectable node address
On board EPROM for NETBIOS

2.3 Software characteristics

File transfer facilities : Search, Transmit, Receive, Store.
Electronic mail facilities : Create, Receive, Transmit, View, Store, List.



BLOCK DIAGRAM OF LAN CONTROLLER

circuit termination equipment for operation in the packet mode on public data networks.

A preliminary design specification had been generated by project personnel and was reviewed by the expert. The expert suggested some changes in the specification in order to enhance performance. The expert advised on design methods and strategies, microprocessor and component selection, and introduced various software design techniques.

It was decided that the design be based on the Intel 8088 microprocessor. Other system components would tentatively include two 32K static RAMs, an octal UART with RS232 and RS422 communications interfaces for asynchronous port communications, a synchronous link communications controller implementing X25 level 2, a programmable interrupt controller and either EEPROM or dip switches for user selection of configuration options.

The expert discussed software design and programming methods. Software concepts discussed that are directly applicable to this project included: data structures, linked lists, queues, dynamic memory allocation and management, foreground and background process synchronization.

The expected completion date for this project is March 1989. The revised specification and a block diagram of the stat mux hardware has been included in this report.

4.3.4 Local Area Network Communications board for VME bus

The possiblity of designing a local area network communications board for the VME bus running under a UNIX environment was also discussed. This project had been included in the initial project development schedule although the project is only in its earliest planning stages. The expert suggested that the project would require significant hardware and software design expertise before the project should be considered further. This project would involve a high degree of expert assistance at the planning and system design stages.

The project would involve the development of a communications board based on the ARCNET network. This will provide a modified token bus architecture based on the IEEE 802.4 standard for VME bus systems. The VLSI communications device used is the same controller used for the PC bus, the Standard Microsystems Corp. COM9026 Local Area Network Controller. Although the board will use the same LAN controller as was used in the PC bus implementation, the expert suggested the basic design philosophy should be quite different. VME bus systems are typically high performance multi-user, multi-tasking, multiple bus master systems. This implies that the design of a

STATISTICAL MULTIPLEXER

1. SPECIFICATION

Multiplexer Type	:	Statistical
Network capabilities	:	Point to point
Terminal channels	:	8 asynch channels, 16 speeds/channels from 50 - 9.6K bps
Code accepted	:	data : 5 to 8 bits stop bits 1, 1.5, 2 parity : even, odd, nil
Speed intermix	:	Any intermix upto 9.6K * 8 = 76.8K bps
Control port	:	Asynchronous, RS 232C/V.24
Network port	:	Synchronous, upto 9.6K bp
Terminal port	:	Asynchronous, RS 232C/V.24
Buffer	:	64 K

2. FEATURES

* 16 speed options, from 50 to 9.6K bps, indepdendently selectable for each terminal port.
* dynamic allocation of buffers for each channel
* BURST rate of 73.8 kbps
* Auto echo and fly back delay
* terminal port data constraint using either XON/XOFF or RTS/CTS
* Performance and mode monitoring indicators
* Continual self diagnostics
* Use of X.25 level 2 protocol for synchronous channel
* Control port terminal provides centralized control of configuration monitoring and diagnostics
* Use of EEPROM for storing configuration parameters
* Terminal break handling capability
* Local and remote loop back mode

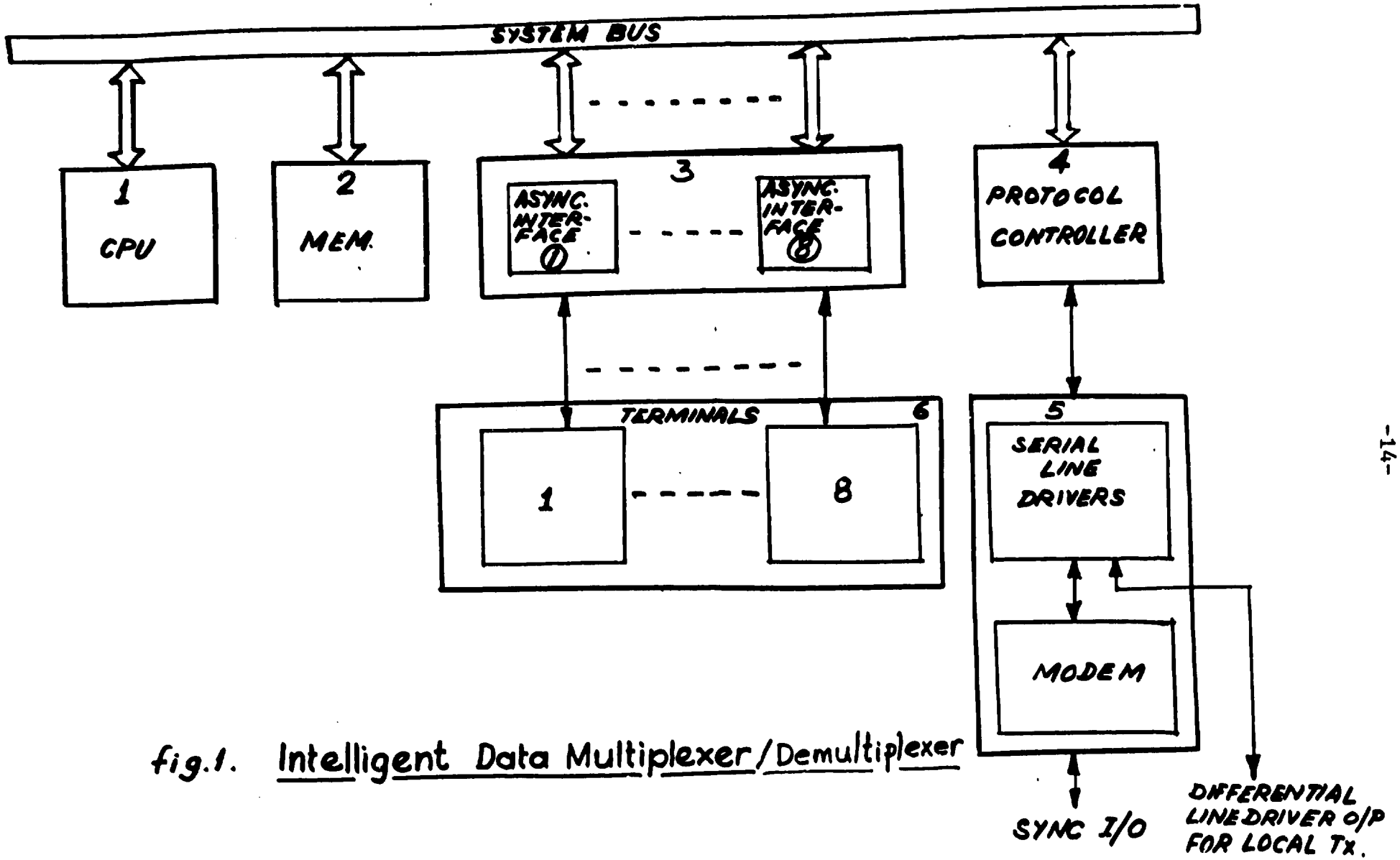


fig.1. Intelligent Data Multiplexer/Demultiplexer

communications board should make maximum use of the bus for short bursts of time permitting other devices maximum bus use. This dictates the design of a VME bus master with on board CPU and DMA as well as the LAN controller. The on board CPU should manage the LAN controller as well as coordinate DMA transfers between the LAN controller memory buffer and system memory. As a VME bus master, the board would request use of the bus and when granted, burst transfer a block of data to/from system memory then flag the system that a data block is available. The on-board CPU could further be used for diagnostics and error statistics. Possible later implementations could contain resident software for Transport and Network layer protocols.

4.3.5 Knowledge Base Shell for Communications Networks

The application of knowledge base techniques, also referred to as expert systems, involves the generation of an appropriate knowledge base. This constitutes the application relevant database and the rules according to which the information in the database can be related to each other. Inferences are made by the inference engine which manipulate these data and rules leading to logically correct inferences.

The first phase of this project involved an interactive, user-friendly front end (window manager) for capturing the application dependent data and rules and development of the inference engine. This has been implemented on an IBM PC/AT compatible, running MS-DOS operating system. Programming languages used for the implementation were 'C' and GCLISP.

Second phase tasks currently under development are:

1. Coupling of the user-friendly interface and the inference engine

2. Coupling of the inference engine and the database

3. Implemention of an explanation module

4. User input of variables to inference engine

5. Creation of illustrative knowledge bases for the different applications in communication networks

6. Porting the software packages to an Intel 80386 based IBM PC/AT.

The expected completion date of this project is March 1989. The expert met with the Senior Engineer in charge of this project, Mr. Sivaramakrishnan, in order to review the current status. There was no further expert involvement with this project.

4.4 Future Projects

Possible future projects were very briefly discussed with the Project Coordinator. These projects might involve the following areas:

1. LAN utilities
2. Network Operation and Maintainance Equipment
3. LAN Analyzer
4. X.25 Front Ends for Wide Area Networks
5. PC based Microcomputer Development Systems with In Circuit Emulation

4.5 UNIDO Training Fellowships

Four engineers were deputed for two months from 20/10/87 to 21/12/87 to two telecommunications companies in the U.K. and two in the U.S.A. for exposure to advanced communications systems. The four engineers were: M.S. Mohan, M.V. Roopchandar, H.V. Nagaraja and P.S. Ullagaddi.

The companies providing the training were: Advanced Micro Devices, U.S.A., Capricorn Systems Intl. U.S.A., GEC Telecommunications, U.K, Marconi Communications, U.K.

It is proposed to depute the following three engineers for a 3 month training program during 1988 for training in data communications: Chidambara, K.J. Somashekar and K. Nalinakshan.

Organizations willing to provide training have not yet been identified and the centre is currently searching for commercial and academic organizations to provide sponsorship.

4.6 Student Training

The MAEP centre provides work facilities for 25 undergraduate and 2 graduate engineering students presently. They will be working on various aspects of MAEP projects for 4 months and 8 months respectively. Project work is carried out under the supervision of the MAEP staff. In addition to current MAEP projects, student trainees are involved in development work on a number of minor projects.

4.7 Conclusions & Observations

Activities at the MAEP centre in Bangalore are divided into two main areas. The first area involves training courses in microprocessors and communications systems. The second area is project development in the field of data communications.

Training activities at the centre are commendable. Intensive courses provide hands-on training using educational kits and materials provided by the centre. Most sessions are given by highly qualified local experts in their respective areas. Lecture notes are given to all course participants.

Project development is proceeding slowly. A systems design approach has been greatly emphasized by the expert prior to implementation. The current equipment position is quite good and should provide an adequate microprocessor systems development environment. The MAEP staff seem to be well qualified although there is a general lack of design experience. Particular deficiencies have been identified and should be addressed in order for project development progress to improve. The following lists more specific conclusions and observations:

4.7.1 UNIDO expert assistance is required to aid in system design engineering especially during the early stages in project design.

4.7.2 There is an acute lack of microprocessor software engineering expertise. The centre should add to its engineering staff a software design engineer with experience in microprocessor systems.

4.7.3 A UNIDO expert with specific software design experience in local area network design, implementation and applications could provide invaluable assistance to this centre.

4.7.4 Rapid completion of the new MAEP building is necessary in a minimum amount of time in order to provide the necessary space for equipment and project personnel. Presently, there is insufficient space available for MAEP needs.

4.7.5 There is a lack of project management and coordination due to the minimal amount of time that the project coordinator has been able to devote to MAEP. As an employee of I.T.I., Mr. Rajaram manages both commercial I.T.I. activities as well as MAEP activities. Mr. Rajaram is a highly capable and dynamic individual who can certainly provide the project management and coordination required by MAEP if only he is permitted to dedicate his time to MAEP activities.

4.7.6

Commercial organizations are often reluctant to permit project personnel visits due to the proprietary nature of their development work. Further, there is a general lack of motivation on the part of any commercial agency to provide training. All prior fellowships were arranged through personal contacts of either project personnel or UNIDO experts. This problem could be alleviated if fellowship assistance could be modified to include workshops promoted by commercial vendors around the world. A wide variety of such workshops are available within Asia (Bangkok, Singapore, Hong Kong) in areas such as data communications, local area networks and microcomputer development systems which provide hands on training.

4.7.7 The centre has been having difficulty due to non-receipt/late receipt of information from UNDP regarding expert visit notification and equipment arrival notification. Coordination between UNDP and MAEP centres should be improved.

APPENDIX I

Itinerary: A.M. Norton

13 May - 15 July 1988

Date	Activity
Fri, 13 May	Leave Mexico. Arrive New York.
Sat. 14 May	Leave New York.
Sun, 15 May	Arrive Vienna.
Mon, 16 May	UNIDO Briefing.
Tues, 17 May	Leave Vienna.
Wed, 18 May	Arrive New Delhi.
	UNDP Administrative Briefing: Ms. V. Sukuntha
Thurs,19 May	UNDP Briefing: Mr. Islam, SIDFA Appointment: Dr. Krishna Kant Dept. of Electronics
Fri, 20 May	Leave Delhi/Arrive Bangalore.
	Appointment: S. Rajaram Project Coordinator, MAEP
Mon, 23 May	Project Briefing/Itinerary Appointment: S. Rajaram Project Coordinator, MAEP
Tues, 24 May	Evaluation of Intensive Course on Microprocessors
Wed, 25 May	Preparation of Lecture Notes Evaluation of equipment
Thurs,26 May	Organization of Lecture Series
Fri, 27 May	Discussion of Microcomputer Development Systems
Mon, 30 May	Literature Review: Statistical Multiplexers
Tues, 31 May	Preparation of Lecture slides/diagrams
Wed, 1 June	Evaluation of Intensive Course on Microprocessors
Thurs, 2 June	Review of Local Area Networks

Fri. 3 June	Project Design Review
Mon. 6 June	Project Design Review
Tues. 7 June	Project Design Review
Wed. 8 June	Lecture Series
Thurs. 9 June	Library
Fri. 10 June	Lecture Series
Mon. 13 June	Project Design Reviews
Tues. 14 June	Meeting with: Dr. Varadan, Dept. of Electronics Mr. Rajaram, MAEP Coordinator
Wed. 15 June	Lecture Series
Thurs. 16 June	Preparation of Final Report
Fri. 17 June	Lecture Series
Mon. 20 June	Project Design Reviews
Tues. 21 June	Lecture Series
Wed. 22 June	Meeting with: Mr. Rajaram, MAEP Coordinator
Thurs. 23 June	Preparation of Final Report
Fri. 24 June	Lecture Series
Mon. 27 June	Project Design Reviews
Tues. 28 June	Project Design Reviews
Wed. 29 June	Meeting with Mr. Rajaram, MAEP Coordinator Lecture Series
Thurs. 30 June	Preparation of Final Report
Fri. 1 July	Lecture Series
Mon. 4 July	Meeting with Mr. Sivaramakrishnan Senior Engineer
Tues. 5 July	Lecture on Programmable Logic Devices
Wed. 6 July	Project Design Reviews
Thurs. 7 July	Preparation of Final Report

Fri,	8 July	Discussion of Future Projects
Sat,	9 July	Leave for New Delhi
Mon,	11 July	Meeting with Dr. Krishna Kant Dept. of Electronics
Tues,	12 July	UNDP office
Wed,	13 July	Leave Delhi. Arrive Vienna
Thurs,	14 July	UNIDO Vienna. Debriefing
Fri,	15 July	Leave Vienna. Arrive New York.

APPENDIX II

Lecture Series Outline: Microcomputer Bus Standards

1. Introduction to Microcomputer Buses

    1.1 Function
    1.2 Type
    1.3 Organization
    1.4 Protocol
    1.5 System Components

2. Intel MULTIBUS (IEEE 796)

    2.1 Functional Description
    2.2 Signals
    2.3 Data Transfer Operations
    2.4 Interrupt Operation
    2.5 Bus Exchange/Arbitration/Priority
    2.6 Power Fail Considerations
    2.7 Electrical Spec
    2.8 Mechanical Spec
    2.9 Design Guidelines/Examples
    2.10 Bus Interface ICs

3. VMEbus (IEEE P1014/D1.2)

    3.1 History/Introduction
    3.2 Data Transfer Bus
    3.3 Data Transfer Bus Arbitration
    3.4 Priority Interrupt
    3.5 Utilities
    3.6 Electrical Spec
    3.7 Mechanical Spec
    3.8 Design Guidelines
    3.9 Bus Interface ICs

APPENDIX III

Intensive Course on Microprocessors and Communication Systems
19 May - 1 June 1988

Organized by the Southern Regional Centre for MAEP
Indian Telephone Industries
Bangalore

The set of topics discussed in the 2 week intensive course include: architecture and programming of 16 bit microprocessors. I/O interfacing and support devices, methodology and aids for the design of microprocessor based systems, applications of microprocessors in modern telecommunication systems, SPC exchanges, data communications and satellite transmission systems. Faculty for the course consisted of senior R & D engineers of the Indian Telephone Industries.

Morning sessions generally consisted of lectures while afternoons involved nine different lab sessions.

Detailed course contents:

Date	Lecture Topic	Lecturer
19/5/88	Microprocessor History, Product Range and Applications	S. Rajaram
	Microprocessor Architecture/Programming	
	Intel 8086	Chidambara
	Motorola 68000	Nalinakshan
20/5/88	Microprocessor Architecture/Programming	
	Intel 8086	Chidambara
	Motorola 68000	Nalinakshan
21/5/88	Data Communications	S. Rajaram
	Microprocessor Architecture/Programming	Nalinakshan
23/5/88	I/O Interfacing	R.Srinivasan
	Data Communications	S. Rajaram
24/5/88	I/O Interfacing and support devices	R.Srinivasan
	Data Communications	S. Rajaram
25/5/88	I/O Interfacing and support devices	M.S. Mohan
	Data Communications	Somashekar
26/5/88	I/O Interfacing and support devices	M.S. Mohan
	Microprocessor Systems Development	Radhakrishnan

27/5/88	Microprocessor Systems Development SPC Exchanges	Roopchandar K.K.Sundaram
28/5/88	Microprocessor Systems Development SPC Exchanges	Roopchandar K.K.Sundaram
30/5/88	SPC Exchanges Satellite Communications	H.V. Nagaraj Ullagaddi
31/5/88	SPC Exchanges Satellite Communications	H.V. Nagaraj Ullagaddi
1/6/88	Status/Trends in Communication Systems	Rajendran

APPENDIX IV

List of MAEP Personnel with whom expert met

UNDP New Delhi	
Ms. V. Sukuntha	UNDP Advisor
Mr. Islam	UNDP SIDFA
Dept. of Electronics - Government of India	
Dr. Krishna Kant	Chief Coordinator MAEP
Dr. Varadan	Coordinator MAEP
MAEP Southern Regional Centre - Bangalore	
S. Rajaram	MAEP Project Coordinator Deputy General Manager, ICS Group
Chidambara	Senior Engineer
Sivaramakrishnan	Senior Engineer
M.V. Roopchandar	Engineer Executive
M.S. Mohan	Engineer Executive
Nalinakshan	Assistant Executive Engineer
K.J. Somashekar	Assistant Executive Engineer
V. Rajasekar	Assistant Executive Engineer
Ms. B.D. Gandhi	Finance Officer
Ravichandran	Clerk-cum-typist
Ms. Kanaka Nayak	Clerk-cum-typist

APPENIDIX V

Southern Region MAEP Centre
List of Equipment

Quantity	Type
2	Intel MDS Series IV Development Systems with 8086/88 In Circuit Emulator 80186 In Circuit Emulator EPROM Programmer
1	HP 1631D Logic Analyzer
1	HP 4995 Protocol Analyzer
1	Programmable Data Communications Tester
1	OMC 68020 VME based system
4	IBM PC compatibles
2	Tektronix digital oscilloscopes
10	8085 microprocessor trainer kits
6	8086 microprocessor trainer kits
6	68000 microprocessor trainer kits
10	CRT terminals
4	Paradyne DCX815 Statistical Multiplexers
4	Modems (4800 & 9600 baud)
1	Video System comprising VCRs, camera, monitor and accessories
1	Omega 58000 system
3	OMC Designer Workstations
1	Microwave frequency counter