OCCASION

This publication has been made available to the public on the occasion of the 50th anniversary of the United Nations Industrial Development Organisation.

DISCLAIMER

FAIR USE POLICY

CONTACT

Please contact publications@unido.org for further information concerning UNIDO publications.

For more information about UNIDO, please visit us at www.unido.org

UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION
Vienna International Centre, P.O. Box 300, 1400 Vienna, Austria
Tel: (+43-1) 26026-0 · www.unido.org · unido@unido.org

James MASON

16723

FORSEEABLE APPLICATIONS OF INTEGRATED CIRCUIT TECHNOLOGY FOR DEVELOPMENTAL ACTIVITIES IN DEVELOPING COUNTRIES

by

J. L. MASON
QUEEN'S UNIVERSITY
KINGSTON, CANADA

PRESENTATION TO: UNIDO CONSULTATIVE GROUP ON INFORMATICS TECHNOLOGY

VIENNA, DECEMBER 1987

"The true pay-off of informatics technology for developing countries will only be realized if the technology leads to applications to meet the specific requirements and needs of developing countries. This requires on the part of those countries a technological capacity which will need to encompass software development, capacity for applications involving standard chips and equally design capacity for semi-custom or custom chips"

- INTRODUCTION

- IC DESIGN METHODOLOGIES
  - Gate Array
  - Standard Cell
  - full custom

- MPC PROJECTS -
  - examples
  - essential ingredients for success

- COMMERCIAL EXAMPLE

- GENERAL CONCLUSIONS

SEMICUSTOM - GATE ARRAY METHODOLOGY

- Array of standard logic circuits
- Only the metal layers need to be designed in order to define function
- Rapidly growing approach

  1982 – 35 vendors 1987 - 250 vendors

- Very popular for ASIC's

TECHNOLOGIES
- nMOS
- CMOS
- BIPOLAR

PROTOTYPE TURNAROUND TIME

- design	7 weeks
- fabrication	5 weeks
- package/test	2 weeks
	14 weeks

achievable goal 4 weeks

TESTING
- relatively easy
- standard I/o pad placements

COST
- 0.17 to 0.2 cents/gate
- dropping rapidly

CAD and CAT software well developed

SEMICUSTOM - STANDARD CELL METHODOLOGY

- Circuit constructed from combination of standard building blocks
- specialized cells often not available in gate array i.e. analog blocks, PLA's, multiport memories

ADVANTAGES - cf Gate Array

- flexibility in shape of circuit
- flexibility in function
- flexibility in pad count and position
- more packaging options

DISADVANTAGES - cf Gate Array

- requires complete fabrication cycle
- more masking stages
- prototype and manufacture turnaround longer
- higher cost
- more sophisticated CAD and CAT
- fewer vendors

CUSTOM DESIGN - MPC PROJECTS

INTRODUCTION

MPC PROJECTS

- examples
- details France, USA, Canada

ESSENTIAL INGREDIENTS

C - Evolution of MPC projects 1981-1986

The following table summarizes MPC projects evolution from begining of projects in 1981 until 1986.

EVOLUTION OF MPC PROJECTS 1981-1986

Date	Manufacturer	Technology	Channel length micron	Lambda micron	Number of centers	Number research circuits	Number educatio. circuits	Total circuit area λ^2	Mean circuit area λ^2
81	UCL	UCL	-	4	1	7	1	-	-
82	CNET	NMOS/NC	4,5	3	10	15	12	$39\ 10^6$	$1,4\ 10^6$
83	CNET	NMOS/L3	3,15	2,25	18	25	23	$62\ 10^6$	$1,3\ 10^6$
84feb	CNET	NMOS/L3	3,15	2,25	15	15	28	$72\ 10^6$	$1,7\ 10^6$
84mar	MHS	CMOS/Saji4	3,5	2,25	8	3	6	$18\ 10^6$	$2,0\ 10^6$
84oct	CNET	NMOS/L3	3,15	2,25	12	9	18	$48\ 10^6$	$1,8\ 10^6$
85mar	THOMSON	NMOS/hmos1	3,5	2,5	10	19	21	$50\ 10^6$	$1,3\ 10^6$
85june	MHS	CMOS/Saji5	2	1 et 2	11	18	14	$203\ 10^6$	$6,3\ 10^6$
86feb	THOMSON	NMOS/hmos1	3,5	2,5	13	37	16	$122\ 10^6$	$2,3\ 10^6$
86june	MHS	CMOS/Saji5	2	1 et 2	22	34	39	$657\ 10^6$	$8,9\ 10^6$
Total						182	178		

A total of 360 circuits has thus been fabricated, half research circuits, half educational circuits.

In 1986 it should be noticed the increase of the participation and the increase of the mean size of the circuits. From 1985 to 1986, the increase of the participation (in circuits' number) has been 30% for the NMOS and 130% for the CMOS and the increase of the mean size of the circuits (in $\lambda 2$) has been 75% for the NMOS and 40% for the CMOS .

LABORATORIES AND UNIVERSITIES WHICH HAVE SUBMITTED CIRCUITS TO THE FRENCH MPC

FRANCE	Town / Country
Ecole Supérieure d'Electricité	Gif / Yvette
Ecole Supérieure d'Electricité	Rennes
Ecole Nat. Sup. d'Electron. et de Radio Electri.	Grenoble
Ecole Nat. Sup. d'Inform. et Math. Appl	Grenoble
Ecole Nat. Sup. d'Ingen. Electriciens	Grenoble
Laboratoires Circuits et Systèmes	Grenoble
Techniques de l'Inform. des Math. de la micro-electr. et de la Microscopie quantit.	Grenoble
Institut Supérieur d'Electronique du Nord	Lille
Laboratoire d'Autom. et de Microelectronique	Montpellier
Institut d'Electronique Fondamentale	Orsay
Laboratoire de Recherche en Informatique	Orsay
Ecole Polytechnique	Palaiseau
Université Paris VI	Paris
Ecole Nat. Sup. des Télécommunications	Paris
Ecole Normale Supérieure	Paris
Institut Supérieur d'Electronique	Paris
Institut de Rech. en Informat. et Syst.Aleatoires	Rennes
Institut Nat. de Recherche en Inform. et Automat.	Roquencourt
Laboratoires d'Autom. et d'Analyse des Systèmes	Toulouse
Institut National Sciences Appl.	Toulouse
Institut Universitaire en Informatique	Toulouse
Institut de Physique Nucléaire	Villeurbanne

FOREIGN COUNTRIES	
Universidad Fédéral do Rio Grande do Sul	Porto Alegre BRASIL
Universidad Autonima de Barcelona	Barcelone SPAIN
Universidad Politecnica de Madrid	Madrid SPAIN
Politecnico di Torino	Turin ITALY
Instituto de Engenharia de Sistemas et Computadores	Lisbonne PORTUGAL
Institut für Matematische Maschinen und Datenverarbeitung	Eriangen GERMANY
Ecole Polytechnique Fédérale	Lausanne SWITZERLAND
Commissariat aux Energies Nouvelles	Alger ALERIA
Laboratorium Elektronika	Bandung INDONESIA

THE MOSIS® SERVICE

Price Schedule

(Prices valid through June 30, 1988)

Technology	Maximum Project Size (mm)	Minumum Quantities	Total Price	Additional Parts
NMOS	4.6 x 6.8	12	$2,900	$ 660
3u and up	6.9 x 6.8	18	$5,100	$ 950
	7.9 x 9.2	24	$8,600	$1,370
CMOS	2.3 x 3.4	4	$ 400	N/A
3u	4.6 x 6.8	12	$3,500	$ 830
	6.9 x 6.8	18	$6,000	$1,130
	7.9 x 9.2	24	$10,400	$1,670

Technology	Price per Sq. mm	Minimum Lot	Packaging Cost per Lot	
CMOS				
2u	$140/sq. mm	30	$ 900	N/A
1.2u	$610/sq. mm	50	$1,500	N/A

Project Size:

MOSIS will add scribe lanes and other overhead to the submitted geometry for all technologies; the maximum project sizes listed above refer to actual design area.

Packaging:

Packaging is included in the 3u prices, but the 2 and 1.2u feature sizes are priced at $900 for 30 packaged parts and $1500 for 50 packaged parts, respectively. If you wish to use your own packages, send them to MOSIS with a bonding diagram; this diagram will be sent to the packager along with your chips. A sample bonding diagram is provided in this package. When you provide the packages, there is a special handling and bonding fee of $20 per package.

Standard fabrication quantities are expected, but not guaranteed, to yield working parts after allowing for normal VLSI fabrication defects, provided the submitted design is correct. MOSIS delivers a set of bonded and packaged integrated circuits, containing the design exactly as submitted by the customer. MOSIS checks for correct syntax but does not validate designs. Circuits are either bonded per customer instructions or MOSIS provides a diagram showing how bonding was done. A sample from the lot is visually inspected.

TABLE 1: Design Activity in Universities Participating with CMC

Year	Process Technology	Number of Participating Universities	Number of Multi-project Dies	Number of Designs Implemented	Number of Packaged Chips
1983	6-micron NMOS	8	17	34	408
	5-micron CMOS	6	11	47	204
1984	6-micron NMOS	9	37	59	900
	5-micron CMOS	15	40	109	464
1985	6-micron NMOS	5	25	32	360
	5-micron CMOS	20	88	259	1022
1986	3-micron CMOS	20	55	157	914
	5-micron CMOS	16	41	138	870
1987	3-micron CMOS	20	86	199	1151
	5-micron CMOS	9	13	41	305

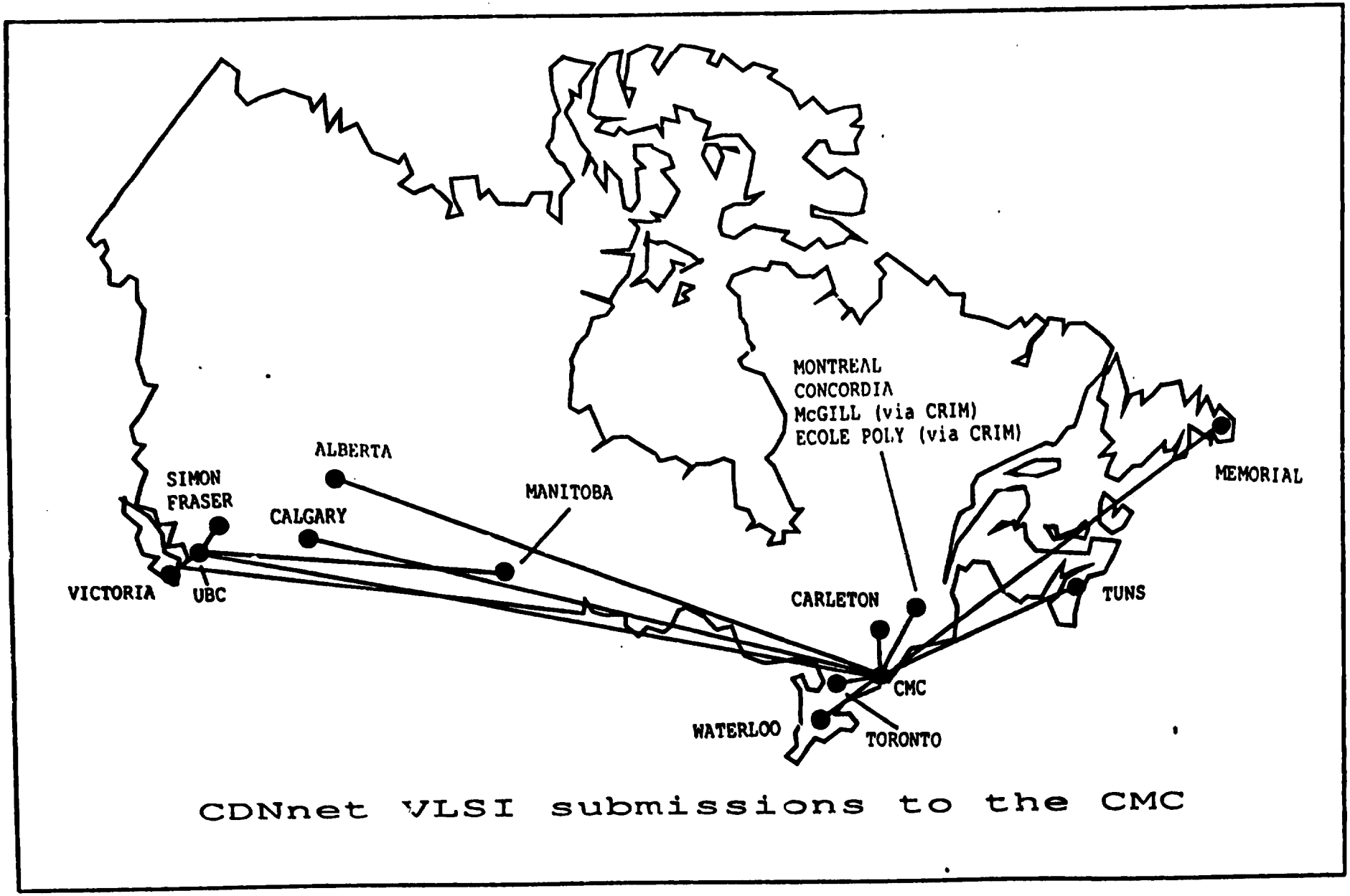

Figure 3: Network Communications

1.1(a) People Active in VLSI Research

	Total	Appointments made in 1986	Appointments ending in 1986
Academic Faculty	171	14	1
Visiting Faculty	5	1	2
Research Staff	29	7	4
Technical Support Staff	42	8	1
Graduate Students	372	81	14
Other	22	5	4

Breakdown of Faculty by Department:

Electrical Engineering	116
Computer Science	36
Physics/Eng. Physics	4
Other	23

1.3 Graduate Student Activity

DEPARTMENT	PENDING		COMPLETE		EXPERIENCE		EMPLOYMENT			
	Masters	PhD	Masters	PhD	Design	Test	IND	PUB	UNI	F
Electrical	145	71	34	9	142	113	24	2	2	7
Computer Sc.	23	8	4	3	12	3	1		1	3
Other	21	8			2	2				
TOTAL	189	87	38	12	156	118	25	2	3	10

RESULTS OF TRENDS IN PROCESS TECHNOLOGY

GOOD

- smaller feature size
- increasing circuit density
- increasing circuit speed

BAD

- increased design complexity
- increased design time
- increased testing problem

COST OF PROTOTYPING

- increased !!
  - more sophisticated packaging required
  - MPC not possible without direct write E-beam
  - fewer suppliers, therefore less competition

ESSENTIAL INGREDIENTS

① Equipment Access - hardware/software

② Communications

③ Access to fabrication for prototyping

④ Centralized purchasing yields economies of scale and efficient solution of common problems

ONE EXAMPLE - ASIC Application

THE COMPANY

- large New Zealand manufacturer of "white goods" washing machines, refrigerators, stoves

THE PROBLEM

- washing machines were becoming expensive
- large number of mechanical parts

THE SOLUTION

- complete redesign of agitator mechanical system and control and timer systems
- ASIC used for control

THE RESULT

- less expensive, more reliable washing machine
- exported to Australia

THE IMPLICATIONS

- local applications will be recognized locally
- local skills and awareness required in order to recognize the need for a technological solution to a problem and the appropriate way of satisfying that need.
- in the short-term, expertise and facilities are available to assist in the IC design

EXPLOITATION OF IC TECHNOLOGY

Prime long-term goal should be to develop a good skill base

Gate array or standard cell methodologies most promising in short-term

Bulk of applications do not require state-of-the-art technology

Fabrication should be done through broker. Cost of local fab line too high to be supportable

Good communication links are essential

Joint, cooperative programs beneficial