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SEMICONDUCTOR DEVICES AND ELECTRONIC SUB-SYSTEMS FOR TRANSPORTATION

DP/IND/84/015

INDIA

Technical report: Power transistor devices for transportation equipment (Part II)*

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of H. B. Assalit
Expert in power semiconductor devices

Backstopping officer: J. Fürkus, Engineering Industries Branch

United Nations Industrial Development Organization
Vienna

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ABSTRACT

This report outlines the activities of the consultant during his three months assignment at CEERI, Pilani. Project involvement was in the development of Power Darlington Transistor Devices, and more specifically in areas relevant to device design, package design, material selection, fabrication processes and facility evaluation.

As a whole, the processes and facilities that are utilized in this project are quite satisfactory; however, some problems still exist in the areas of :

- Silicon availability
- Package availability
- Alloying Equipment
- Alloying Process

Quick actions are required to find solutions to these problems in order to preserve the continuity of the project.

1. INTRODUCTION

This consultancy assignment at the Central Electronics Engineering Research Institute (CEERI) in Pilani, Rajasthan, India, was established within the framework of the UNDP Project: "Semiconductor Devices and Electronic Sub-Systems for Transportation" (IND/84/015).

Its purpose was to provide assistance to the Institute in Research and Development of Power Transistors for Power Control in Electric Devices for Transportation.

The consultant arrived in Delhi on February 17, 1987, and started his assignment in Pilani on February 19, 1987, for a period of three months terminating May 15, 1987.

2. PROJECT INVOLVEMENT & SCHEDULE

After discussion with Dr. G.N. Acharya, Institute Director, Dr. W.S. Khokle, Deputy Director, and various project related scientists, a work programme was established as shown in Appendix I.

This schedule included the following major tasks:

- Review of present device design, package design, and material selection.
- Evaluation of the fabrication processes for Power Transistor Devices.
- Evaluation of the facilities in use at CEERI to produce Power Semiconductor Devices.
- Evaluation of a new process for the diffusion of Gallium into Silicon.
- Computer simulation in relation to Transistor Switching Speed.
- Series of lectures on Power Semiconductor Devices such as Power Transistor Modules, Darlington Transistors, Gate Turn-off Thyristors, etc.
- Assistance in power semiconductor device related fields as requested by the members of the Institute and within the knowledge of the consultant.

3. PROJECT ACCOMPLISHMENTS

Accomplishments have been limited and below the expected level. Various delays in installation and repair of processing equipment have slowed down the planned program.

3.1 Review of Device Design, Package Design, and Materials

3.1.1. Device Design

The present design to be used with the 300A Transistor is basically an enlargement of the 100A Transistor design. It uses circular segmented interdigitation as shown on figure 1. The technology is planar and requires an especially shaped molybdenum shim to make contact to the emitter fingers without shorting the base elements of the device.

The new device is provided with an extra base connection (B2 on figure 2) to be used to speed up the device desaturation during turn-off.

The free-wheeling diode (DI on figure 2) is presently integrated with the transistor itself. This diode shares its own base with the collector of the transistor (see figure 3). The Recovery Parameters of this diode may be too large* to be acceptable in inverter circuit applications, and it may be necessary to separate the diode from the transistor (in the application, a selected discrete diode would then be connected across the transistor outside of its package).

Therefore, as an alternate, a new mask was designed without the by-pass diode for the 100A device. A copy of this mask is shown on figure 4. The six diffused resistor $RB2_1$ to $RB2_6$ form an equivalent resistor, RB2 on figure 2, which is about 2Ω in value.

The new mask is available, but it has to be evaluated. If satisfactory, this mask design will be extended to the 300A transistor device.

* Note:

This is based on the measured lifetime in the transistor collector region ($\approx$ 20 µsec). No recovery measurements were made of the integrated diode at the time of this writing.

A full evaluation of the recovery characteristics of the diode should be performed.

3.1.2. Package Design

The 100A Transistor utilises a standard design package available from a US Company (LATRONICS).

The 300A Transistor Package is not commercially available and had to be designed by CEERI. This design was already available at the time of arrival of the consultant at CEERI.

This design includes an extra base connection as shown on figure 5 to be used to speed up the device desaturation during turn-off.

The package supplier appears to have originally provided a quote for this type of package.

An order was placed for the following items:-

Item 1 - 100 X 33 mm Transistor packages

Item 2 - 100 X 40 mm Thyristor packages

Item 3 - 100 X 40 mm Transistor packages.

Todate, only item .2 (40 mm Thyristor packages) is satisfactory.

Due to errors in numbering and sizing, item 1 was received

as a "30 mm thyristor package" (and not "33 mm transistor package") ; item 3 was not delivered because of lack of information as noted by the supplier.

Since these components are critical for project completion, some actions should be quickly taken to solve the present delivery problem.

CEERI should reorder 100 x 33 mm transistor packages, and negotiate with the supplier the return of the 100 wrong thyristor packages. Contact should be again established with the supplier to find out about the status of the 40 mm transistor package.

Without immediate action, this item will not be available on time for project completion.

3.1.3. Materials

The critical item in the list of material is silicon.

Silicon wafers have been ordered from Wacker in Germany; the specified diameter is 2.0".

Although Wacker has accepted an order for 700 wafers of this size, it appears that this supplier will not be able to deliver this material on time and with the specified quantity.

With the limited availability of small size silicon wafers, and the lack of interest from the silicon suppliers to continue the production of silicon wafers with a diameter less than 3.0 inches, it becomes obvious that silicon device processing facilities should gear their equipment to handle at least 3.0" wafers. Although 4.0" diameter wafers would be a better choice, the equipment available at CEERI limits the size of the wafers to be processed to 3.0" maximum.

In order to permit the continuation of activities in power semiconductor device processing, it appears therefore that the present facilities

should be modified to handle 3.0" wafers.

Various discussions were conducted with CEERI scientists to investigate the requirements for 3.0" wafer processing.

Other silicon sources should be contacted. Possible sources are: Komatsu (Japan), Topsil (Denmark), SEH (US-Japan), Monsato (US)

3.2 Process & Facilities Evaluation

A batch of 33 wafers - 19 x 33 mm + 14 x 40 mm - was processed from diffusion to alloying (not included). The goal was to evaluate the processing steps involved and establish some yield figures for technology transfer. Since the batch was not fully processed, the yield figures could not be established. Process evaluation was based on the processing done on the wafer batch and a few additional experiments.

The following is an evaluation of the processes and facilities available at CEERI for the fabrication of Power Darlington Transistors. A summary of the facilities evaluation is given in Appendix II.

3.2.1. Tube Sealing

The tube sealing operation is performed with a Varian Evacuation System which operates in a satisfactory manner.

A new multiple nozzle torch system was installed to facilitate the sealing operation; it appeared however that the old system (more manual than the new one) is performing better. Activity to improve the system was therefore discontinued.

3.2.2. Gallium Diffusion (Closed Tube)

The Gallium diffusion (closed tube) was performed in a furnace tube available outside of the power device processing area.

A furnace tube (Tube # 3 on figure 6) is available in the

power device area and should be used for subsequent Gallium diffusion.

An Alumina tube liner (Mullite Tube) should be used to give support for the sealed quartz tube during closed tube diffusion. This liner would also provide support for the quartz - tube to be used for the open-tube Gallium Diffusion that CEERI is planning to investigate.

An Alumina liner of this kind can be obtained from the Mc Dand Refractory Co., in USA.

3.2.3. Oxidation

At time of processing no oxidation system was available (operational) in the power device area. The wafer batch was therefore oxidized by wet oxidation in other processing facilities.

Since then, a Pyrogenic Oxidation System has been installed. The Hydrogen Injector required for the system has been built by CEERI.

Pyrogenic Oxidation experiments are still being performed to evaluate the system operation.

There is a need in the oxidation area for reliable sources of High Purity Hydrogen and High Purity Oxygen (see paragraph 3.2.17 - Supporting Facilities).

3.2.4. Photo masking

Photo masking is performed in the "Yellow Room" of the Power Device Area, and in other photo masking facilities when precise alignment is required. The equipment of the power device area is outdated, and the space available is limited. There is therefore a need for more space and better equipment in this

area (Note: the purchase of a double side mask aligner is being planned by CEERI).

3.2.5. $POCl_3$ Diffusion

At time of processing, the $POCl_3$ system of the power device area was not operational; the batch of wafers was therefore processed outside of this area with other facilities.

Since then, the $POCl_3$ system in the power device area has been installed and is operational; this system is still under evaluation.

Here again, there is a need for a reliable source of oxygen (see paragraph 3.2.17).

3.2.6. Lapping

Lapping was done in a satisfactory manner, and the facilities available for this operation are sufficient and adequate. (The space available is however limited).

3.2.7. Slice Cutting (Laser Cutting)

Slice cutting is performed by means of the Trimming Laser of the Hybrid Facilities. This laser lacks power to perform efficient cutting; it is however the only laser tool available at CEERI to cut silicon wafers.

The software necessary to command the circular movement of the laser beam has been developed by CEERI and is now in operation.

The time required to cut one pellet with a diameter of 40 mm from a 2.0" wafer - 20 mils thick is about 30 minutes. (A dedicated laser would do the operation in 2-3 minutes).

3.2.8. Alloying

The alloying process, and its associated equipment, have been a problem area for several months. The new Vacuum Furnace which was received in 1986 has been in state of repair until the end of April 1987. A few temperature runs were then performed to proceed with the necessary control adjustments. A vacuum leak developed again in the vacuum chamber in the same location as before. Repairs were made with a high temperature weld alloy. Good vacuum ($\approx 10^{-6}$) can be now achieved at room temperature; high temperature tests have to be conducted to verify the quality and reliability of the new weld.

The goals in this area were to commission the alloying equipment, and establish the process for alloying the diffused transistor pellets to the molybdenum substrate using various alloy systems such as:

- Original Ag-Pb-Sb preform
- Aluminum Preform
- Aluminum/Silicon Preform
- Evaporated Aluminum on Silicon only
- Evaporated Aluminum on Silicon and Molybdenum

The Aluminum systems are lower temperature systems as compared to the Ag-Pb-Sb system which seems to produce unwanted stresses on the silicon during the high temperature alloying process.

The penalty for the use of the aluminum system resides in the difficulty in obtaining a good ohmic contact on n-type silicon material.

Since the vacuum furnace was not available, experiments

were performed with the old alloying furnace using Hydrogen as ambient; further experiments were also conducted by CEERI scientists at BHEL in Bangalore. The results of these experiments have not been yet fully analyzed to provide precise conclusions.

The alloying operation is becoming a critical step in device processing, and solutions must be provided quickly.

First, the equipment should be made fully operational and commissioned. The process should then be established using the original Ag-Pb-Sb alloy system, or the Aluminum system. Recognizing that aluminum is not the best choice material for ohmic contact to n-type silicon, one should further investigate the use of Al/Si eutectic alloy in order to limit the penetration of aluminum into silicon. The addition of a deep n^+ enhancement diffused layer on the collector side of the diffused wafer could also help in avoiding p-type conversion due to Aluminum. Also, since a higher Lead content in the ternary Ag-Pb-Sb alloy decreases the liquidus temperature, one should investigate the use of alloys with higher percentage of Lead. Tungsten, as a substrate material instead of Molybdenum, could also help in limiting the alloy penetration.

3.2.9. Metallization

The metallization operation is performed with Aluminum by means of a Sloan Electron Beam Evaporator System, and should not present any problem. There are however some quesions concerning the control of the deposited metal thickness and the repeatability of the process. The interested CEERI personnel should investigate the problems associated with this operation.

3.2.10 Sintering

As specified, this process calls for a heat treatment at 450^0C for 20 minutes in a Nitrogen atmosphere. The single tube THERMCO furnace to be used for this operation is not yet functional. The quartz tube is broken and should be fixed. The gas distribution system should be connected.

3.2.11. Bevelling

The bevelling operation is done on a SWAM Machine; this equipment is operational and the process is satisfactory.

3.2.12. Final Etch (Spin Etch)

The installation of the Spin Etch Machine required for the final etch operation has now been completed (the exhaust system must still be installed).

Since DI water is not available in this area, a DI water tank pressurisation system had to be designed and was built by CEERI to permit water distribution to the Spin

Etch Machine. This equipment is now operational. The evaluation of the final etch operaton has to be completed.

3.2.13. Passivation

Passivation is performed at CEERI using a Silicon Elastomer Compound (SES). This operation is done manually and appears to be well controlled.

Other passivation systems such as those using RTV, Varnishes, and Polyimide should be investigated.

3.2.14. Junction Testing and Final Tests

The equipment available for device testing includes a Tektronix 576 Curve Tracer with a High Current Plug-In Unit Fixture, a Transistor-meter from the LEM Company, and a Press Fixture from LEM to be used with the former equipment.

The Curve Tracer is used to check the voltages $BVCB_0$, $BVCE_0$, $BVEB_0$, and the associated leakages, the saturation voltage VCE (SAT), and the current gain hFE. This equipment is in operating order.

The switching parameters such as turn-on time, storage time, fall time, crossover time can be measured on the LEM Tester. This equipment allows also the measurement of VCE (SUS). The tester is operational, but in order to perform the tests on junction assemblies, or packaged devices, the Press Fixture must be connected to the test equipment. To reduce stray inductance to a minimum, the "Driver Rack" of the tester has to be located as close as possible to the test point in the Press Fixture (See

Fig. 7).

These modifications have yet to be done. Also required for the testing of junction assemblies (if the 40 mm package is not available) would be a test jig to hold the junction assemblies, and provide the proper electrode contacts to the device under test.

Additional equipment could be made available in this area to permit full device characterization. Safe Operating Area, Thermal Impedance, Thermal Fatigue are some of the additional tests that would be required for full evaluation of the devices being developed.

3.2.15. In-Process Control

All required in-process control equipment is available in this area.

The Sreading Resistance Profiling Equipment (SRP) has been however out of order for several months (years'). A computer malfunction seems to be the cause of the problem.

An extension board was built by CEERI to check the computer boards. The computer manual was obtained from the DEC Corporation in the US. The personnel, who has been trained in the US to take care of the maintenance of the equipment, has not been available long enough to accomplish any serious progress in repairing this equipment. Repair work is still in progress.

Additional visual inspection equipment should be added in this area. This includes a Stereo Microscope and a Metallurgical Microscope.

3.2.16. Assembly (Packaging)

The packaging operation is presently done by means of arc welding. A better technique would be Cold Welding by means of special Press.

CEERI has received information and quotation about such equipment from a US Company (ASSOCIATES GENERAL LABORATORIES). This equipment should be added to the present facilities.

The hermeticity and the quality of the package weld can be verified with a Leak Tester. Information about this equipment will be sent to CEERI.

3.2.17. Supporting Facilities

During the course of project experiments, it was not uncommon to run out of Oxygen, Hydrogen and Nitrogen gases. The supply of these gases is critical to the processing operations and therefore should be available where and when needed.

Since a gas plant with purification units is not yet in the planning, a solution to the gas shortage would be to install gas tanks with manifolds; the systems should be designed to provide enough supply and reserve.

DI water is not yet available in the Power Device Area. This creates some difficulties and problems in chemical processing. The DI water supply should be made available where needed in the Power Device Area.

3.3. New Process Evaluation

Some work was done in preparation of a new system for open-

tube Gallium diffusion.

If satisfactory this process could advantageously be used to replace the expensive closed tube process presently in use at CEERI.

The Gallium Source (Ga_2O_3) could not be procured during this assignment and therefore there was no activity in experimenting in this area.

3.4. Lecture Program

The Lecture Program was established as follows:

Lecture 1 - Power Modules

Lecture 2 - Triple Diffused Darlington Fabrication Process

Lecture 3 - Gate Turn-Off Thyristors

Lecture 4 - Semiconductor Device Thermal Meanagement

Lecture 6 - Review of CEERI Power Device Facilities & Process.

In addition to these lectures a presentation about Asymmetrical Thyristors (ASCRs) was made at the first National Seminar on AC Motor Devices for Transportation and Industrial Applications that was held at CEERI on April 15-17, 1987. The paper is available in the Seminar Proceedings.

Various meetings were also conducted with members of the Solid State Group to discuss subjects related to device design, processing, and testing.

3.5. Computer Simulation

The aim of this simulation was to correlate the computer results with actual test results, and verify the accuracy of the computer modelling as far as switching speeds are concerned.

The simulation was done by CEERI Scientists with selected values of lifetimes, base drives, and loads while awaiting for the test results.

The computer results are listed in the table of Appendix III.

The general conclusions are that the turn-off time is practically independent of the collector lifetime (τ_c), much dependent of the base lifetime (τ_B) and negative base drive (I_{B2}) - decreasing as τ_3 is reduced and I_{B2} is increased - and is affected by the type of load (being larger with inductive load than with resistie load).

The quantitative effect of these parameters can be seen in the table of Appendix-III.

In inductive load application, the resulting votage which appears during turn-off may exceed the device voltage rating and create breakdown problems.

Since not test results were available at the time of this writing, it was not possible to verify the accuracy of the computer predictions.

Further work is needed in this area to evaluate the performance and precision of the computer model.

3.6. Comparison between SCR/ASCR/GTO/TR Inverter Systems

A comparison between inverter systems utilizing SCRs, ASCRs, GTOs, and TRANSISTORS was made in order to answer some questions concerning the development of an electric vehicle using MICROPROCESSOR BASED A.C. MOTOR DRIVE. The relevant information is contained in Appendix III.

The system is a 30 KVA PWM INVERTER which requires devices rated at 200A RMS. A safety margin of almost 100% has been included in this rating (See Exhibit A in Appendix IV). For the dimensioning of the commutation components, it has been assumed that the current to be turned off was only 200A. A turn-off time of 20 μsec for the SCR devices, and 10 μsec for the ASCR devices was used to size the L-C commutation circuit of the SCR and ASCR systems.

The voltage rating was selected to be 1200V for the SCR, ASCR, and GTO devices, and 1000V for the transistor devices (the choice of a lower voltage rating for the transistors reflects the reduced availability of these components in the high voltage range).

The various system configurations (one inverter leg) are shown in Exhibit B of Appendix-III).

The SCR and ASCR Systems require a commutation circuit (L, C, A1 and A2) to turn-off the main switching devices (M1 and M2). There are non-polarized snubber circuits (RS, CS) across each switching component. The by-pass diodes, D1 and D2, handle the reactive current provided by the inductive load. Four gate drivers are needed to activate the four switching devices.

The GTO System has the advantage of not requiring the commutating circuitry of the former systems. The main switching devices, GTO1 and GTO2, are turned on and turned-off by their associated gate drivers (The power consumption of these gate drivers is much higher than that of the SCR/ASCR Gate Drivers since the turn-on current is much higher, and they also have to provide a large negative gate current to turn-off the device). A large polarized snubber circuit (DS, RS, CS) is required across each GTO in order to limit the dv/dt to a safe value. The by-pass Diodes, D1 and D2, have the same function as before.

The TRANSISTOR System basically has the same configuraion as the GTO System, except that the main switching devices are the Darlington Transistors, T1 and T2, and the basic drivers have less power consumption than the GTO drivers (but more than the SCR-/ASCR gate drivers).

The number of components required for each system is shown

in Exhibit C of Appendix. Due to the requirements of the commutation circuit, the SCR and ASCR systems employ more components than the GTO and TR Systems.

EXHIBIT D gives a Summary of the POWER LOSSES for each system with the overall system efficiency. The numbers shown on the table of EXHIBIT D must be divided by two to reflect the fact that each component of the system is active only half the time. The final results are given in the last two lines of exhibit D; these results are repeated below for clarification:

System / Power & Efficiency	SCR	ASCR	GTO	TR
TOTAL Power Dissipation (W) PT/2	3729	2342	2495	2361
Efficiency (η %)	87.6	92.2	91.7	92.1

From the above results, the most efficient system appears to be the ASCR System (η = 92.2%). The second most efficient system would be the Transistor System (η = 92.1%), followed by the GTO System(η = 91.7%), and finally by the SCR System (η = 87.6%).

Considering the approximations involved in this estimate, one should consider that the ASCR - GTO-TR Systems are equivalent in efficienty for this particular application.

The selection of one system over the others will depend then on the AVAILABILITY, COST, and RELIABILITY of the active components. Referring to EXHIBIT E of the Appendix-III, which gives a summary of the former results and other pertinent information, and considering the AVAILABILITY COLUMN, it appears that the

GTO System and the TRANSISTOR System should be the first and second choices for this application.

Note:

A precise conclusion on this matter would require a "Paper Design" of each system with an estimate of performance and cost. Building and evaluating actual systems would be the best way to a precise estimate.

3.7. Trends and New Devices

The trends in the Power Conversion Industry is towards the use of "turn-off" devices in converter applications. This excludes therefore the conventional thyristor devices. The latter however will still be used for many years to come in high power conversion applications without any risk of being replaced by other devices.

In medium power applications - up to about 300 KVA - the "turn-off" devices are becoming the workhorses of the Industry. The candidates are here the Power Darlington Transistors and the Gate Turn-Off Thyristors or GTOs. (The Power FETs have been here excluded as being low power devices in our power classification).

The advantages and disadvantages of the Darlingtons and GTOs have been extensively evaluated in theory and practice, but there is no universal rule available to decide which device should be preferred over the other. This can only be established for a specific application as described, for example, in paragraph 3.6 of this report.

In general, however, for applications where the voltage exceeds about 1200 volts, the GTO devices become the prime candidates due to the limited availability of Transistors at this voltage level and above.

Therefore, in addition to Transistors, GTO devices should be part of any development concerning pwer conversion components.

However, it is felt that GTOs are only "transition" devices that will probably be used until more efficient "turn-off" devices become

available. A GTO project should therefore be a "short term" project with a maximum completion time not exceeding two years.

The next generation of power devices should offer power handling capability combined with high switching speeds. These devices will make use of "Field Effect Control" or "Static Induction Control" to operate efficiency at elevated switching speeds and powers. There are now some devices of this kind available in Japan.

The development of such devices would involve LSI processing techniques combined with large area device processing. Due to the processing complexities involved here, a static Induction Device Project would be a long term (3 to 5 years) program and would require new types of expertises.

In addition to "turn-off" devices, the Medium Power Conversion Industry appears to have selected the Power Module Packaging configuration as the preferred device encapsulation system. These Modules may contain Transistors, Thyristors, Diodes, GTOs, Power FETS, or combination of these devices. They offer electrical isolation which make them convenient to use and, whenever possible, they are generally selected over any other form of device packaging. Therefore Power Modules should also be part of the power components family. The development of Power Modules is relatively simple and a project in this field could be a "Short term" program (2 year max.)

At the present time, it appears that the Power Conversion Industry needs:

- Power Transistors
- GTOs
- Power Modules (Containing Transistors or GTOs)
- and, SI Devices for the future.

CEERI has now acquired the expertise in Power Transistor Technol-

ogy, the GTO Technology could be derived from the Transistor Technology without any major difficulty. The Power Module Technology requires Semiconductor Device Tekchnology, Hybrid Circuit Technology, and Plastic Packaging Technology. The first two Technologies are available at CEERI; the latter could be easily acquired.

The components of the SI Device Technology exist at CEERI. They will have, however, to be combined to produce the specified devices. The efforts required to make this technology integration will be at a much higher level than those required for making GTO or Power Module Devices.

4. CONCLUSIONS & RECOMMENDATIONS

Project accomplishments were limited due to various causes mainly related to equipment installation and repair. In several instances, lack of high purity gases was the cause of the delay. Limited silicon supply restricted the number of processed wafers.

At the moment, there are several identified problem areas:

The package availability problem must be quickly solved in order to preseve the continuity of the project.

The Silicon availability should be confirmed by the present supplier, and other silicon sources should be investigated.

To limit the impact of the limited supply of small size silicon wafers, processing capability for 3.0" wafers should be implemented at CEERI.

A satisfactory alloying process should be developed and applied to transistor processing. (The new vacuum furnace should be available to perform this operation). This is a critical process area and solutions to the associated problems must be found quickly in order to allow project continuation and completion.

The test facilities should be fully installed to permit device characterization.

The repair of the profiler equipment (SRP) should be completed. Supporting facilities should be made available where needed. A detailed list of actions to be taken is given in Appendix-V.

In view of the future needs of the Industry and the Silicon Device Competence developed at CEERI, it is recommended that future work on advanced power devices be supported by UNIDO.

The concerned Industry could be involved at the inception of the Project to permit a smooth transfer of Technology.

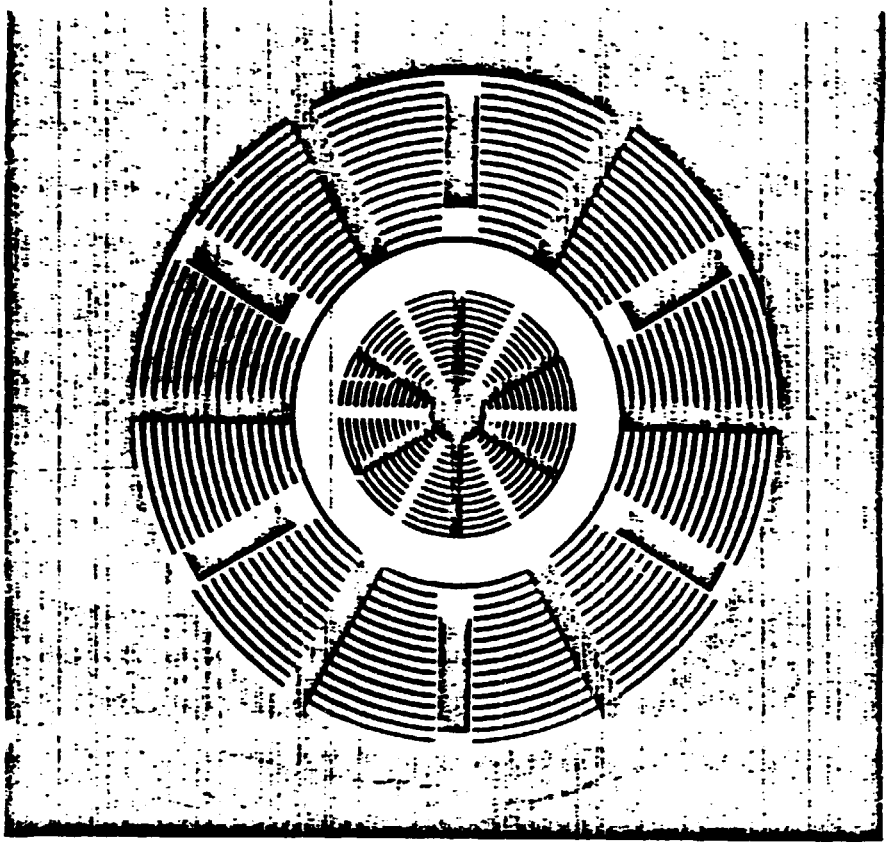


Fig 1. 300A Darlington Transistor.
Emitter/Base Configuration

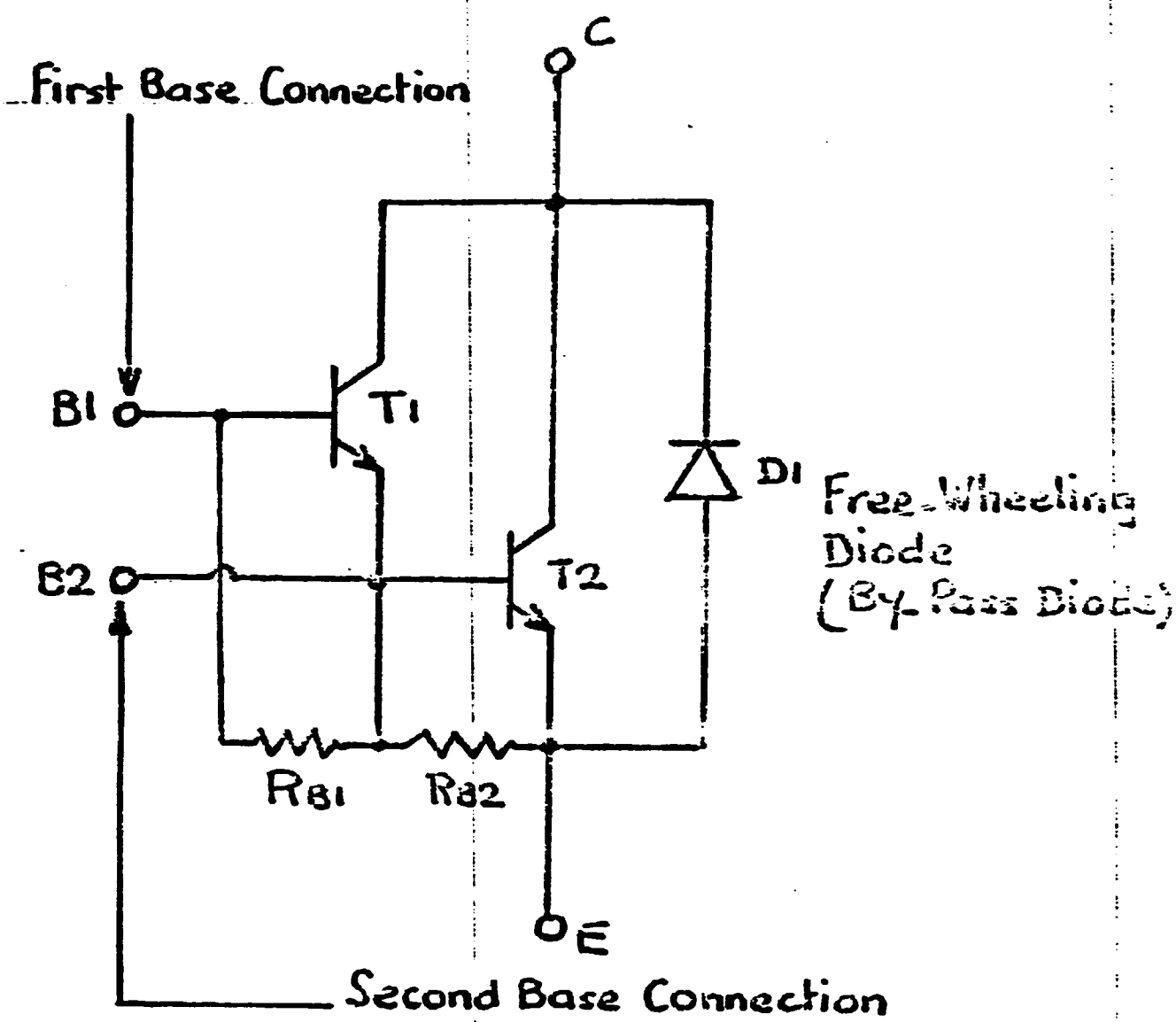


Fig 2 . Darlington Transistor Schematic

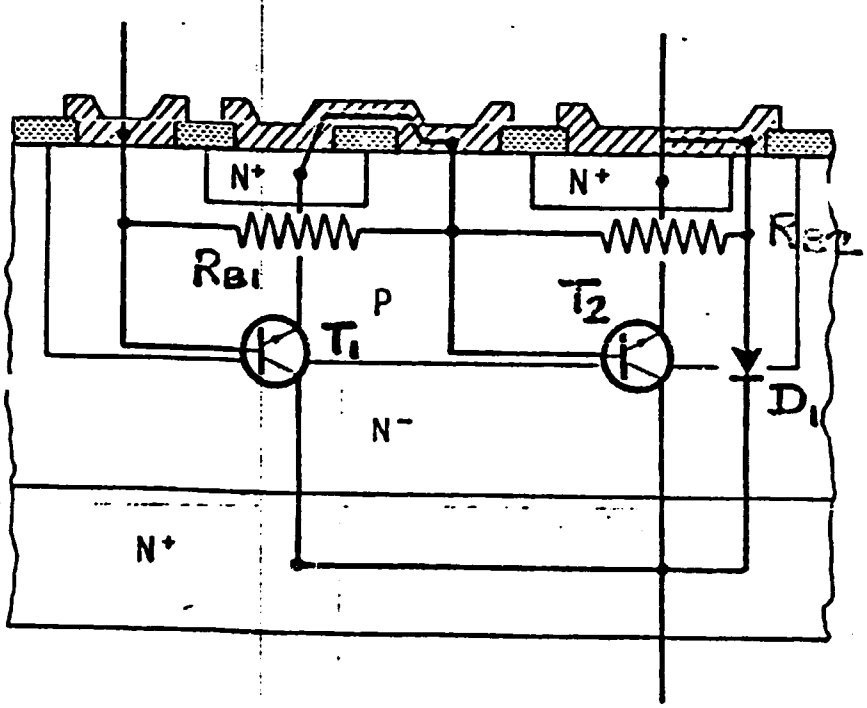


Fig 3. Transistor and By-Pass Diode Connection

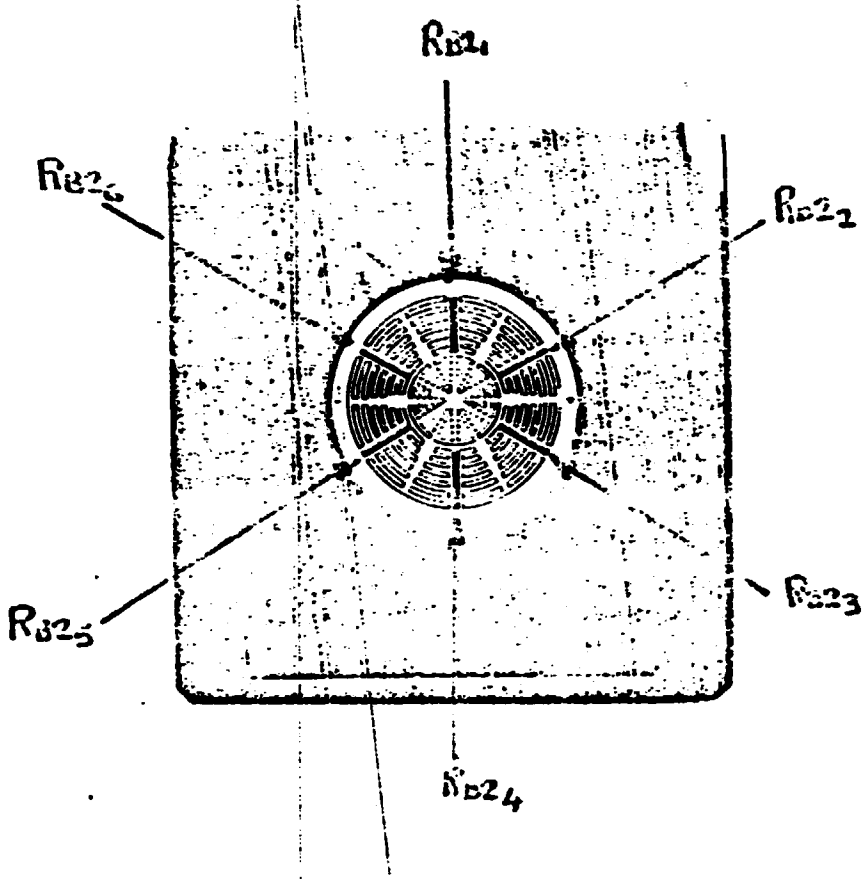
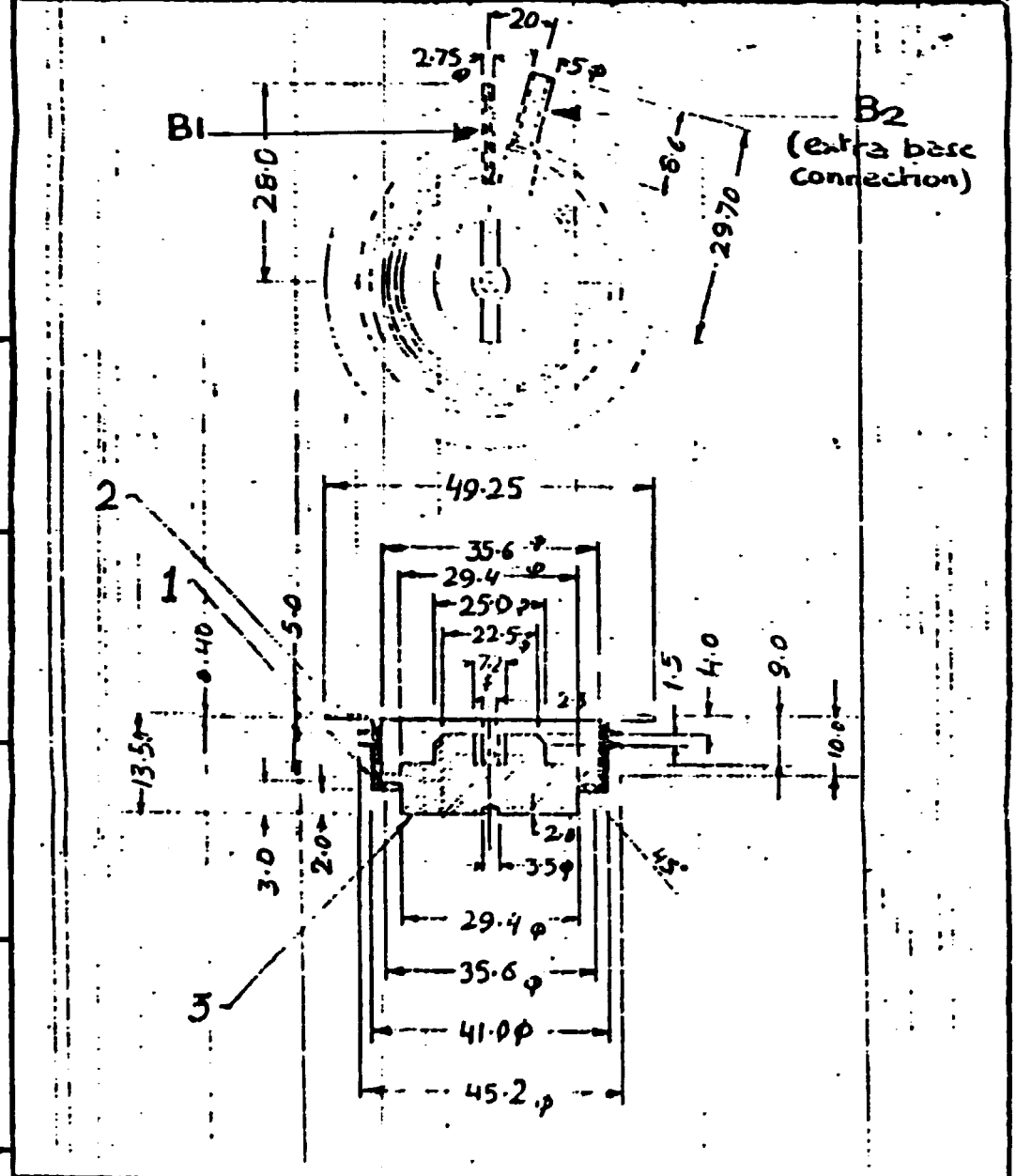


Fig 4. New Mask (Without By-Pass Diode)



DIMENSIONS IN MM	GEN. TOLERANCE	COATING	NO OFF

TITLE: HOUSING (Ceramic to metal Seal) 40 mm fusion facility	DRG. NO. SSD/DRT/1-85	
	SCALE	WEIGHT
	SHEET NO.	SHEETS
MATERIAL 1:- CERAMIC 2:- COPPER NICKEL PLATED 3:- COPPER NICKEL PLATED	CEERI PILANI (Raj)	

DESIGNED			
DRN.			
TCD.			
CHD.			
APP.			

1ST APPLICATION

Fig 5. - 300A Darlington Package (Housing)

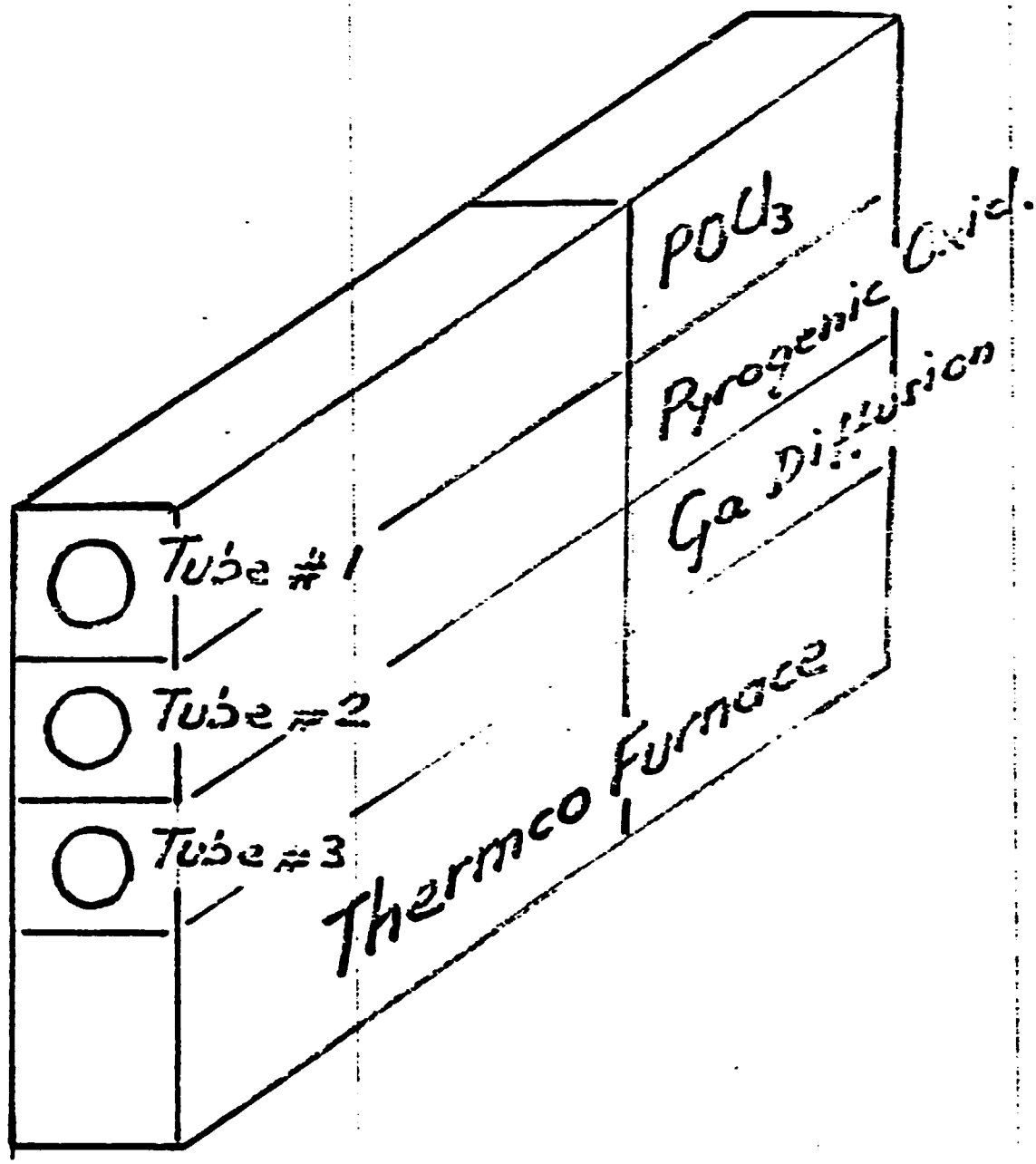


Fig 6. Power Device Laboratory - Diffusion Tube Location

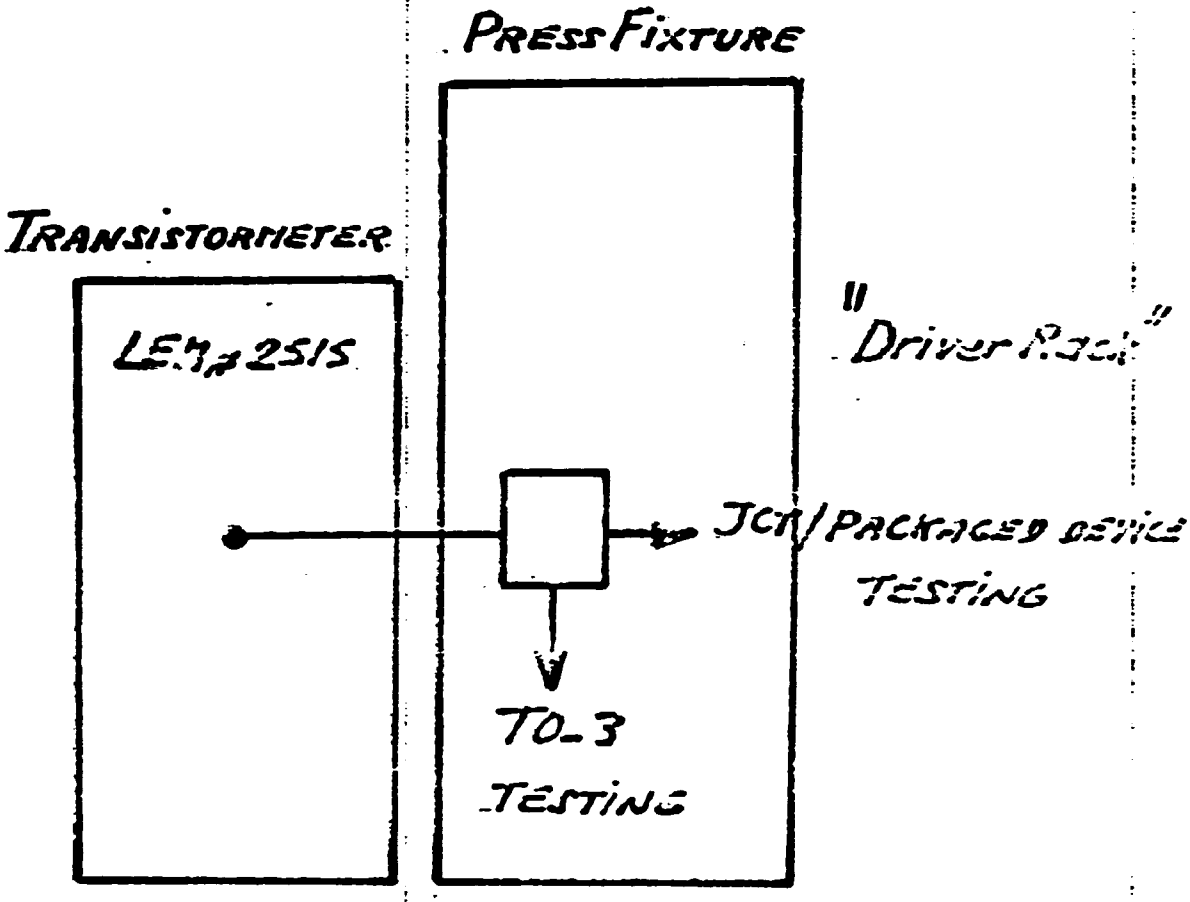
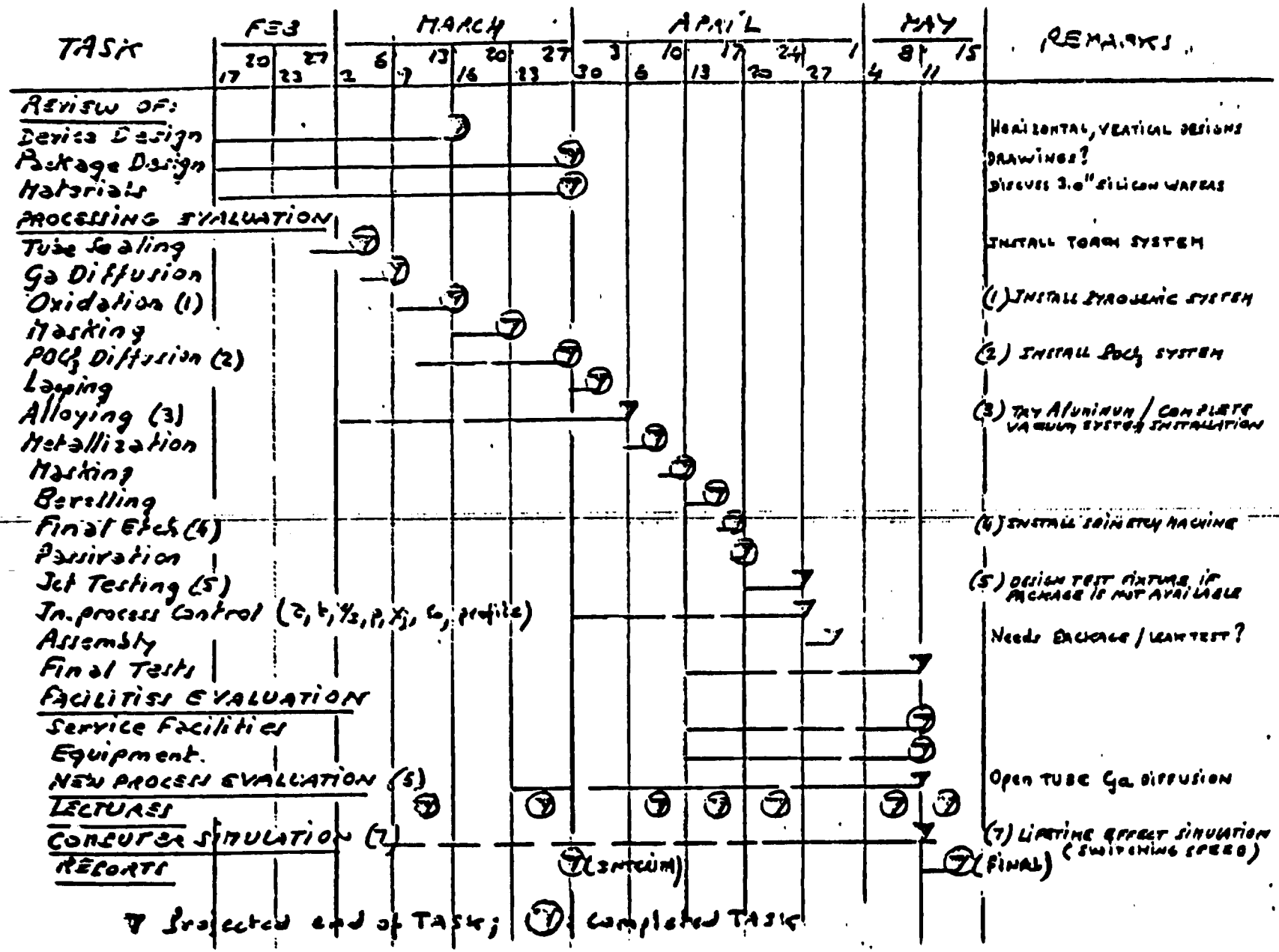


Fig 7. Transistormeter / Press fixture Connection


TASK
FEB
MARCH
APRIL
MAY
17 20 23 27 2 6 9 13 16 20 23 27 30 3 6 10 13 17 20 24 27 1 4 8 11 15
REMARKS
Review of:
Device Design
Package Design
Materials
PROCESSING EVALUATION
Tube Sealing
Ga Diffusion
Oxidation (1)
Masking
POCl3 Diffusion (2)
Lapping
Alloying (3)
Metallization
Masking
Beveling
Final Etch (4)
Passivation
Jet Testing (5)
In-process Control (x, t, Rs, R, Xj, Co, profile)
Assembly
Final Tests
FACILITIES EVALUATION
Service Facilities
Equipment
NEW PROCESS EVALUATION (6)
LECTURES
COMPUTER SIMULATION (7)
REPORTS
HORIZONTAL, VERTICAL DESIGNS
DRAWINGS?
DISCUSS 3.0" SILICON WAFERS
INSTALL TORCH SYSTEM
(1) INSTALL PYROGENIC SYSTEM
(2) INSTALL POCl3 SYSTEM
(3) TRY ALUMINUM / COMPLETE VACUUM SYSTEM INSTALLATION
(4) INSTALL SCRIBETECH MACHINE
(5) DESIGN TEST FIXTURE IF PACKAGE IS NOT AVAILABLE
Needs PACKAGE / LEAK TEST?
Open TUBE Ga DIFFUSION
(7) LIFETIME EFFECT SIMULATION (SWITCHING SPEED)
(INTERIM)
(FINAL)
▼ Projected end of TASK; ⑦ Completed TASK

FACILITIES EVALUATION

OPERATION EQUIPMENT	TO BE INSTALLED	INSTALLED	TO BE FIXED	TO BE EVALUATED	UNSATISFACTORY	REMARKS
TUBE SEALING					X	- New Torch System is not satisfactory (See paragraph 3.2.1)
Ga DIFFUSION	X			X		- Needs a Mullite -Tube Liner - Closed Tube & Open Tube Diffusion in same liner
$POCl_3$ DIFFUSION		X		X		- Needs N_2-O_2 Supplies
PYRO - OXIDATION		X		X		- Needs N_2-O_2-H_2 Supplies
PHOTO MASKING					X	- Space is limited - Double-Side mask Aligner is being ordered.
LAPPING					X	- Space is Limited
ALLOYING		X	X	X		- Space is Limited - New Vacuum Furnace to be repaired
METALLIZATION					X	- Deposited metal thickness is not well controlled
SINTERING		X	X	X		- Furnace tube must be repaired
EDGE PROFILING					X	
FINAL ETCH		X		X		- Needs DI water supply
PASSIVATION					X	
IN-PROCESS CONTROL			X			- SAP Equipment out of order - being repaired. - Stereo Microscope/metallurgical.

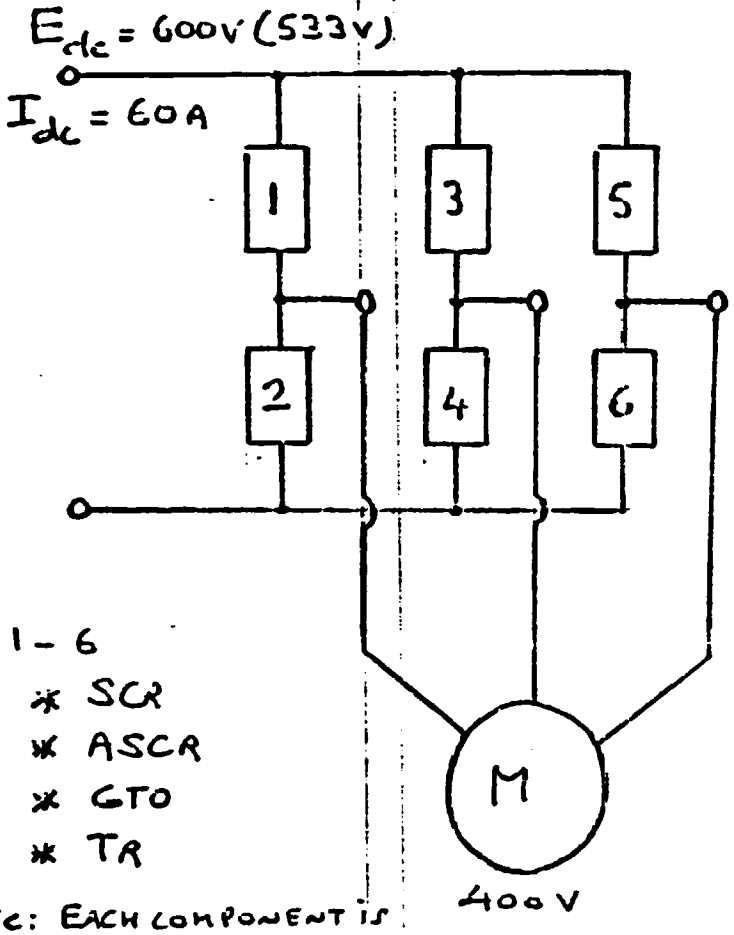
[illegible] equipment	To Be INSTALLED	INSTALLED	To BE FIXED	To Be EVALUATED	OPERATIONAL	Remarks
TESTING	X					- Press Fixture to be constructed at Transistorator - Testing Jig to be built
ASSEMBLY	X					- Needs Cold weld Press (Leak Tester)

COMPUTER SIMULATION RESULTS

BASE DRIVE →		$I_{B1}=1A; I_{B2}=0$				$I_{B1}=1A; I_{B2}=-5A$			
LOAD →		RESISTIVE		INDUCTIVE		RESISTIVE		INDUCTIVE	
LIFETIME τ_c (μsec)	τ_B	t_{off} (μsec)	V (V)	t_{off} (μsec)	V (V)	t_{off} (μsec)	V (V)	t_{off} (μsec)	V (V)
5	8	8.8	452	11.3	560	4.75	408	/	/
8	8	8.9	454	11.0	594	4.8	429	7.0	676
18	8	8.9	449	11.0	606	4.9	444	/	/
18	2	6.4	454	7.5	641	3.45	440	/	/

30kVA PWM INVERTER

(f_{com} = 1,500 Hz max)



1 - 6
* SCR
* ASCR
* GTO
* TR

Note: EACH COMPONENT IS ACTIVE ONLY HALF THE TIME

$$I_{RMS} = \frac{30000}{\sqrt{3} \cdot 400} \times 2.5 = 108\,A$$

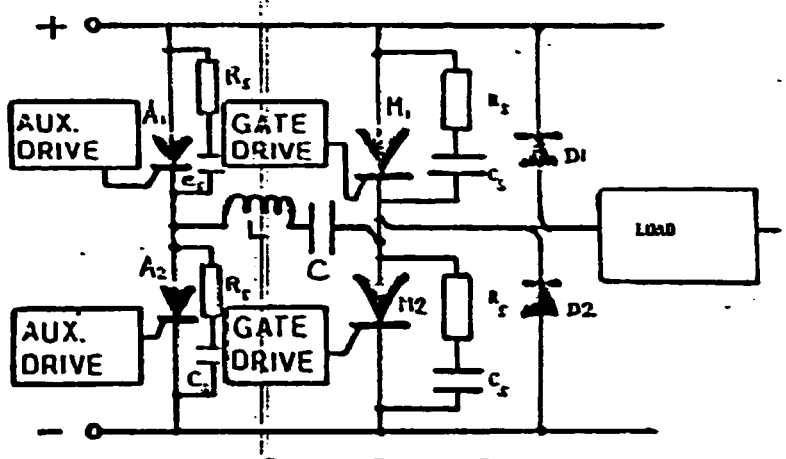
(2.5: STARTING; 108 A → 200A RMS DEVICE)

VOLTAGE ≥ 1000V

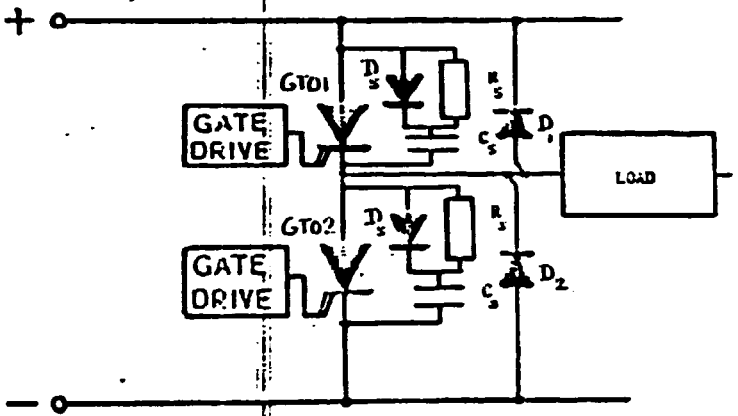
SCR, ASCR, GTO : $V_{DRM} = 1200V$

TR : $V_{CE} = 1000\,V$

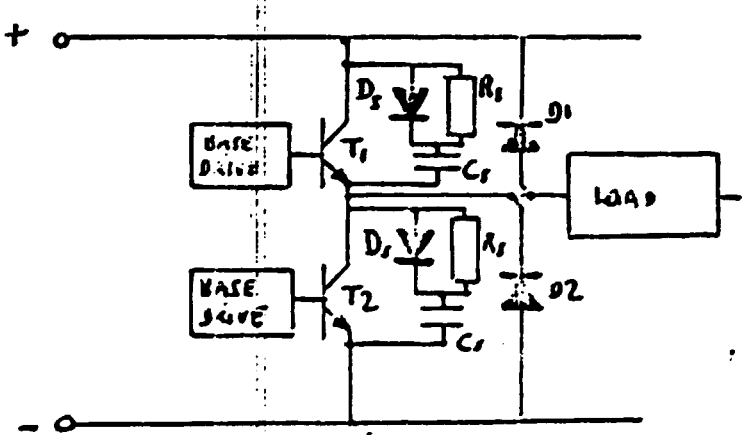
Exhibit A



SCR SYSTEM
ASCR



GTO SYSTEM



TRANSISTOR SYSTEM

Exhibit B

Nb of components

INVERTER TYPE / COMP.	SCR	ASCR	GTO	TR
Power Cont.				
MAIN	6	6	6	6
AUX.	6	6	/	/
BP DIODE	6	6	6	6
SNUBBER				
D_S	/	/	6	6
C_S	6x2	6x2	6	6
R_S	6x2	6x2	6	6
Commut. Cont.				
L	3	3	/	/
C	3	3	/	/
DRIVER (MAIN)	6	6	6	6
DRIVER (AUX)	6	6	/	/

Exhibit C

INVERTER LOSSES

Power \ Inverter Type	SCR	ASCR	GTO	TR
$P_{cond.}$	720/2	540/2	540/2	432/2
P_{sw}	1620/2	1050/2	2260/2	2160/2
P_{com}	4050/2	2025/2	/	/
P_{snub}	648/2	648/2	1620/2	1620/2
P_{DR}	60/2	60/2	210/2	150/2
P_{BP}	360/2	360/2	360/2	360/2
P_T	7,458W/2	4,683W/2	4,990W/2	4,722W/2
Power Dissipation & Efficiency				
$P_T/2$	3,729	2,342	2,495	2,361
$\eta\%$	87.6	92.2	91.7	92.1

Exhibit D

ANNEXURE-A

80 KVA, 3 Phase Inverter

(D.C. Supply Voltage: 600 volts, I d.c. max. 200A)

Comparison of Transistor Inverter, Thyristor (SCR) Inverter & GTO Inverter

Parameter	Transistor	SCR	GTO	ASCR
Switching Losses	1080	810	1130	525
Power Losses (Total)	2361	3729	2495	2342
No.of Semiconductor Devices *	12	18	12	18
No. of Electromagnetic Devices & snubber devices (L,S,R)	30	18	30	15
EMI	?	?	?	?
Acoustic Noise	72dB	83dB	72dB	80dB
Speed/Frequency Range (KHz)	20	10	15	15
Capital Cost **	.90	1.0	.70	.80
Running Cost including maintenance	?	?	?	?
Need or need not commutating circuit	NO	YES	NO	YES
Volume (Equipment)	.90	1.0	.70	.80
Reliability ?	.95	1.0	.95	1.0
Availability (Device)	.60	1.0	.70	.50
Cost (Device)	2.50	1.0	2.50	2.0

* SNUBBER DIODES NOT INCLUDED

** POWER DEVICES NOT INCLUDED

Exhibit E

APPENDIX V

ACTION TO BE TAKEN

1. **DEVICE DESIGN**

   - Evaluate Design without By-Pass diode
   - If satisfactory, apply design to 300A Transistor

2. **PACKAGE**

   - Provide detailed drawings of all parts
   - Re-order 100A transistor packages
   - Return the wrong 30 mm packages
   - Discuss 40 mm Transistor Package and order
   - Evaluate other package sources

3. **SILICON**

   - Get a statement from Wacker about present order
   - Find out what is the prospect for future orders of this size (2.0")
   - Evaluate other silicon sources
   - Retrofit facilities to handle 3.0" wafers.

4. **PROCESS**

   - Investigate Al vs Ag-Pb- Sb alloying system
   - Investigate use of Tungsten as Substrate
   - Investigate Mesa Etch
   - Evaluate Pyrogenic Oxidation system
   - Evaluate $POCl_3$ diffusion system
   - Evaluate new Open-Tube diffusion System

- Evaluate Spin-Etching
- Ensure that Al Evaporation is operating properly
- Provide detailed process instructions.

5. EQUIPMENT

- Commission Vacuum Alloying Furnace
- Complete Spin Etch Machine Installation
- Complete Sintering Furnace Installation
- Complete Test Facilities
- Complete SRP Machine Repair
- Supply Mask Aligner
- Supply Stereo Microscope
- Supply Metallurgical Microscope
- Supply Additional Test Equipment

6. SUPPORTING FACILITIES

- Provide DI Water supply where needed
- Provide N_2 supply where needed
- Provide O_2 supply where needed
- Provide H_2 supply where needed

7. DEVICE CHARACTERIZATION

- Evaluate available devices
- Procure equivalent commercial devices
- Compare CEERI devices to commercial devices
- Establish precise specifications
- Establish test procedures.

8. COMPUTER SIMULATION

- Correlate measured results to computed results and evaluate

9. MISCELLANEOUS

- Document all experiments and report.