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SEMICONDUCTOR DEVICES AND ELECTRONIC
SUB-SYSTEMS FOR TRANSPORTATION

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INDIA

Technical report: Solid State AC Drives using GTO's for Transportation *

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of K. Matsuse,
Expert in Power Electronics

Backstopping Officer: J. Fürkus, Engineering Industries Branch

United Nations Industrial Development Organization
Vienna

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ABSTRACT

This is a report of consultation and assistance provided by me as a UNDP Consultant to CEERI for the period February 26, 1987 through March 24, 1987. The object was to contribute to the UNDP/UNIDO Project Research by CEERI to devise Electronic Systems for AC Motor Drives to use in transportation application. During this period, five lectures were presented on technical topics relevant to variable frequency motor drives and application of GTO thyristors. In addition, two of the five lectures were using the Over Head Projector using my free hand transparencies: the technical substance of the remaining lectures was using a slide projector.

Technical advice was provided on:

(a) Efficiency improvement techniques for the inverter fed induction motor drives.

(b) Accoustic noise measurement.

(c) Reduction on electro magnetic interference measurement.

(d) The design consideration techniques of GTO gate drive circuit, Snubber circuit, Circuits inductance reduction and the equipment layout of the GTO inverter for transportation inverter-induction motor drives.

(e) Technical suggestion was provided on protecting techniques of the induced electromagnetic wave obstraction to communication line for transportation inverter-AC motor drives.

The support concludes with suggestions and recommendations for further work in related topic.

1. INTRODUCTION

I arrived in Delhi on Thursday evening, February 26, accompanied by my wife. We met the travel agent at the airport and received my return flight ticket from Delhi to Tokyo. Then we went to CSIR Science Centre. On Friday, Mr. P.K. Mukherjee, Administrative Officer, CEERI alongwith Mrs. Bhalla came to meet us and escort us at Science Centre. I was taken to the UNDP office at 55-Lodi Estate escorted by Mrs. Bhalla. In UNDP office, I received a briefing on my assignment from the officer and then received funds from the Finance Officer after lunch we went to the CEERI office in Delhi. We left Delhi by car at 3.30 PM and arrived at the Sidhu Guest House in Pilani at about 8.00 p.m. We ate our evening meal and then retired. On saturday evening, Dr. G.N. Acharya, Director of CEERI and his wife invited us to our welcome dinner.

On Monday morning, March 2, Dr. G.N. Acharya met us at the Guest House and took me to CEERI. Dr. Acharya described CEERI activities; we visited laboratory; I had further general discussions with Dr. Acharya, Mr. U.M. Rao, Mr. Perlekar and Mr. Vinod N. Walivadekar on plans for my work. We agreed that I woul first present five lectures starting on 10th March, 87 at 4.30 PM and continue daily one lecture - I prepared a draft of the titles for the lectures which were reviewed by Dr. Acharya and then revised and finalised. After mutual discussions with power electronics group we decided to work on following topics:-

1. Measurement and Reduction of Acoustic Noise from Inverter fed induction motor.

2. GTO Inverter Considerations.

3. Efficiency Improvement techniques for inverter drive

2. EXPERIENCES AND WORK PERFORMED IN PILANI

2.1: Lectures

The following lists of the five lectures were presented in the CEERI Auditorium.

March 10	:	Research activities at Meiji Univ., Tokyo.
March 11	:	Analysis and Characteristics of New Current Source GTO Inverter Fed Induction Motor (1),(2)
March 12	:	Improved Current source GTO Inverter for High Frequency Induction Motor Drive (3)
March 13	:	Steady State Analysis of Inverter Fed High Frequency Induction Motor Drives (4).
March 18	:	Application of GTO, Design Consideration for Circuits and Application of GTO for AC traction drives (5) - (10)

The technical substance of the lectures was presented using specially prepared visual aids with the slide projector (March 11. 12 and 13) and the over head projector using my free-hand transparencies.

2.2: Measurement & reduction of acoustic noise

(A) Accoustic noise reduction is Induction Motor causes of Accoustic noise generations.

Accoustic noise in Induction Motor is generated due to following factors:

(1) Mechanical Noise.

There are two types of noise:

(a) Wind noise.
(b) Magnetic noise of the unbalanced circuit.

(2) Harmonic Noise.

This will be present when the Input to the motor contains Harmonics.

(B) Sensitivity of Human Ear to the sound

The sound level attenuation as a function of frequency of Human Ear is shown in fig. 1.

From the figure, it is clear that the ear is most sensitive in the frequency range 1 KHz to 4 Khz.

The sensitivity decreases towards low frequency as well as towards higher frequencies.

This suggests that the accoustic noise should be minimised in the frequency range between 1 KHz, where as relatively higher level of noise can be tolerated frequencies go below 1 KHz or go above 4 KHz.(11)

(C) Nature of the Accoustic Noise

(i) The accoustic noise increases with the fundamental frequency except with PWM waveform, in which case, it slowly increases up to 25 Hz and then decreases with frequency.

(ii) At any frequency with V/f constant the accoustic noise with PWM and PAM is more than in case of sine wave.

(iii) up to 2.5 Hz Noise with is more than that due of PAM where as above 25 Hz, it is vice-versa.

(iv) Harmonics noise is in pulses and the frequency depends upon the switching frequency.

(D) Suggestions for reduction in Accoustic noise

Mechanical Noise

The wind noise and magnetic noise can be reduced the following way.

(i) The phasewise symmetry should be maintained in the mechanical structure of the machine.

(ii) The magnetic circuit of the machine should be as balanced as possible.

(iii) The mechanical mounting of the machines should be tight so as to reduce the mechanical vibrations. This is because if the frequency is closing near to the mechanical resonance frequency the noise and vibrations are amplified:-

(iv) Space harmonic flux is reduced by an increased length of air gap.

Harmonic Noise

In order to reduce noise due to harmonics which are generated in non-sinusoidal input. The following are suggested.

The switching of the non-sinusoidal pattern is to optimise that.

(i) Least harmonics are generated in the frequency range between 1 KHz to 4 KHz, where human ears are most sensitive.

(ii) Harmonic frequency (Apparant switching frequency) may be shifted at higher frequency side where ears are less sensitive as shifting it to lower frequency side may cause torque pulsation.

(E) Suggestion for Measurement of Noise power

When measuring the total noise power with level meter, a filter may be used, whose characteristic is similar to that of the ear so the readings are more near the real and its effect may be better understood.

(F) Experimental Observations

A measurement set-up was prepared to conduct acoustic noise measurement. The measurements were conducted with following equipment.

(i) Ohmidirectional microphone having 60 db sensitivity.

(ii) Audio amplifier with 60 db gain.

(iii) Spectrum Analyser.

(iv) Two special low voltage AC Induction Machine.

(v) 40 KVA PWM Inverter.

(vi) D.C. Generator for loading the motor.

The observations are given in table I,II and III. It may be noted that the noise picked up by microphone consists of Inverter, both machines and environment noise.

TABLE-I

(i) Fundamental Frequency : 5.8 Hz, PWM waveform

(ii) Distance of Microphone from Induction Motor : 0.5 Meter

(iii) Condition : Induction Motor without load

Noise Frequency	Amplitude in RMS
100 Hz	2.51 V
196 Hz	0.27 V
364 Hz	0.23 V
456 Hz	0.15 V
544 Hz	0.60 V

TABLE-II

(i) Fundamental Frequency : 10 Hz, PWM waveform

(ii) Distance of Microphone from Induction Motor : 0.5 meter

(iii) Condition : Induction Motor without load

Noise Frequency	Amplitude in RMS
32 Hz	0.31 V
98 Hz	2.84 V
128 Hz	0.38 V
160 Hz	0.15 V
230 Hz	0.56 V
268 Hz	0.47 V
322 Hz	1.07 V
452 Hz	0.42 V
644 Hz	0.62 V

TABLE-III

(i)	Fundamental Frequency	: 15 Hz, PWM waveform
(ii)	Distance of Microphone from Induction Motor	: 0.5 meter
(iii)	Condition	: Induction Motor wihout load

Noise Frequency	Amplitude in RMS
32 Hz	0.20 V
96 Hz	2.72 V
232 Hz	1.26 V
316 Hz	0.72 V
469 Hz	1.45 V

2.3: GTO inverter design consideration

Following topics were discussed in details

2.3.1 GTO gate drive circuit.

2.3.2 Turn on and Turn off snubber circuits.

2.3.1 GTO gate drive circuit

In order to turn on the GTO, it is necessary to feed a turn on (forward) current to the gate. The typical current waveform is shown in fig. 4. The turn on gate current consist of two parts. The first part provides the required rise time and the peak gate current while the other part provides average on state gate current. This current is required to maintain (VAK) on state voltage drop to minimum.

To turn off the GTO, a negative voltage is applied to the gate with respect to cathode. The turn off mechanism can be explained by two transistor analogy shown in fig. 2.

When gate is applied negative bias with respect to cathode then the BE junction of T2 is reversed biased and the collector current of T2 decreasing which results in further decrease of IC1, so the rate rise of reverse voltage and permissible reverse voltage and current dictates the turn off time and mechanisms.

The circuit discussed in detail is given in fig. 3

To turn on the GTO transistor Q1 is turned on the capacitor C3 discharges through R1 and GK junction of the GTO providing first pulse and sufficient rise time. Later on capacitor C1 discharges through R2 and R1 GK junction of the GTO providing average gate current. To turn off the GTO transistor Q2 is turned on causing negative voltage connected to the gate. The zener diode-diode network is used to emit reverse voltage to the safe operating limit.

(2) Snubber Circuit

The recommended circuit for snubber is as shown in fig. 5.

It is common practice that manufacturers of GTO provides the value of Cs depending on load current.

The value of Rs is mainly decided by permissible discharge current and the reapplied dv/dt of the device.

The turn on di/dt choke is decided similar to that of thyristor but Ri and Di are essential to dissipate the stored energy in the choke. The diode selected for Ds and Di should be of High Frequency type the di/dt choke should be air core multiturn with current carrying capacity same as that of GTO. Other snubber circuit discussed were shown in fig. 6(a),(b).

Designing GTO gate drive circuit

Gate turn off thyristor under considerastion is SG 300U11 (Toshiba)

Specifications

VDRM	:	1600 V
IT (RMS)	:	120 V
ITGQM	:	300 A
Peak forward gate voltage	:	15 Volts
Peak forward gate current	:	15 Amp.
Minimum gate on state voltage	:	1.2 volts.
Minimum gate on state current	:	0.5 Amp.
Gate turn off voltage	:	20 V.
Gate turn off current	:	80 Amp.
Storage time	:	13 μs
Gate turn off time (Tga)	:	16 μs
Tail time	:	58 μs

In figure 3 ,C1 is the filter capacitor and depends on power supply ripple. To reduce the ripple content generally high frekquency square wave A.C. source is used. The output of this source adjusted to voltage requirements of GTO for turn on and turn off by providing transformaer tapping (S1, S2 in fig.3).This o/p rectified and filtered using C1 and C2 capacitors.

The first pulse requirement of GTO decides the value of R2 and C3. The peak gate current and peak forward gate voltage decides the continuous collector current and VCEO of transistor Q1.

The capicitor C3 is charged to VD when the transistor Q1 is turned on, the capacitor C3 first discharges through R2 and gate eathode junction of GTO providing sufficient rise time and peak forward gate current.

The peak forward gate current - 15 Amp.
The peak forward gate voltage - 15 volts.

Then $R2 = \frac{15\text{volts}}{15\text{ Amp}} = 1$ ohms.

The value of C3 depends on permissible rise time of forward gate current.

$$\frac{di_{FG}}{dt} \text{ for SG300U11 is } 7 \text{ A}/\mu\text{s}$$

Relation between tw and (R2C3) capacitor time constant is empirical and is given by

$$0.5\ t_w = \frac{1}{3}(R_2C_3)$$

C3 can be calculated with R2 known tw is defined in data sheet as ton for SG300ull ton-7.0 and td-2 μsec.

$$t_w \cong 1.5\ t_{on}$$

$$\cong 10.5\ \mu s$$

$$C_3 = \frac{0.5 \times 3\ t_w}{R_2} = 15.75\ \mu F$$

Since the avg. on state current is 500 mA for SG 300U11 therefore the value of R1 is calculated

$$R_1 = \frac{V_D}{I_{FG(av)}} = \frac{15}{500\ mA} = 30 \text{ ohms}$$

To turn the conducting GTO to off state requires a negative voltage across GK junction by turning on Transistor Q2, -Vs is connected to gate of GTO. The capacitor C2 discharges through gate cathode junction via transistor Q2. The maximum permissible GK reverse voltage is specified in manufacturer data sheet. To limit the reverse voltage zenerdiode-diode (ZD-D) is connected across gate cathode as shown in fig. 3. The turn off gate current required for turning off the anode current is 80 Amp and maximum reverse voltage is 20 volts. Transistor Q2, VCEO should be more than Vs and the collector current must be at least 1.5 times the peak gate current.

The most important point in GTO gate drive circuit is the wiring inductances should be as small as possible and the gate cathode leads must be twisted to cancel the inductive effects.

2.3.2:<u>Analysis of Snubber Circuit</u>

The generally recommeded circuit for GTO snubber is as shown in fig.6(c) along with half bridge.

The snubber circuit component plays important role in limiting voltage spike and over shoot and to protect the device from damaging due to excessive rate of rise of on state Anode current. The wiring inductances plays very dominant role is generation of voltage spikes and overshoots. Therefore, the equivalent circuit along with wiring inductances should be considered, while designing snubber circuit component and its influence on overall system performance. Fig. 6(c) indicates the GTO half bridge circuit with all leakage inductances.

The circuit operation is divided in three parts.

Mode 1 Assume load current IT is constant through out turn off process and the GTO G1 is conducting.

At any instant to the GTO G1 is applied turn off pulse. Then the voltage drop across GTO slowly rises and the Anode current of GTO slowly decreases. During this period the snubber capacitor starts charging through Ds and load, maintaining load current constant.

$$i_A \rightarrow i_s$$

$$\frac{di_{G1}}{dt}(l_1+l_2)+V_{AK} = \frac{di_s}{dt}(l_3+l_4)+\frac{1}{C_s}\int i_s dt$$

$$i_{G1} = I_T - i_s$$

$$V_{AK} = (l_1+l_2\; l_3+l_4)\frac{di_s}{dt}+\frac{1}{C_s}\int i_s dt$$

$$V_{DP} = L_{DP}\frac{di_s}{dt}$$

where $L_{DP} = l_1+l_2+l_3+l_4$

or $V_{DP} = -L_{DP}\dfrac{di_{G1}}{dt}$

Mode 2 During this period GTO turn off. The capacitor current is almost constant. This situation prevails till the capacitor voltage becomes equal to Edc.

Mode 3 In this mode capacitor start over charging. Thus Diode is reverse biased and the capacitor charges through RS. The capacitor current starts decreasing and now the load current is supplied by diode D4.

In this case

$$E_d = (l_3+l_4+l_5)\frac{di_s}{dt}+\frac{1}{C_s}\int i_s dt-(l_6+l_7+l_8)\frac{di_{D4}}{dt}$$

and $$V_{AK} = l_3\frac{di_s}{dt}+l_4\frac{di_s}{dt}+\frac{1}{C_s}\int i_s dt$$

Substituting $i_{D4} = i_T-i_s$

and $l_3+l_4+l_5+l_6+l_7+l_8= L_T$

$$E_d = L_T\frac{di_s}{dt}+\frac{1}{C_s}\int i_s dt$$

Solve above equation for i_s, then substituting

$$V_{AK} = E_d+\{\frac{1}{\omega C_s}-\omega(l_3+l_4)\}I_T\sin\omega t$$

where $\omega = \frac{1}{\sqrt{L_T C_s}}$

Thus the overshoot is given by

$$\Delta V = V_{AK}-E_d = \{\frac{1}{\omega C_s}-\omega(l_3+l_4)\}I_T$$

or $\Delta V \doteqdot \frac{I_T}{\omega C_s} = I_T\sqrt{\frac{L_T}{\omega C_s}}$

Thus the peaking voltage and overshoot can be calculated.

3. RECOMMENDATIONS:

At present CEERI POWER ELECTRONICS group is engaged in thyristor inverter mainly because of the availability of thyristors in India, under the present programme CEERI is developing AC motor drives for transportation applications. After discussions with the personnel of Power Electronics group, I observed that CEERI is planning for road vehicles operating from low input voltage and main line locomotives from high input voltage. In this regard I recommend Power transistors inverter for road vehicles and GTO inverter for main line traction. Unfortunately CEERI is unable to procure power transistor & GTO's in time which may hamper the progress of the project. Even though CEERI is trying their best to procure these devices I suggest that UNIDO should put special efforts to procure & supply power transistor, GTO's, GTO gate drive module, S.I. Thyristor and also S.I. transistor from Japan to CEERI for research and development work for the project of Electric vehicle

Regarding the measurements of accoustic noise, I suggest that this needs further investigation in following ways.

(a) Comparison of the noise by PWM input and sine wave input. This clearly shows the effect of harmonics on accoustic noise.

(b) Separation of the accoustic noise produced by:

a) induction motor.

b) inverter

c) environment

As the power electronics group of CEERI in having limited personnel this type of theor tical study needs extra personnel say one or two to strengthen the group.

Already CEERI designed and developed transistor inverter using 100 Amps transistor. I suggest that CEERI should put more efforts in developing GTO inverter.

In my view I feel that CEERI power electronics group is having plans for transportation similar to that of what Japan thought of in early eighties. As Japan has already done a lot of work in AC Motor drives for transportation it is advisable that CEERI Scientists of Power Electronics group should visit Japanese Universities and industries to get more practical knowledge about transportation equipment. As a first step Mr. U.M. Rao, CEERI who is going to university of Wiscosin in near future may have a stop over in Japan during his return journey for a short time. Mr.

U.M. Rao may send his exact programme so as to fix his visits in Japan. I also strongly recommend other engineers of CEERI for long time stay under exchange programme.

While working on GTO inverters, I suggest that CEERI should we readyly available gate drive circuits instead of developing than.

Finally I recommend the following equipment to entrance the facilities in power electronics lab of CEERI.

I also recommend to CSIR, Govt. Of India and other relevent bodies that it is worth thinking of having a collaboration project between CEERI, Meiji University and possibl with a Japanese industry on AC Motor drives which willplay a vital role in industry and transportation in near future.

Detailed discussions with CEERI, Scientist of power electronics group, I have, and the work on which CEERI power electronics group is engaged, I feel happy to visit CEERI in future for further collaboration.

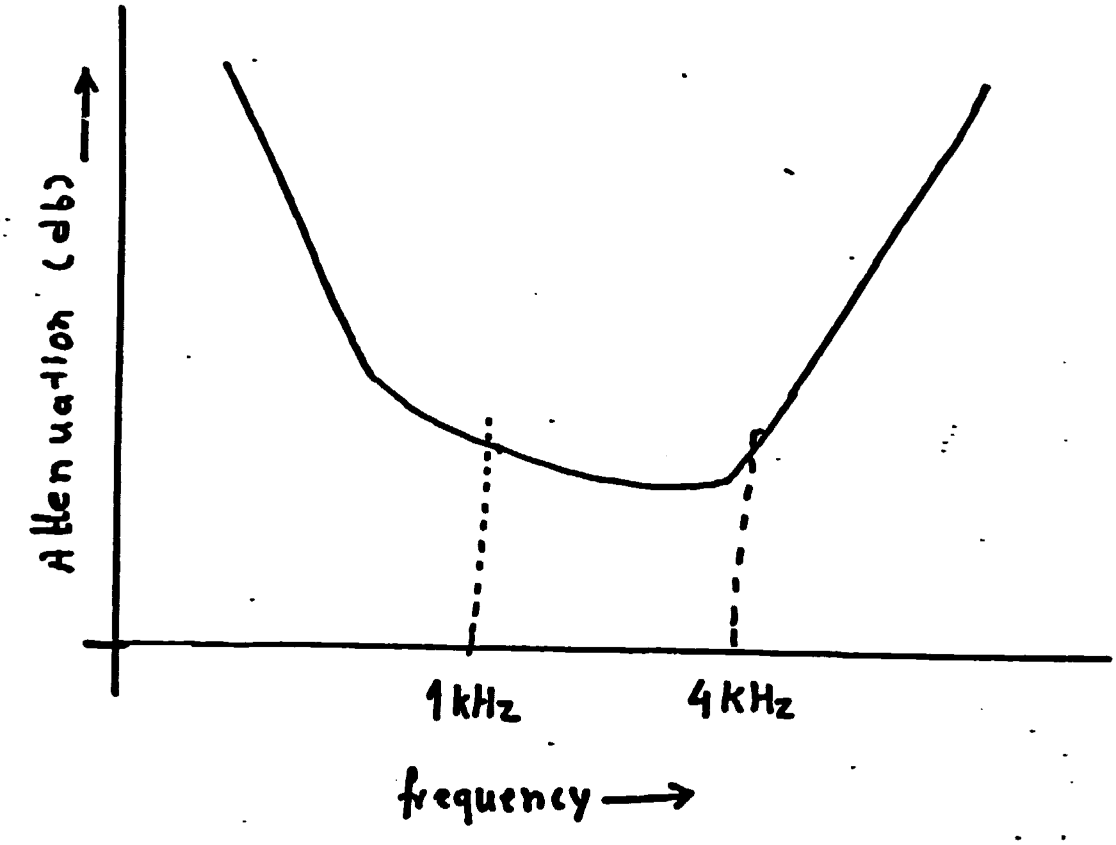

FIGURE 1

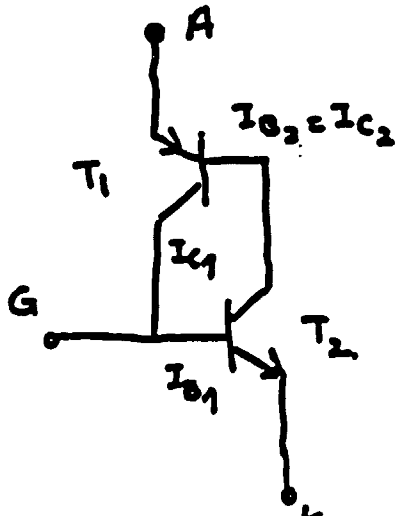

FIGURE 2

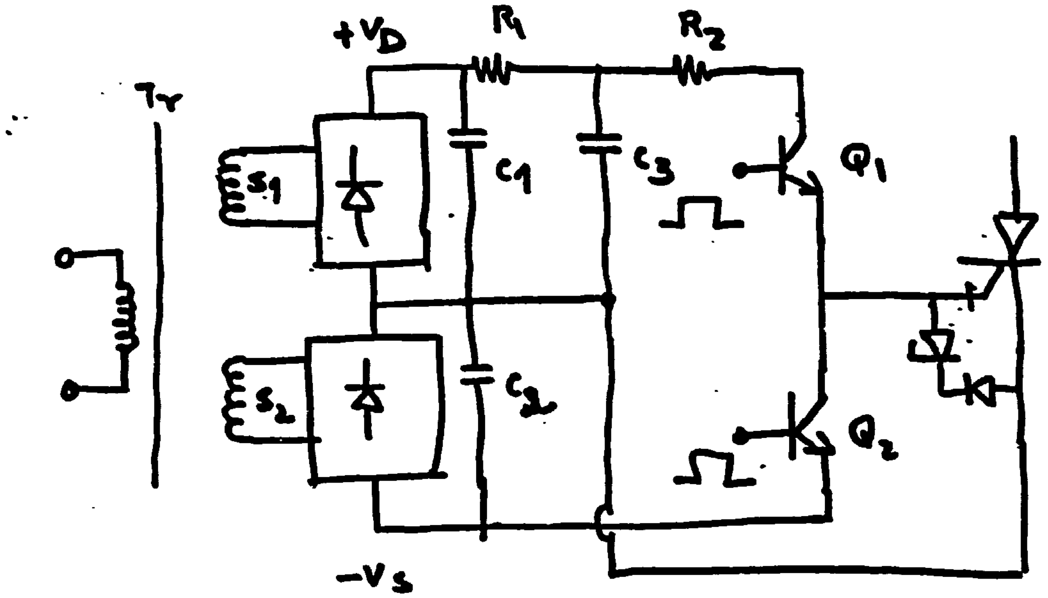

FIGURE 3

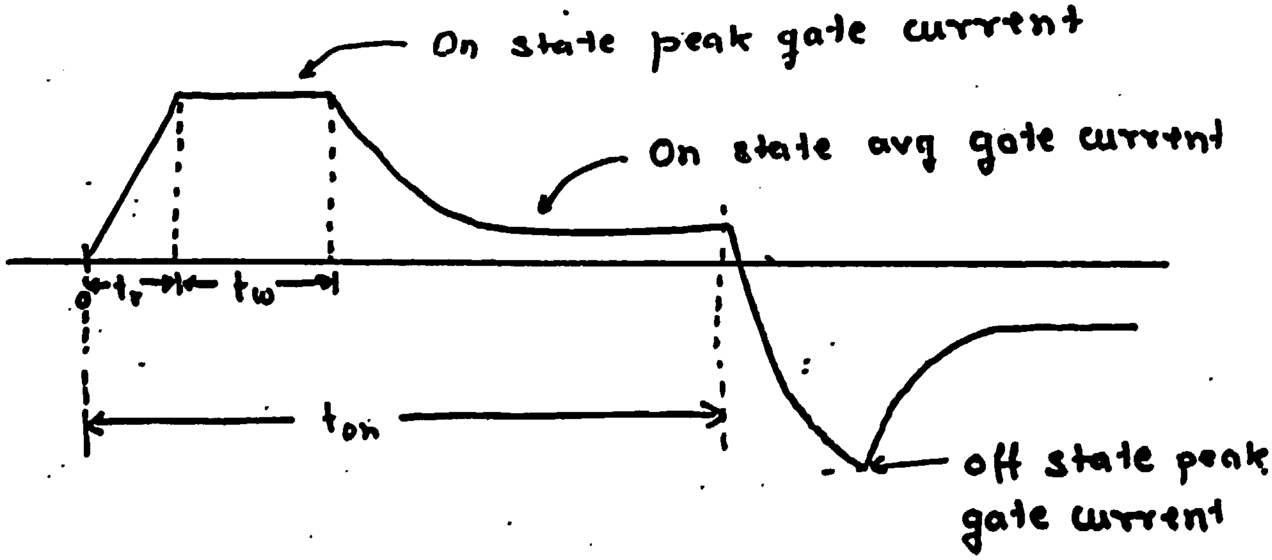

FIGURE 4

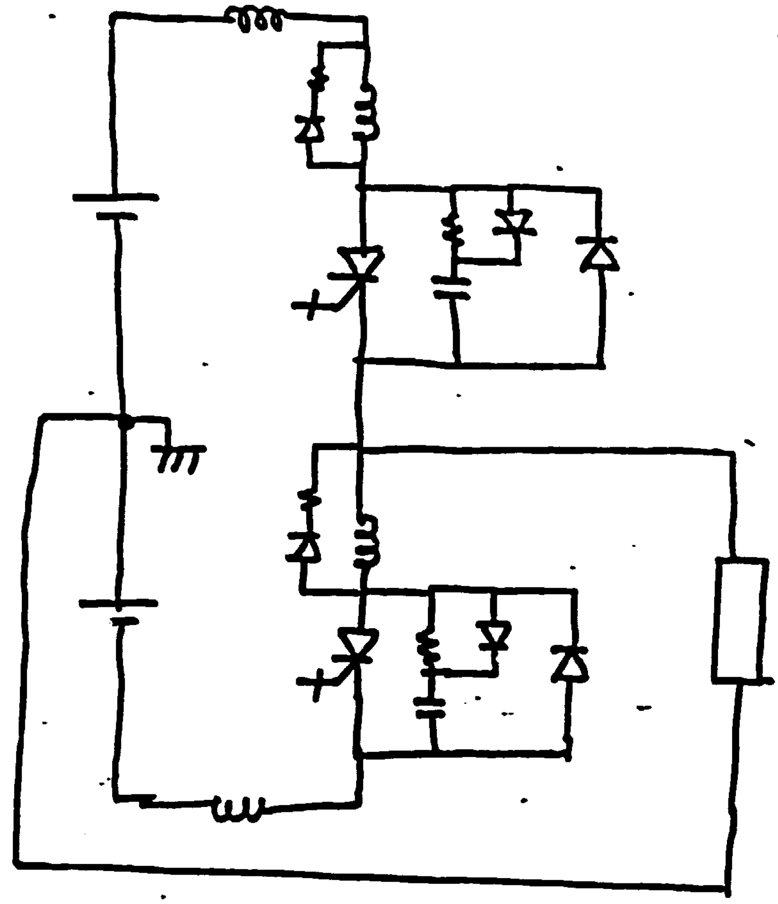

FIGURE 5

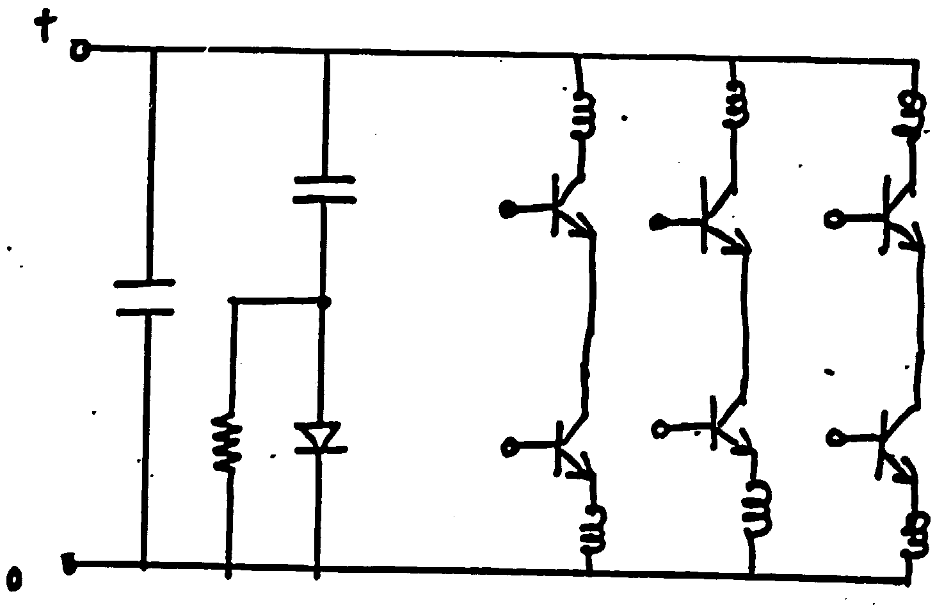

FIGURE 6 (a)

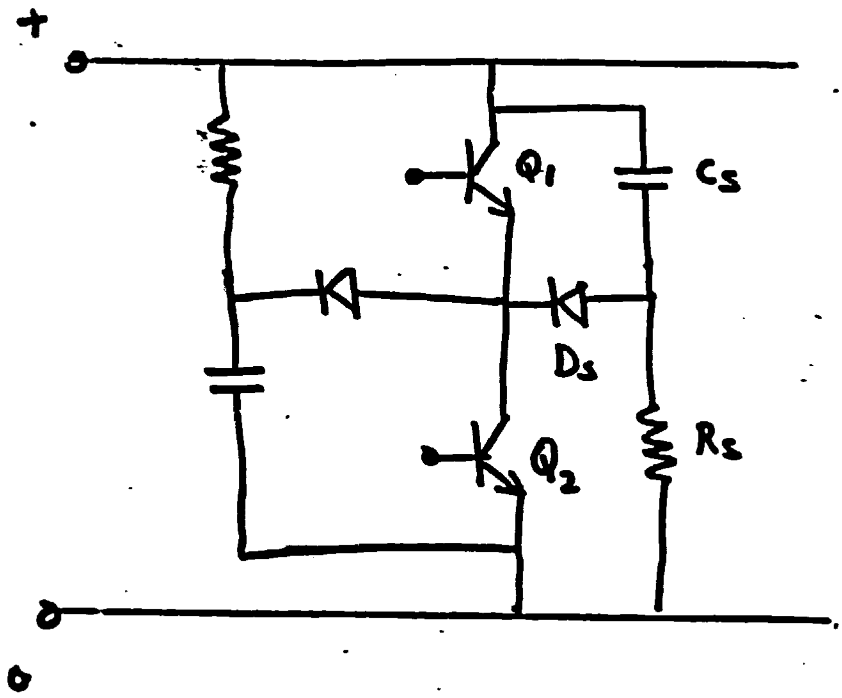

FIGURE 6(b)

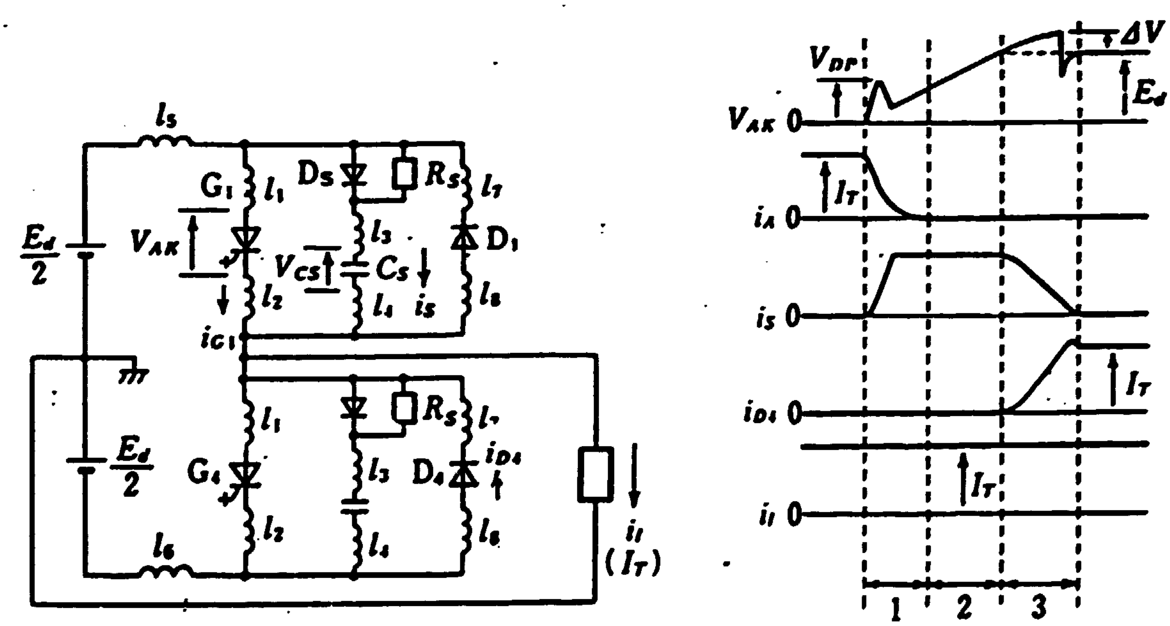

FIGURE 6(c)

4. **ACKNOWLEDGEMENT**

I would like to express my great appreciation to a number of persons for their kindly help during my stay in CEERI.

I wish to Express my great appreciation to Dr. G.N. Acharya, Director, CEERI. It was a great pleasure to meet with Dr. Hausila Singh, Mr. U.M. Rao, Mr. R.S. Mahajan, Mr. V.N. Walivadekar, Mr. S.D. Perlekar and Dr. U.S. Tandon.I also want to thank Mr. Samnol, Mr. P.K. Yadav for helping my official and technical work. My wife and myself are also thankful to Mr. Samnol and P.K. Yadav for other special arrangement.

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APPENDIX I

CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE
PILANI (RAJASTHAN) INDIA-333 031

A NOTE

ON

APPLICATION OF GTO, DESIGN CONSIDERATION FOR CIRCUIT AND APPLICATION OF GTO FOR AC TRACTION DRIVES

By

Prof. K. Matsuse (Meiji University, Japan)

UNDP Expert at CEERI

(March, 1987)

1. INTRODUCTION

The content of this lecture is as follows:

The first is "Gate Turn Off Thyristor" that includes principle of GTO operation, Ratings and characteristics of GTO.

The second is "Design consideration for circuit" that includes gate drive conditions and circuit, waveforms of gate current/voltage and anode current/voltage, gate drive circuit and snubber circuit. The third is "General Application of GTO" that includes GTO Converter, GTO inverter and Active filter. The final subject is "Application of GTO for AC traction drives" that is composed of Present status in the GTO Inverter - Fed AC traction system in our country and main subjects of GTO inverter, Induction motor and electromagnetic interference for traction.

2. Gate Turn Off Thyristor

2.1: Principle of GTO Thyristor

The basic principle of operation and construction of GTO thyristors are similar to those of ordinary reverse blocking three-terminal thyristors. However, the GTO is carefully devised to maximize its function of interrupting a load current by injecting a negative gate current.

Figure 7 shows a theoretical cross-section of a thyristor. The thyristor has a construction of four layers, P1, N1, P2 and N2. The layer P1 is formed into an anode electrode, the layer N2 into a cathode, and the layer P2 into a gate. This thyristor can be assumed as a combination of two transistors, as shown in figure.1

I wish to omit the illustration of turn-on operation.

In order to return the thyristor from on-state to off-state, a reverse bias may be applied for a certain time between anode and cathode, or the load current may be kept below the holding level. In order to apply a reverse bias between anode and cathode, an ordinary thyristor calls for a commulation circuit to sustain a flow of reverse current against the load current.

Figure 8 shows an off-operation model of the GTO thyristor. Assume that a positive bias is applied to the cathod and a negative bias is to the gate between gate G and cathode K, as illustrated.

At that time, a current flows from the gate to extract the stored carrier in the base region of the the N2-P2-N1 transistor and to apply a reverse bias to the N2-P2 junction. At the same time, the negative gate current causes the collector current Icl of the P1-N1-P2 transistor to reduce forward base current of N1-P2-N2 transistor because N2-P2 junction is reversed based. For this reason, the N2-P2-N1 transistor loses its base current and assumes an off-state.

On the other hand, the supply of base current to the P1-N1-P2 transistor is suspended because N2-P2-N1 trnaistor is in off-state and the collector current Ic1 stops also. Thus the GTO gains in blocking state.

The gate reverse current keeps flowing and then stops when the collector current of the P1-N1-P2 transistor is finished.

However, this current has to be maintained below a holding current. Otherwise, this current Ic1 becomes a base current of the N2-P2-N1 transistor, which can be a cause of retriggering. The turn off capability of the GTO by injecting negative base drive is described.

This capability is called the function of self-arc-extinction.

For the Power GTO´s the following characteristics are called for:

i) Controllable on-state current is large.
ii) Turn-off gain is large.
iii) Reverse gate voltage is high.
iv) ON-state voltage is low.
v) Gate trigger current is small.
vi) High reliability is assured.

2.2: Rating and Characteristics of GTO

I will show to you about operation, Ratings and characteristics of GTO Operation of the GTO should be observed in the following four periods:

(1) OFF State

(2) Turn-on process

(3) ON State

(4) Turn-on process

Characteristics and ratings in the above status are explained on the basis of the sample selected, for example.

Table 1 shows ratings characteristics regarding the off-status.

In these tables, the repetitive peak off-state voltage (1800 V) is a maximum voltage that can be applied in the forward direction under the condition that the GTO is off. The peak off-state current (400mA) is a maximum lelakage current carried at that time.

If a steep change occurs in the applied voltage, the GTO cannot maintain the off-state unless the rate of change of the applied voltage is limited below the critical off-state voltage rise rate (1000 V/μs). In addition, it is necessary to keep the reverse gate voltage (V/μs) applied between gate and cathode, in order to maintain the off-state.

On the other hand, the repetitive peak reverse voltage (200V) is a maximum voltage that can be applied in the reverse direction. The peak off-state reverse current (40 mA) is a maximum leakage current carried at tha time.

Table 2 show ratings and characteristics concerned with the turn-on process.

In order to get the GTO turned on, it is necessary to feed a turn-on (forward) current to the gate. The peak gate current (50A) is a maximum value of gate current which can be led without damaging the GTO at that time.

If repetitive turn-on operation is intended, it is necessary to suppress the average value of this gate on-state current below the average on-state gate current (4A)

When intending to avoid unusal temperature rise during turn-on operation, it is necessary to suppress the rise of anode current in turn-on mode below the crictical on-state current rise rate (200 A/μs).

The permissible loss generated in the gate area due to this gate current is indicated by the average gate on-state power (20W). The time required for turn-on operation is called the turn-on time (6μs) and it is specified in the table of characteristics.

Table 3 show ratings and characteristics concerned with the on-state.

The RMS on-state current (200 A) is a maximum rms (effective) value of a current that can be led through the GTO. The non-repetitive surge on-state current (6000A) is an overcurrent which can be led in unusal case such as load short-circuiting.

The peak on-state voltage (2.3V) is a terminal voltage of GTO appearing when the on-state current is carried. This value is specified at GTO's rated controllable on-state current.

Table 4 show ratings and characteristics concerned with the turn-off process.

In these tables, controllable on-state current (400A) is a maximum anode current that can be turned off by applying negative gate current, while the time requirement for turn-off operation is specified by the turn-off time (5 µs).

In order to get the GTO turned off, it is necessary to take out the current from gate by applying maximum permissible reverse voltage across gate and cathode as indicated by the reverse gate voltage (50V).

The GTO may be damaged unless the maximum value of the above mentioned current is kept below the peak gate turn-off current (220A). When this current flows inside the GTO, there arises a voltage drop which is indicated by the reverse gate voltage drop (35V).

When turn-off operation is over, a surge voltages is generated by the effect of wiring inductance in the gate circuit. This surge voltage should be absorbed otherwise gate-cathode junction may be damaged.

Therefore, this value has to be suppressed below the value indicated by the peak reverse gate voltage (130V) by minimising stray wiring inductances.

Table 5 shows the main ratings and characteristics of very big GTO's which are available at present. The GTO which is ratings of VDRM/4500V and ITGQ 2000A has a maximum ON state voltage drop 3.5V with turn off time 10 µ sec.

3. Design Consideration for Circuit

3.1: Gate Drive Conditions

To make full use of the GTO functions, the gate conditions are the most essential factors. Figure 9 shows an example of gate waveform which assures exact on-off operation of the GTO. Let me express the gate current required in each mode shown in this figure in more details. At first, turn-on period (Mode A) is the one in which the GTO moves from off-state to on-state by the effect of gate current and the load current carrying area is going to be expanded from a narrow area to the overall area of junction. Therefore, current density is very large in the initial state and a local temperature rise occurs.

The greater the gate current, the wider the initial conductive area and lower the local temperature rise. In general, it is necessary to lead through the gate a current which is roughly 10 to 30 times the gate trigger current specified in catalog.

I will express about the second period that is on-state period (Mode B). As I already shown you, the GTO is just the same as a conventional thyristor so far as it assumes a turn-on state. Therefore, the GTO will be turned off if the anode current is below the holding current and there is no gate current if there is a lagging load like a motor control inverter.

I will show about during the third and fourth periods, turn-off periods (Mode C and D). Since the GTO makes itself turned off by leading an off-gate current, insufficient off-gate current (IGQ) or a small gradient of that current (digr/dt) will result in extension of turn-off time, thus causing internal destruction of the device due to failure in interruption of current.

The maximum value (IGQK) of off-gate current has to be arranged in a circuit configuration where it can be more than the crest value determined by the following expressions:

IGQK is equal to or is larger than controllable on-state current (ITGQM) divided by off-gain (G).

The off gain (G) usually lies between 3 and 4. In the section of Mode D for the turn-off process, this period (C+D) is a time necessry for the recovery of the off-state blocking capability through the elimination of carriers of positive holes and electrons accumulated in the base layer.

I will show about during the fifth period, off period (Mode E). When the off-gate current stops flowing and the turn-off time has expired, the GTO recovers its blocking capability. However, since the GTO is not provided with a cathode-emitter shorting construction like a conventional thyristor, the gate must be applied with reverse voltage to hold the rated blocking voltage.

This voltage can differ according to the device construction. It is generally maintained above 10 volts.

In this state, false turn-on cannot occur even though a steep rising voltage (dv/dt) should have been applied, provided that this voltage is below the permissible level.

3.2: Gate Drive Circuit

I will show to you about gate drive circuit for getting the above mentioned gate current waveforms.

The gate drive current is composed of two parts: a turn-on gate drive current, and a turn-off gate drive current. The turn-on gate drive current also has two parts; a short time pulse, and a long time pulse.

Figure 10 shows the gate drive circuit for getting the this requirements.

At first, when transistor Q1 is turned on, the charge stored in capacitor C3 discharges through Resistor R2, Q1 and G generating the first short time high aplitute current pulse. After this period, a long time pulse current flows through Resistors R1 and R2, Q1 and G. At the turn-off, we use the transistor Q2.

In this figure, we have the two parts turn-on circuit and turn-off circuit.

The second gate drive circuit is shown in figure-11

In this figure, we also have the two parts, but which composed of a long time pulse circuit and a short time pulse circuit.

The generation of surge voltage during turn off demands a low leakage inductance type pulse transformer and also we should be to reduce the inductance including the turn-off circuit.

3.3: Snubber Circuit and di/dt limiting chock

I will show you about the snubber circuit. At first, I will express about why we require the snubber circuit in parallel with GTO, and the di/dt limiting choke in series with GTO.

Figure 12 shows the waveforms of the anode current and the anode voltage of the GTO. In this figure, the solid lines indicated the voltage and current with di/dt choke and dv/dt snubber circuit. The dotted lines indicated the s same without di/dt and dv/dt ckt. As you can see if you do not have the di/dt limit choke, the increasing rate of the anode current becomes greater and then the switching loss grows up in the turn-on period, which may result in internal destruction of the device.

The snubber circuit is used to relieve the voltage duty when the GTO has been turned off. When the GTO is turned off, a spike voltage is generated as shown in this figure by dotted lines.

Figure 6(c) shows the circuit of one phase of the GTO inverter and waveforms of current and voltage in this circuit. In this circuit, $\ell 1$ to $\ell 8$ shows the wiring inductance in parts of this circuit.

I will show to you how to calculate the spike voltage VDP and the overcharged voltage . We can divide the operation in the three mode the comulation period from the GTO1 to free wheel diode D4.

In this case, we give an off-trigger signal to G1 but the load current continues to flow because of lagging load.

In the mode 1, the snubber diode, Ds, conducts at first. So, the load current flows through G1 and the capacitor Cs and diode Ds. In this period, we get the voltage equation, this one. Therefore, we can obtain, the equation for spike voltage (VDP). As you can see, we should decrease the inductances $\ell 1$ to $\ell 4$ for reducing the spike voltage. At the end of this mode, the anode current of the GTO goes out.

Next, in mode 2, the snubber current is constant. At the end of this mode, the voltage VAK has reached to the value Ed.

In the mode 3, diode D4 conducts the current because the snubber capacitor is overcharged by the snubber current. While the diode D4 conducts, the overshort capcitor voltage is applied across G1. At the end of this internal, the current into the snubber capacitor goes out and the load current flow through the diode D4 only. At the end of this made, we calculate to the incrimental voltage ΔV of the GTO, that is equal to VAK nimus Ed. In this mode, we obtain the equation.

Finally, we get the relation between the overcharged voltage ΔV and capacitor Cs.

4. General Application of GTO

4.1: GTO Converter

Fig. 13 shows the circuit for PWM controlled converter. It is a very important problem how to treat the energy stored in the leakage inductance of source line. Several different circuit of GTO converter have been proposed.

I will talk about number (c) circuit in more details.

Figure 13 (c) shows the main circuit of the GTO converter. The circuit is composed of two main parts: One is a new auxiliary circuit which includes an auxiliary capacitor C and the other is the GTO controlled rectifier.

Now, the new auxiliary circuit is developed to treat the commulating energy generated in the ac source leakage reactance during circuit commulation.

The Comulating energy is stored temporarily in this auxiliary capacitor and then discharged to the dc load side in a pulse after each complete commulation. Futhermore, the auxiliary capacitor connected in this position also helps to limit the voltage spikes to the same voltage level Ecd.

On the other hand, the GTO controlled rectifier is operative in PWM mode so that PWM waveforms of line input currents and controllable dc output voltage are obtained.

4.2: GTO Inverter

Figure 14 shows the main circuit of voltage source GTO inverter for the general purpose application. In this circuit, we get the senusoidal current by PWM controlled converter with the adjustable power factor of source line.

Figure 15 shows the main circuit of current source GTO inverter.

Figure 16 also shows the main circuit of other current source GTO inverter.

Figure 17 shows the other main circuit of current source GTO inverter.

These three types of current source GTO inverter differ the main circuit from each other depending on the treatment in the load-inductance.

4.3: Active Filter

Figure 18 shows the principle of Active Filter. As shown in this figure, without being limited to special harmonics only, suppression of harmonics of any order is possible with the use of PWM circuit.

Major generl Application of GTO's are:

(1) VVVF Power Supply
(2) UPS
(3) ACTIVE FILTER
(4) GTO Circuit Breaker.

5. APPLICATION OF GTO FOR AC TRACTION DRIVES

5.1: Present status in the AC Traction System in Japan

Table 6 shows the state of ac drive system applications to electric car, not electric locomotive, in our country. The beginning of the practical application was to apply the street electric car in local big town in 1982.

At present, the total number of electric car of ac drive system is equal to 110 cars including bogies. The type of inverter is the PWM controlled voltage source inverter, and in general an individual inverter unit is provided for one, two in general an individual inverter unit is provided for one, two or four tractive machines i.e. induction motor in one car.

In the Japanees National Railways, the AC drive system entered the stage of practical application in last year. I attended the practical experiement in the normal lines in the month of January, 1987.

The AC system was 207 type of ten bogie. This photo 1 show the front view of the electric car.

For example, I will show you the power circuit schematic diagram of AC traction drives in figure 19.

In this system, 4 induction motors are provided in motor coach, and a one-unit of voltage source PWM inverter drives a total of 8 machines driving motor coaches. A filter leactor and a filter capacitor are provided at the trolley line side of the power unit, which function to prevent a higher harmonic current generating the ivnerter circuit flowing out to the trolley line side. This equipment suppresses the electromagnetic interference by means of the shorter wiring between the ivnerter and filter capacitor and using a luminum shilding of inverter equipment.

Let me show the specification of this system in table 7.

5.2: Relation among Ratings of GTO, Inverter and Motor

Finally, table 8 shows the relation among the ratings of GTO, inverter and motor. As you can see, the ratings VDRM, ITRMS, ITGQM and tgq of GTO are related to the rating of voltage, current and frequency of inverter, and the ratings of voltage, current, and speed of motor.

Therefore, it is very important problem that the ratings of VDRM, ITRMS, ITGQM and tgq of GTO is developed.

6.0 CONCLUSION

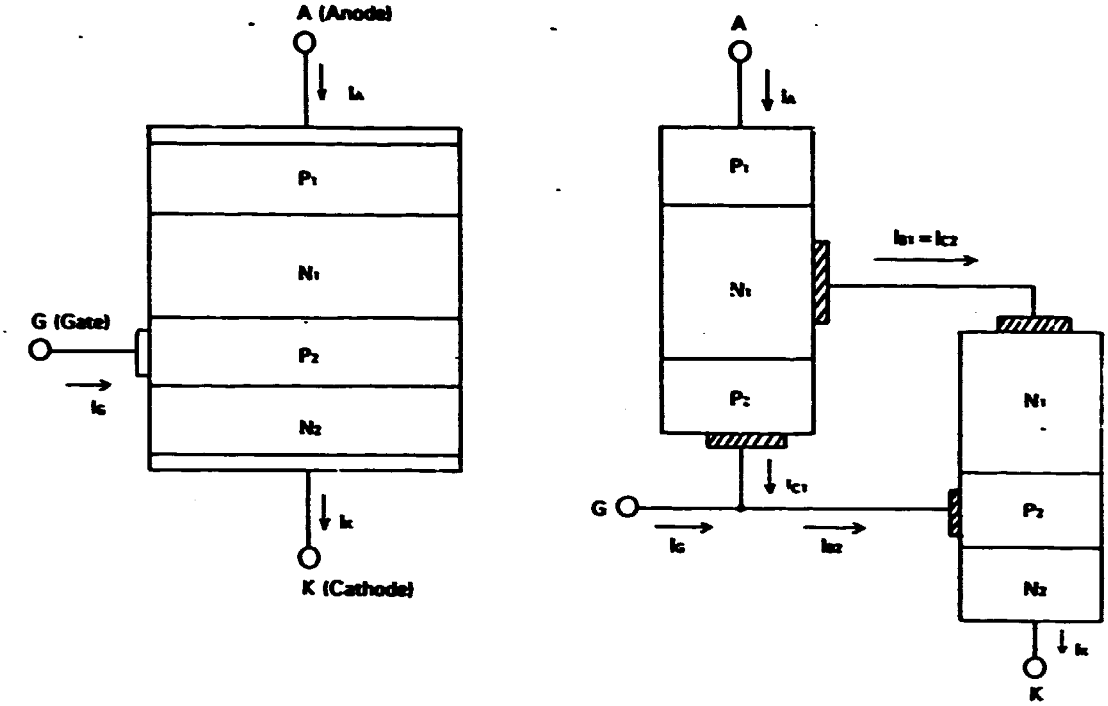
In this lecture, I told to you about Gate turn-off thyristor, at first subject, secondly, design consideration for circuit, at third subject, general application of GTO, and, finaly Application of GTO for AC Traction drives.

I wish to express my great appreciation to Dr. Acharya, Director and I wish you all good luck for CEERI

I want to come here once again if it is possible for me.

Thank you for your kind attention.

BAHUT DHANYABAD



Cross-Section of Thyristor

Transistor Model

FIGURE 7

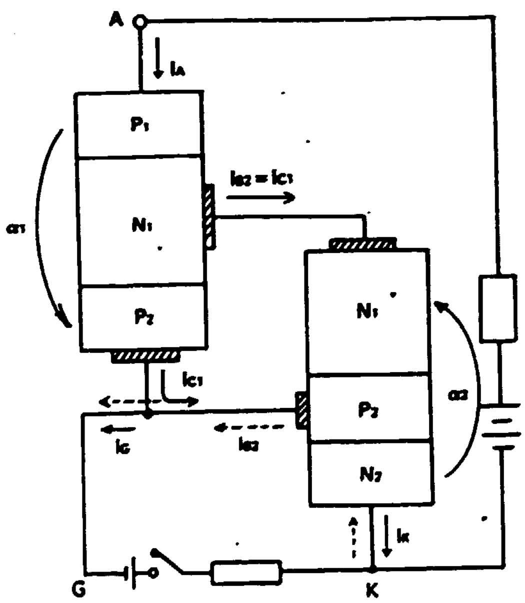


FIGURE 8 OFF-Operation Model

TABLE 1 Ratings and characteristics regarding the off status

Ratings

Item	Symbol	Ratings	Unit	Conditions
Repetitive peak off-state voltage	V_{DRM}	1800	V	V_{GR} :15V
Repetitive peak reverse voltage	V_{RRM}	200	V	V_{GR} :15V

Characteristics

Item	Symbol	Conditions	Min.	Standard	Max.	Unit
Peak off-state current	I_{DRM}	$T_j = T_{jmax}$ $V_D = V_{DRM}$			40	mA
Peak off-state reverse current	I_{RRM}	$T_j = T_{jmax}$ $V_R = V_{RRM}$			40	mA
Critical off-state voltage rise rate	dv/dt	$T_j = T_{jmax}$ $V_D = 2/3\ V_{DRM}$ $V_{GR} = 15V$	1000			V/μs

TABLE 2 Ratings and characteristics concerned with the turn-on process

Ratings:

Item	Symbol	Ratings	Unit	Conditions
Critical on-state current rise rate	di/dt	200	A/μs	$I_T = I_{TGQ}$, $V_D = 1/2 V_{DRM}$ $I_{GF} \geqq 5A$, $I_{GM} \geqq 15A$
Peak gate current	I_{FGM}	50	A	$t_w \leqq 100\mu s$
Average gate on-state current	$I_{FG(AV)}$	4	A	

Characteristics:

Item	Symbol	Conditions	Min.	Standard	Max.	Unit
Turn-on time (delay time)	t_{gt} t_d	$V_D = 1/2 V_{DRM}$ $I_{TM} = I_{TGQ}$		 3	6 	μs μs

TABLE 3 **Ratings and characteristics concerned with the on-state**

Ratings:

Item	Symbol	Ratings	Unit	Conditions
RMS on-state current	$I_{T(RMS)}$	200	A	$T_c = 80°C$
Non-repetitive surge on-state current	I_{TSM}	6000	A	Half sine wave 1 cycle (50Hz)
I^2t limit value	I^2t	160000	A^2S	1ms – 10ms

Characteristics:

Item	Symbol	Conditions	Min.	Standard	Max.	Unit
Peak on-state voltage	V_{TM}	$T_j = T_{jmax}$ $I_{TM} = I_{TGQM}$			2.3	V

TABLE 4 **Ratings and characteristics concerned with the turn-off process**

Ratings:

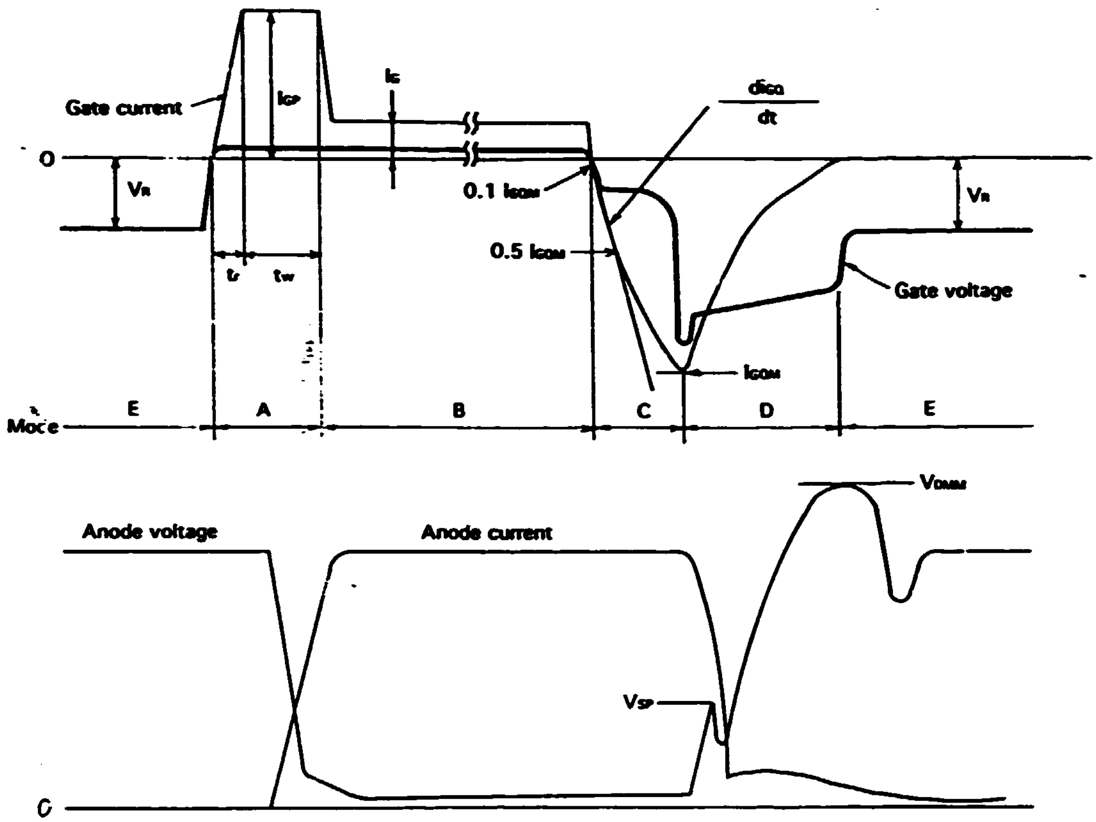
Item	Symbol	Rating	Unit	Conditions
Peak reverse gate voltage	V_{GRM}	130	V	
Reverse gate voltage	V_{GR}	50	V	
Controllable on-state current	I_{TGQM}	400	A	$C_s = 1\mu F$, $V_s \leqq 400V$ $d\,i_{GQ}/d\,t \geqq 100A/\mu s$
Peak gate turn-off current	I_{GQM}	220	A	
Reverse gate energy	E_{RG}	10	Ws	
Average gate reverse loss	$P_{RG(AV)}$	10	W	

Characteristics:

Item	Symbol	Conditions	Min.	Standard	Max.	Unit
Reverse gate voltage drop	V_{GRO}				35	V
Gate turn-off time (storage time)	t_{gq} t_s	$I_{TGQ} = 400A$ $V_D = 1200V$		 4	5	μs μs

Table 5 Main ratings and characteristics of very big GTO

	A	B	C	D	E	F
Repetitive Peak Off-state Voltage VDRM	2500 A	2500	2500	4500	4500	4500
Controllable On-state Current ITGQ	1800 A	2000	2000	2000	2500	3000
RMS On-state Current IT	860 A	700	800	940	800	1000
Peak On-state Voltage VTM	3.0 V	2.8	2.5	3.5	3.5	3.5
Critical On-state Current Rise Time DI/DT	300 A/µsec	300	450	300	300	300
Non-repetitive Surge On-State Current ITSM	11000 A	14000	11000	13000	16000	16000
Turn-On Time TGT	10 µsec	15	10	10	15	10



Waveforms of Gate Current/Voltage and Anode Voltage/Current

Recommended Values of Gate Waveform for the

$I_{GP} = 3A$	$I_G = 1A$
$t_r = 1\mu s$	$di_{GQ}/dt = 100A/\mu s$
$t_w = 6\mu s$	$V_R = 15V$
$t_{gt} = 7\mu s$	

FIGURE 9

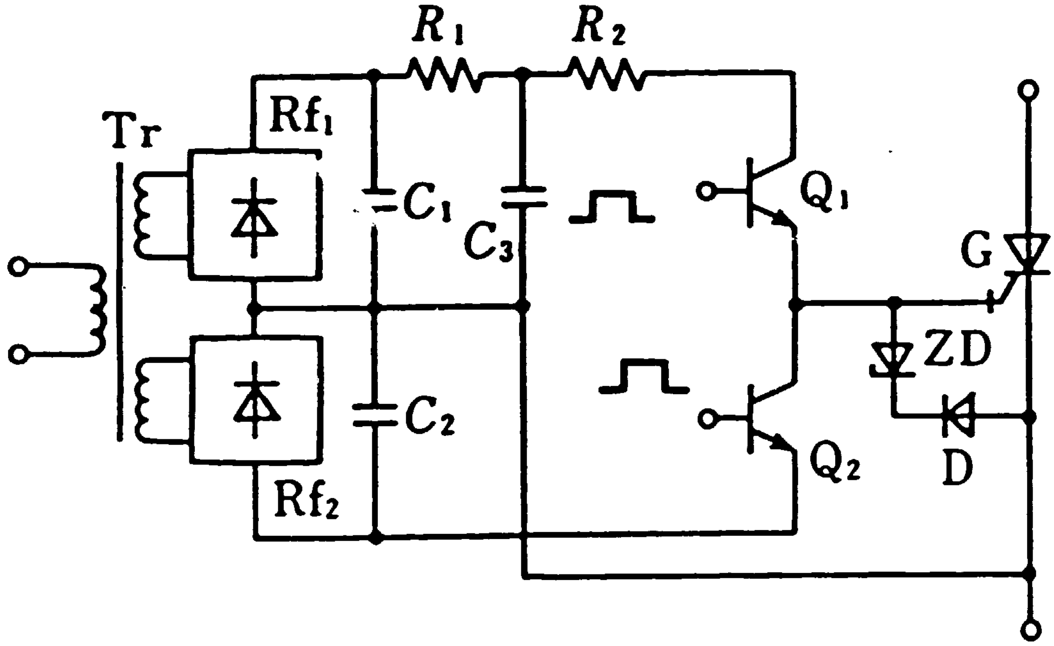
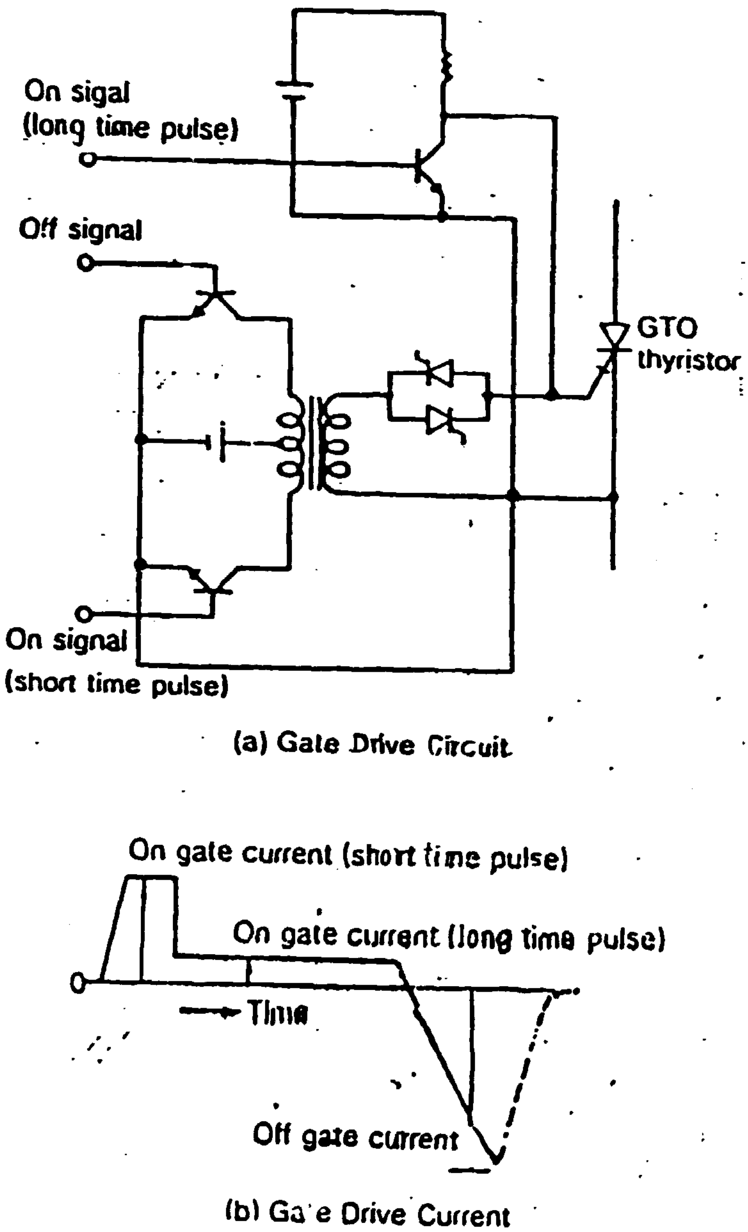


FIGURE 10



(a) Gate Drive Circuit

(b) Gate Drive Current

FIGURE 11 Gate Drive Circuit and Gate Drive Current

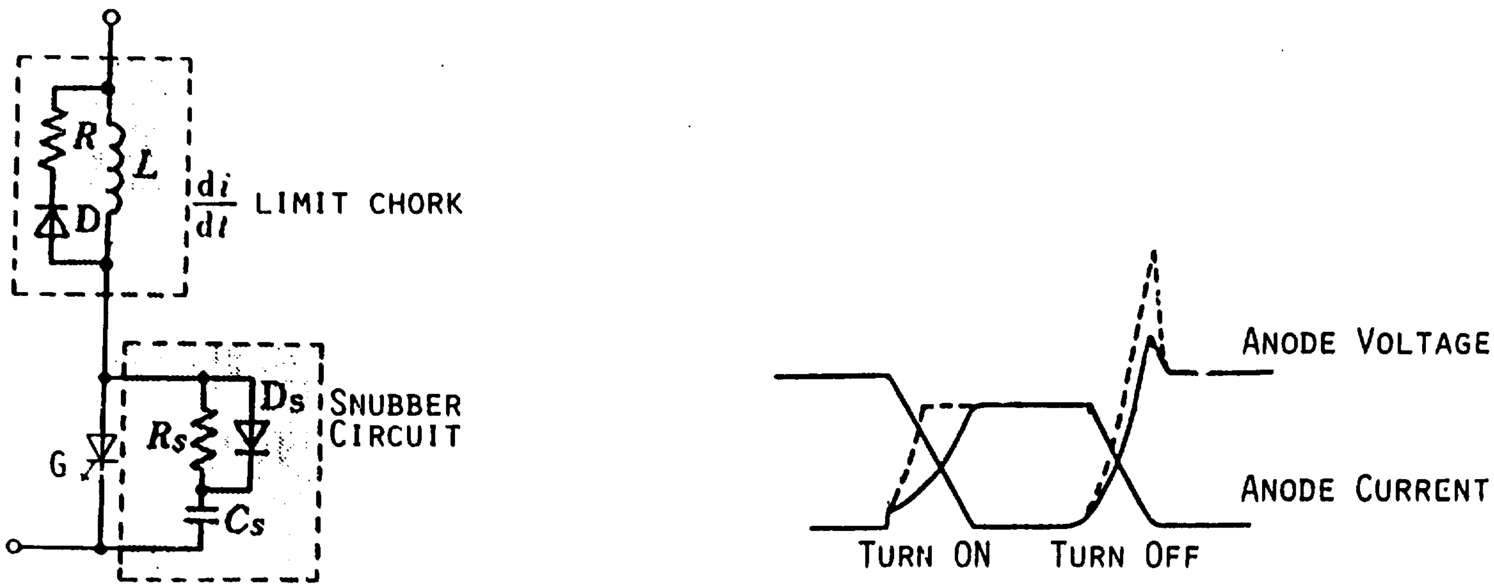

R
L
D
$\frac{di}{dt}$ LIMIT CHORK
G
Ds
Rs
Cs
SNUBBER
CIRCUIT
ANODE VOLTAGE
ANODE CURRENT
TURN ON
TURN OFF

FIGURE 12

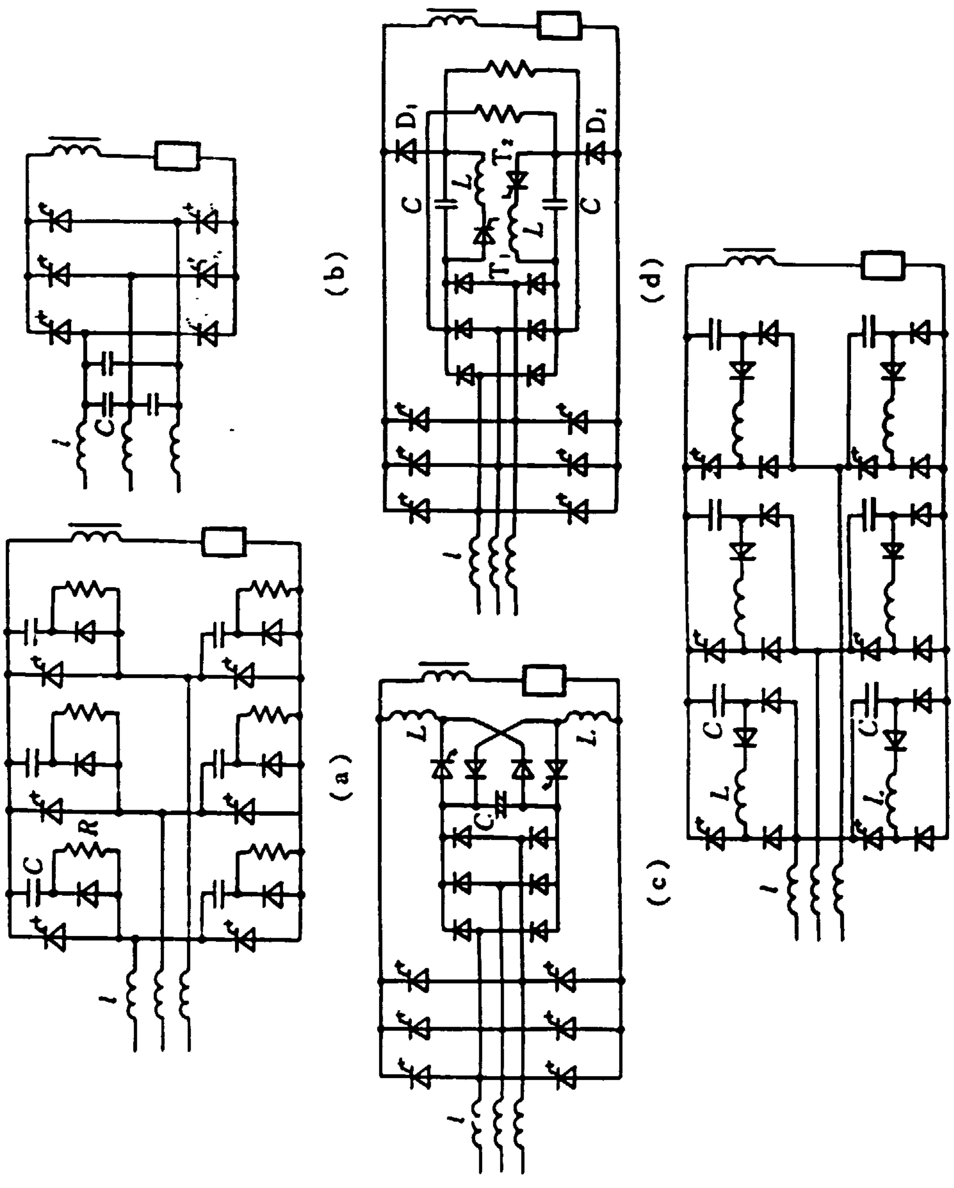


FIGURE 13

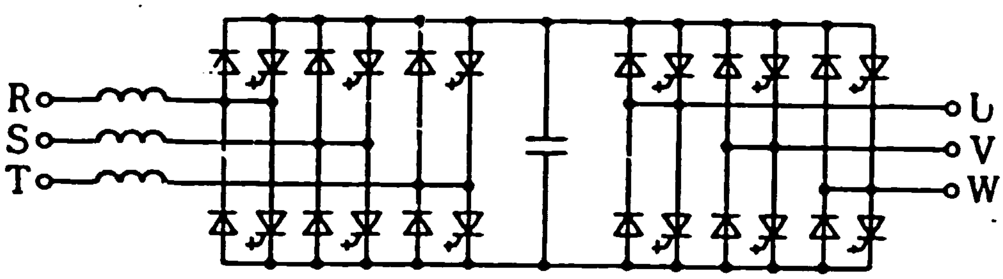


FIGURE 14

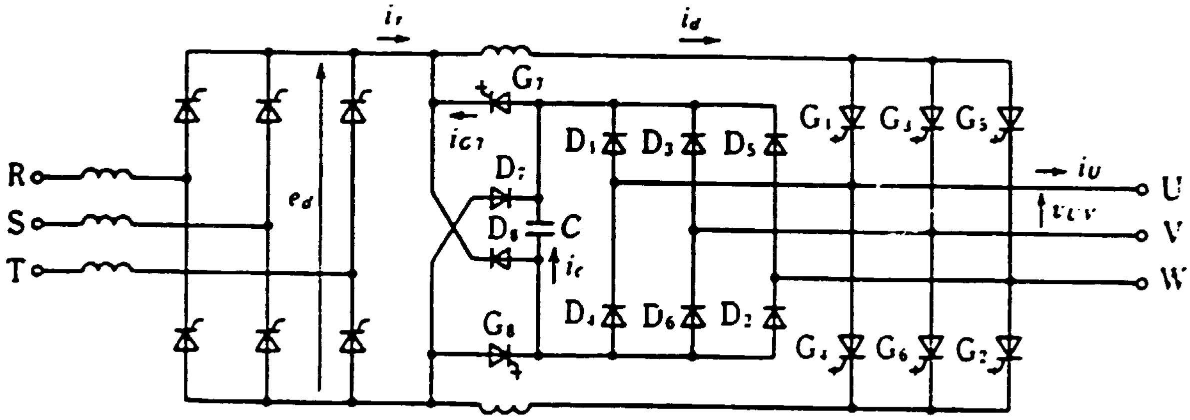


FIGURE 15

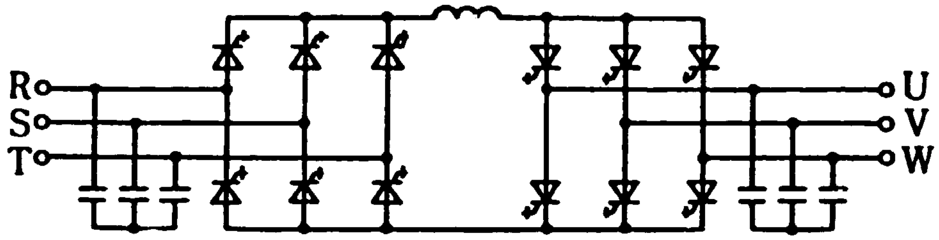


FIGURE 16

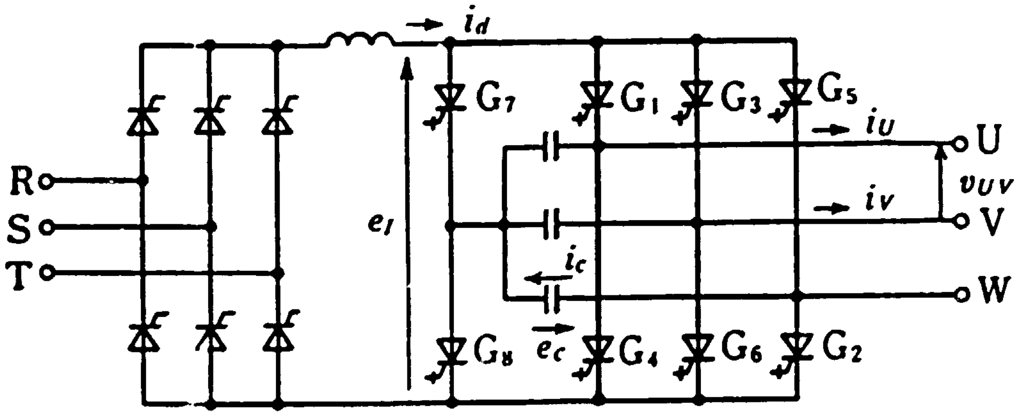
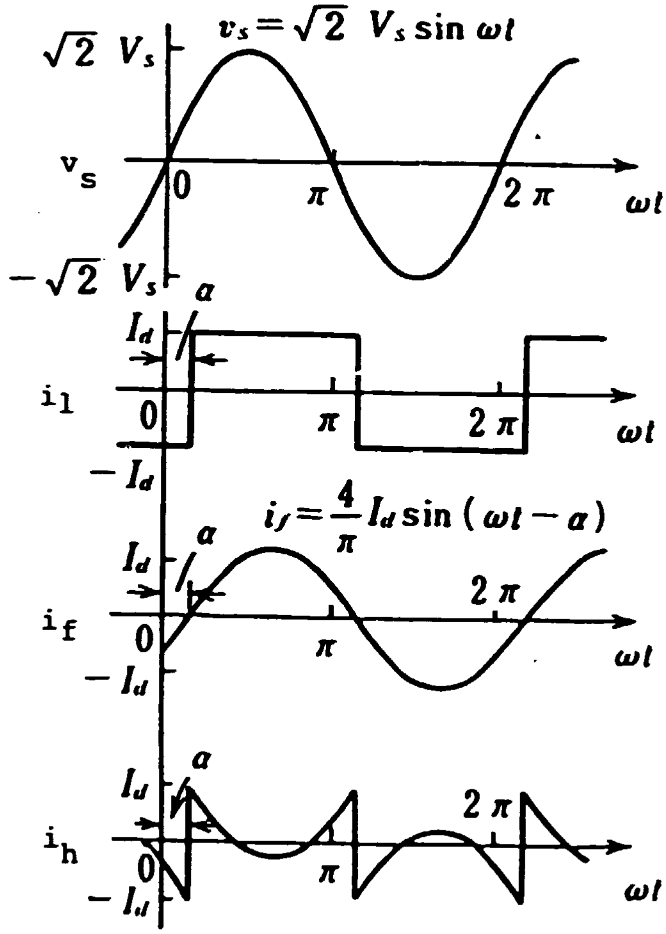
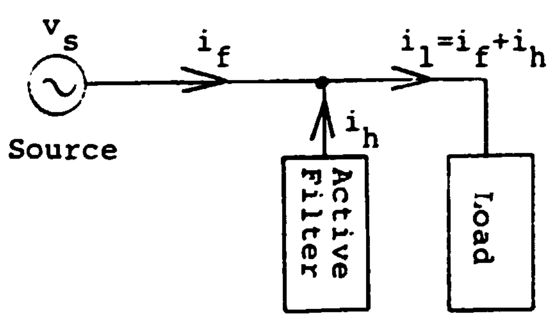


FIGURE 17



$v_s = \sqrt{2}\ V_s \sin \omega t$
$\sqrt{2}\ V_s$
v_s
0
π
2π
ωt
$-\sqrt{2}\ V_s$
α
I_d
i_l
$-I_d$
$i_f = \frac{4}{\pi} I_d \sin(\omega t - \alpha)$
i_f
i_h



v_s
i_f
$i_l = i_f + i_h$
i_h
Source
Active Filter
Load

FIGURE 18

TABLE 6 The state of ac drive system applications to electric car in Japan

Railway & Type			Number of Car	Power Source	Device and Composition	Mortor	Start of service running
KUMAMOTO.M.T.B.	8200		2	DC 600V	RCT 2500V,1000A 1S1P6A	120kw×1	1982.8.2
TOKYU	6200	*	1	DC1500V	GTO 2500V,2000A 2S1P6A	165kw×4	1984.7.25
KINTETUS	1250		2	DC1500V	GTO 4500V,2000A 1S1P6A	165kw×4	1984.10.31
OSAKA	20		30	DC 750V	GTO 2500V,2000A 1S1P6A	140kw×4	1984.12.24
SEIBU	8500		12	DC 750V	GTO 2500V,1000A 2S1P6A	95kw×1	1985.4.25
TOKYU	6300	*	1	DC1500V	GTO 2500V,1600A 2S1P6A	160kw×4	1985.4.30
TOKYU	6000	*	1	DC1500V	GTO 2500V,2000A 2S1P6A	165kw×4	1985.4.30
SAPPORO.M.T.B.	8500		2	DC 600V	RCT 2500V,1000A 1S1P6A	60kw×2	1985.5.13
HANKYU	2720		2	DC1500V	GTO 4500V,2400A 1S1P6A	150kw×4	1985.7.17
SHINKEISEI	8800		8	DC1500V	GTO 4500V,2000A 1S1P6A	135kw×4	1986.2.26
KINTETUS	3200		12	DC1500V	GTO 4500V,2000A 1S1P6A	165kw×4	1986.3.1
TOKYU	9000		8	DC1500V	GTO 4500V,2000A 1S1P6A	170kw×4	1986.3.9
ODAKYU	2650	*	1	DC1500V	GTO 4500V,2000A 1S1P6A	175kw×4	1986.3.17
KINTETUS	6400		4	DC1500V	GTO 4500V,2000A 1S1P6A	155kw×4	1986.6.10
TOKYU	7600	*	6	DC1500V	GTO 4500V,2000A 1S1P6A	110kw×8	1986.5
KITAOSAKAKYUKO	8000		8	DC 750V	GTO 2500V,2000A 1S2P6A	140kw×4	1986.
J.N.R.	207		10	DC1500V	GTO 4500V,2000A 1S1P6A	150kw×4	1987.2

* ---remodeling

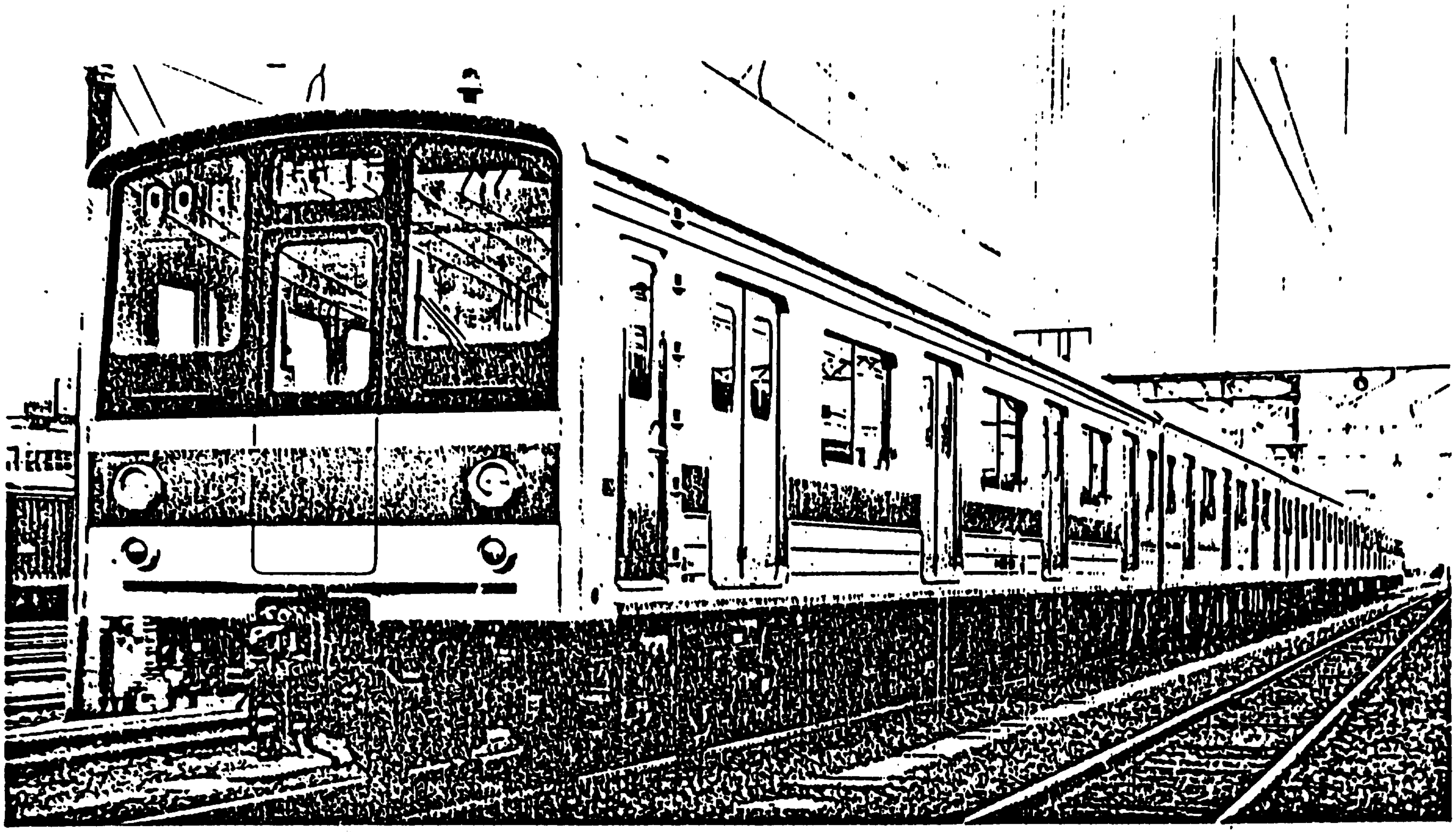
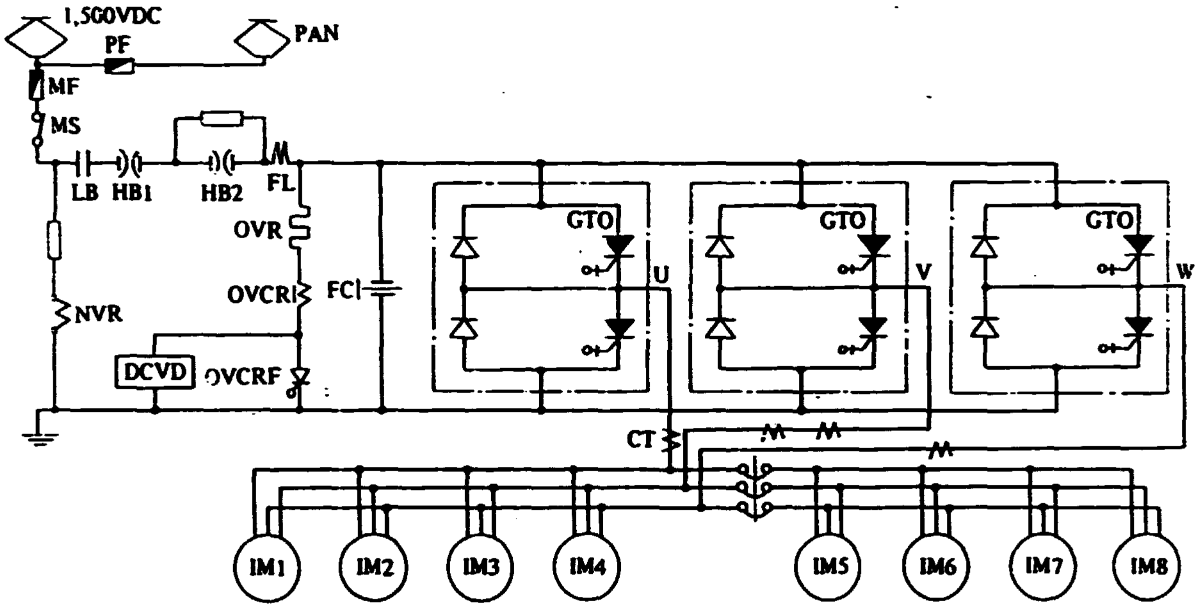


PHOTO 1 J.N.R. 207 TYPE



PAN : Pantograph
PF : Pantograph fuse
MF : Main fuse
MS : Main switch
HB : High speed circuit breaker
FC : Filter capacitor
FL : Filter reactor
NVR : No-voltage relay
DCVD : DC voltage transducer
OVR : Over voltage relay
OVCR : Current relay
OVCRF : Over voltage thyristor
CT : Current transducer
IM : Induction motor

FIGURE 19 Power circuit schematic diagram

TABLE 7 Specification of AC Propulsion System

Electric system	DC 1,500V (900-1,850V)
Train formation	4-motor coaches 2-trailler coaches
Maximum speed	100 km/h
Acceleration	α= 3.2 km/h/s (0.89 m/s/s)
Deceleration	β= 3.5 km/h/s (0.97 m/s/s)
Wheel diameter	860 - 780 mm
Gear ratio	14:85 = 1:6.07
Traction motor	3-phase 4-pole cage type induction motor
One hour rating	110kW 1,130V 73A ,1,180rpm
Type of inverter	3-phase GTO PWM inverter
Output frequency	3 Hz - 150 Hz
Cooling	Freon evaporation cooling (submerged system)
Rating of GTO	4,500V, 2,500A/800A(r.m.s.)

TABLE 8 · RELATION AMONG RATINGS OF GTO, INVERTER AND MOTOR

RATINGS

GTO | INVERTER | MOTOR

REPETITIVE PEAK OFF-STATE VOLTAGE VDRM —— INPUT VOLTAGE

OUTPUT VOLTAGE $\fallingdotseq \frac{\sqrt{6}}{\pi}$ INPUT VOLTAGE —— RATING VOLTAGE

RMS ON-STATE CURRENT IT(RMS) —— OUTPUT CURRENT —— RATING CURRENT

MAXIMUM OUTPUT CURRENT —— MAXIMUM CURRENT

CONTROLLABLE ON-STATE CURRENT ITGQM —— MAXIMUM SUSPENDED CURRENT

TURN-OFF TIME TGQ —— MINIMUM PULSE WIDTH | RATING SPEED

MAXIMUM OUTPUT FREQUENCY —— MAXIMUM SPEED

APPENDIX II

30 KVA, 3 Phase Inverter

(D.C. Supply Voltage: 600 volts, I d.c. max.=500A).

Comparison of Transistor Inverter, Thyristor (SCR) Inverter & GTO Inverter

Parameter	Transistor	SCR	GTO
Switching Losses	0	+	++
Power Losses	0	+	++
No. of Semiconductor Devices	6 Tr	12+6 diodes	6 GTO+6 diode
No. of Electromagnetic Devices & snubber devices	6di/dt one main snubber	6 di/dt + 3 comm, choke + 12 snubber	6 di/dt choke 6 snubber
EMI	+	++	+
Accoustic Noise	+	++	+
Speed/Frequency Range	++	0	+
Capital Cost (Due to Device cost)	+	0	++
Running Cost including maintenance	0	++	+
Need of need not commulating circuit	-	yes	-
Volume	0	++	+
Reliability	0	+	++
Availability	+	+	+

Highest ++ Medium + Bad 0

Comparison of Machines for 30 KW Power Rating

	Switched Reluctance Motor	Asynchronous Induction Motor	Synchronous Motor or Brush less type	Induction Reluctance Motor
1. Optimum Power Rating for Operation	Not available Commercially (In R&D stage)	Easily available	To difficult to procure	Not available commercially, (In R&D Stage)
2. Efficiency	+	++	+++	0
3. Cost ++++ Highest 0 lower	+++	0	++	+
4. Size/Weight	++	0	+++	+
5. Accoustic Noise.	NO DATA AVAILABLE	+++	NO DATA	NO DATA
6. EMI	NO DATA	0	NO DATA	NO DATA
7. Type of Input most suitable	Pulse in put	30 sinusoidal input	30 sinusoidal input	30 sinusoidal input
8. Control Method	Pulse number/sec for speed & Pulse Amp. fir tirgue.	v/f constant	v/p constant	v/p constant
9. Power Output/ weight	+++	0	++	+