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SOME CONSIDERATIONS FOR THE ESTABLISHMENT OF SILICON FOUNDRIES AND DESIGN CENTRES*

by

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Explanatory note

The paper was prepared in the context of UNIDO's activities in the Arab region. However, some proposals it contains could also be applied to other regions.

Reference to "dollars" ($) is to United States dollars.

Summary

The establishment of an electronics industry in the Arab region, particularly in microelectronics, can take different paths ranging from design centres to full-scale wafer factories.

Technological developments now allow the successful design of applications-specific integrated circuits (ASICs) independent of a silicon foundry. The interfaces between user and manufacturer are standardised; mounted and tested chips can be delivered within a few weeks of submitting the files that describe the chip behaviour.

The study has therefore been able to examine the issues surrounding the establishment of design centres and silicon foundries in two distinct and separate discussions. Part I looks at three types of design centres: the electronic system development centre, the electronic component development centre and the design centre of a silicon foundry fabrication line. The specific tasks, know-how and investment costs of each centre are outlined. A typical training course to test the first Arab multi-project chip is described, covering content of lectures, basic literature and other elements like hardware and software.

Part II examines three types of silicon foundries in-depth: the analog standard biopolar line, the advanced CMOS line and the semicustom foundry. Various technologies and what they offer in terms of wafer and chip size, minimum dimensions and applicability to pilot lines and mass production are explored.

The study underlines the need for developing countries to gain access to microelectronics, to capture a share of the world market or to at least be self-reliant in the sector. Specific recommendations are presented on how to choose the most suitable technologies and how best to gain access to them.

CONTENTS

Part One

DESIGN CENTRES

INTRODUCTION

Previous UNIDO reports and studies have described the state of the electronics industry in the Arab region as follows:

(a) fabrication of electronic equipment is limited to a few locations;

(b) development of electronic systems is still restricted; and

(c) several public research institutes are involved in electronics but without strong links to industry.

From this, a basic recommendation emerges: The promotion of microelectronics should take into account all other aspects in the development of the electronics.

Chip processing is undertaken in a limited number of geographic areas while design centres are spread out in all directions. Chip fabrication is concentrated today in East Asia and in the United States. Unlike previously, today ICs are designed preferably on the application side while manufacturing takes place in any part of the world offering the best and least costly terms. To develop an electronics industry, specifically microelectronics, it is important that design centres be established and potential product applications be identified.

I. THE DEMAND FOR DESIGN CENTRES

Corresponding to the goal of developing all aspects of the electronic industry, three types of design centres are proposed: The first type is oriented mainly towards products. The second type, the development centre for electronic components, is the most crucial in starting the development of a national industry in integrated circuits. The third type is directly related to an IC factory.

This section sets out to investigate the technical aspects of designing electronic circuits. It is not meant to provide all the answers in running a design centre. Political and cultural considerations are beyond the scope of this study.

A. Electronic system development centre: Type I

Its main task is the development of electronic system prototypes for future production.

Its sub-tasks are:

(a) identification of market needs
(b) development of the electronics area
(c) development of other areas (say, in connection with the industry)
(d) development of the software area (if necessary)
(e) partial responsibility for marketing questions

These sub-tasks describe the typical operations of a small- or medium-scale company in an industrial country that aims to introduce and sell new products. The development centre of such a company may be separate from its production line. The Type I centre corresponds directly to the R&D division of a manufacturer of electronic products.

The R&D centres in the Arab region are not as yet strongly linked with a fabrication line, but they form a base that can be developed.

The know-how comprises:

(a) electronics hardware
(b) software
(c) marketing questions
(d) mechanics (e.g. design for cases)

Modern electronic market products are, above all, systems composed of software and hardware. Therefore, the main objective of a Type I centre is the development of systems realized by one or more printed circuits boards (PCBs) and by more or less extended software packages. To complete the design of the product, mechanical parts and peripheral elements also have to be developed (or bought), e.g. monitors, floppy discs and printers for personal computers.

The investment covers:

		(Estimates in US$)
(a)	hardware (Total)	85,000 - 170,000
	- measuring equipment	40,000 - 100,000
	- component stock	5,000 - 10,000
	- breadboarding	10,000 - 20,000
	- PLA development (programmable logic array)	30,000 - 40,000
(b)	PCB prototyping	
	- CAE workstation (computer edit engineering)	50,000 - 250,000
	- technology	100,000
(c)	software development	
	- personal computer	5,000 - 20,000
	- programs (emulation system)	5,000 - 10,000

The necessary equipment for ASIC equipment is listed for the component design centre (Type II).

Training topics:

(a) circuit design and theory

(b) computer science and programming

(c) use of CAE stations

Although only topics in the field of electronics are mentioned here, training needs in other fields should not be ignored.

The first two topics are taught in universities while the third can be summarized in a single course of perhaps two weeks. The same length of time is necessary for experts to be introduced to a special logic family or a special microprocessor system. But for the most part, training must be done through a regular educational programme. Short courses are successful only if focussed on special problems.

Most university graduates in industrialized countries are trained in theory and require further experience to to be able to determine the needs of the marketplace. This part of education takes place in industry itself. The transition from the theoretical to the practical is often called "the shock of practice". In developing countries, reaching this state of education is particularly difficult because of a lack of corresponding industry. (As a matter of fact, even graduates of universities in developed countries are generally not trained sufficiently in product development.) It would be useful if at least the senior staff of this type of development centre have behind them several years' working experience in the industrial sector in developed countries. To be successful, a centre must be led by a manager who thinks like an entrepreneur.

B. Electronic component development centre: Type II

Its main task is the development of electronic components.

The sub-tasks involve the development of:

(a) PCBs
(b) ASICs
(c) test of components and PCBs

This type of R&D centre is responsible for the electronic circuitry of systems, i.e. the hardware. The centre works with standard electronic equipment and standard components as well as with computer-aided design (CAD) equipment for the design of ASICs. The technology and equipment for the fabrication of PCB prototypes and the necessary testing machines should be available. But not all centres have to have their own PCB fabrication in-house. New technology like multilayer cards and SMD (surface mounted device) technology should, for instance, be concentrated in only a few locations.

This Type II centre may be a subdivision of the Type I centre although it is not necessary that the system as well as the single-hardware components be developed under the same roof. Many design centres in industrialized countries are responsible solely for specialized fields. Typically, software for PCB or ASIC development is offered by one such company that is well-equipped with the best tools. The expertise and the equipment in a specialized company often offer a less costly and faster solution than in a systems house. The systems house can concentrate its efforts on other more important, general aspects.

The know-how comprises:

(a) electronic systems and components
(b) analog and digital circuits
(c) bipolar and MOS devices
(d) use of CAD tools
(e) programming experience

There are three methods of circuit design:

(a) The hardware of electronic systems can be developed experimentally (as is usual) or by simulation. The experimental method uses standard components of the market, put together to a PCB or a breadboard. Errors are identified by measurements. Changes in the circuit are always possible during prototype development. Simulation is not used often. The experimental method is time-consuming and is not sufficiently accurate in the high-frequency range because of problems with long metal lines. Logic density is high in components like microprocessors, RAMs and ROMs but low in the other parts of the circuit where standard logic gates are applied.

(b) Replacing these gates by programmable devices - PLAs (programmable logic arrays), PALs (programmable array logic), FPLAs (field programmable logic arrays) and the different kinds of PROMs (programmable read-only memories) - increases logic gate density and reduces costs. The development of programmable devices is possible only through CAD. A special kind of simulation is used based on the Boolean description or truth tables.

(c) If the density of control parts still has to be increased further, then the design of ICs will be necessary. Automatic design styles like gate arrays or standard cells are the most popular ones today. However, for special applications, manual full-custom design could also be interesting. Here, no steps of development can be done without CAD equipment. The design is controlled mainly by simulation.

The first method of experimental breadboard development requires the least investment cost; it is still the most popular but not the best when all aspects are taken into account.

The second method, using additionally programmable devices, was introduced in electronic laboratories about two years ago. It has the same advantages as the first method, but special problems arise with the reliability of mass production. Density of programmable devices for random logic is still low compared with ASICs.

The third method of developing ASICs has been considered the best one for at least two to three years now but today only 5 to 10 per cent of all possible applications are actually made by ASICs. Only computer manufacturers have completely switched over to this method during the last year or two.

The design centre should be familiar with all these methods. The first method should be installed. The know-how will not be taught explicitly through special courses but will be expected from personnel trained in educational institutions.

The second method should be installed. A special course of two to four weeks should be sufficient to introduce this special technique if staff are experienced in the first method.

The third method is the latest and should also be implemented. Among the varying degrees of complexity in design methods, the semicustom one should preferably be introduced first. The full-custom design style should be restricted to a few Type III design centres.

Investment covers:

		(Estimates in US$)
(a)	PCB and breadboard development	85,000 - 170,000
(b)	CAD equipment for ASIC design	50,000 - 150,000

Training consists of:

(a) two weeks of PLA design
(b) four weeks of ASIC design

A course of about four weeks is sufficient to teach the fundamentals of one technology, e.g. CMOS, and to finish a design of a digital circuit of perhaps 200 to 500 gates.

Participants should be limited to a range of 20 to 25. Between 6 to 10 designs are combined in a multichip, which will be fabricated by a semiconductor company and then returned to the participants for measurements and tests.

The contents of a first course should concentrate on CMOS technology and semicustom design. MOS transistor technology and behaviour should be explained in detail. Out of the various CAD tools, only simulation and test programmes should be used. This is a base sufficient to allow the design of digital circuits to a 20-50 MHz frequency range. But the fast bipolar or GaAs (gallium arsenide) circuits as well as the whole field of analog design are still left to be tackled.

Digital design in CMOS is the most popular method today. The reasons for this are simple. CMOS is easy to understand, it can easily be designed automatically, and it offers high density and cheap fabrication as well as good electrical properties. There is no better alternative today in starting a microelectronics industry.

But in future the technology may offer new options. More appropriate CAD tools may become available and electrical performance is expected to improve.

The last few points show that obviously, education does not end after familiarity with one technology. If the present analog possibilities in Algeria and Iraq are taken into account, then it is necessary to implement the standard bipolar technology as soon as possible. Typical applications are circuits for consumer electronics, washing machines and cars.

Training is a continuous process. Other additional steps should follow directly from the first course. The direction of future courses will be determined by the identified needs of the market as well as by new technological possibilities.

C. Design centre of a silicon fabrication line (silicon foundry), Type III

Its main task is the development of integrated circuits.

Its sub-tasks are:

(a) full-custom design in different technologies

(b) semicustom designs

(c) test programme development

This type of design centre is directly related to an IC fabrication line. The technology of the designs is defined by the available process line of the factory. At the moment, two manufacturers are located in the Arab region, one in Algeria and another in Iraq. Both lines are bipolar. Since the processing of prefabricated CMOS wafers (gate array master) can be done without huge investments in the same factories, extending the fabrication to modern digital CMOS circuits is also possible.

The know-how consists of:

(a) analog circuit design

(b) transistor properties
- geometrical
- electrical
- technological
- parasitics

(c) semiconductor physics

(d) relations between geometry, technology and electrical properties

(e) measurement experience

(f) analog simulation

(g) full-custom design

Engineers required should be much more experienced than the digital staff of the Type II centre. The specifications in the know-how list are concerned with the full-custom design. In-depth knowledge is required because in designing a full-custom circuit, errors normally occur. Determining these errors by measurement is complicated because of a number of reasons. An error in the layout may be caused by the designer, or a process fault may be caused by the technologist. Since the technologist is not familiar with the circuit function, the designer alone is held responsible for the error identification. The designer should be knowledgeable about the circuit as well as the technology.

The investment covers:

		(Estimates in US$)
(a)	measuring equipment	
(b)	additional to Type II centre:	
	- wafer probing	50,000
	- device characterization	50,000 - 100,000
(c)	full-custom design station	100,000 - 300,000

The software of modern workstations is already rather perfect. Single programmes are also available free of charge from the universities. But the most important aspects, the programme for design rule check and circuit extraction from layout (the net list comparison programmes) are expensive. A commercial enterprise may be better off buying a complete workstation starting immediately with designs. For universities and similar non-profit institutions, one can also recommend proceeding the other way by obtaining the programmes from other universities. The software may not be perfect but at least once the source codes of programmes are obtained, CAD development can commence. The latter is an important task for research organizations, but not appropriate for design centres where running chips have to be developed under a tight time schedule.

Training is complex although simple courses would be sufficient. It is strongly recommended that co-operative training programmes with industrialized countries for at least one year be undertaken. Many European as well as American universities and public research institutes operate their own technologies and are well-suited partners for these arrangements. When the centre gains enough experience, it can serve as a nucleus for the training of other design groups at this level.

The well-known Mead-Conway method (see also Chapter II) offers the full-custom design method even to beginners. These courses have resulted in excellent ICs, but in general this is possible only if the organizing institute is sufficiently experienced in all aspects of IC design. This includes not only CAD and layout - which are considerably simple for beginners - but also all related fields like measurement and wafer probe handling. If the fabricated chip works correctly on the first try, that is, if the function can be measured by merely applying and recording the signals at input-output pins, then testing is a relatively simple task. But if errors occur, if parasites like temperature behaviour, noise, crosstalking and leakage currents have to be investigated, then complicated measurements must be done, which are not easy to understand and to interpret. The design books presented in Chapter II-C neglect this problem. Clearly, additional know-how from outside is necessary for success in this method especially when designing analog circuits. The expensive full-custom method is not needed in developing simple digital circuits. Good automatic design tools as well as inexpensive fabrication methods are recommended more for the semicustom method of Type II centres, explained in detail in Chapter II.

D. Problems in establishing design centres

Success in establishing any of the three different types of centres requires some general considerations. The first is that in comparing the success rates of different economic regions in microelectronics, one conclusion can be drawn: Research and training activities have to be concentrated through one principal centre.

Japan, for instance, founded the Ministry of International Trade and Industry (MITI) as its main focal point. As a result, Japan's microelectronic companies have achieved nearly the same level of knowledge and competition

from information disseminated through MITI. The establishment of research institutes of technology as a way of competing with Japan is under discussion in Europe and the United States. To solve the problem of lack of continuity in training in the Arab region, a high-powered institute also seems to be the best answer.

A centralized set-up becomes economical when the minimum investment cost increases to a level such that it cannot be borne by one company, much less by one country. This situation usually arises in the field of technology. The development of a submicrometer line needs several hundred million dollars. Thus, concentrating all human and financial resources in one agency is absolutely necessary.

Depending on the availability of resources, the same rule may be applied to all types of design centres. Apart from the minimum investment cost a second consideration should be given attention: If research and training dominate the activities of a centre, then the investment returns will be rather low and will never reach the profit level. Such a design centre needs public or private support or should be granted a non-profit status.

Based on both considerations, the Type I design centre for products is not suited for a centralized arrangement. It can be self-financing through its own successful product development.

The Type III full-custom design centre is normally part of a silicon factory. Indeed establishing such a division in a silicon foundry is absolutely necessary. When included in a technology line, its investment and maintenance costs are negligible compared with those of the technology.

One can then identify two candidates for a centralized arrangement: First, the silicon factory itself and secondly, the Type II design centre for electronic components. If a Type III centre for full-custom and analog design is founded independently of a factory, then it is also suited for a central arrangement. It may then be regarded as an even more powerful extension of the Type II central institute.

The following discussion on the advantages and the special functions of one dominating design centre refers specifically to the Type II design centre concept. (The foundry concept is discussed in Part Two.)

Two main functions justify the centralized operation. The first is the organization of courses so that sufficient participants as well as tools (terminals, computer power, measurement equipment) can be provided. This is valid not only for the initial course on digital CMOS circuit. Additional courses should be arranged on other design styles and technologies. Lectures should be updated regularly, corresponding to the state of the art.

The second main function is that of a so-called "silicon broker". To provide access to a technology as well as to inexpensive chip realization, various course designs and different designs of other centres have to be gathered and the corresponding multichips have to be prepared. This task is essential. Only one alternative exists: signing direct contracts with other multichip organizations, say, in Europe or in the United States.

The relatively low investment cost places the establishment of a Type II central design centre within the reach of a single country. Investment and maintenance costs are summarized below from a technical point of view. The variable costs for buildings and personnel depending on the country are not taken into account.

Investments in CAD hardware and software towards a Type II design centre are rather low. Progress in computer science and microelectronics have made computer power considerably inexpensive. Software prices depend above all on the number of installations. Since this number increases drastically as hardware costs decrease, obviously software costs can also come down. In other words, the ratio of software to hardware prices seems to be constant for most software products. In microelectronics, a standard software/hardware package of about $2 million in 1980 is available today for $600,000. In the meantime, the capacity of software and hardware is increased by a factor of at least 3. So, an improvement in performance by a factor of 10 has been achieved from 1980 to 1986. This development is expected to continue. The most important aspects today are the increasing capability of personal computers and the installation of nearly all software products on such PCs.

A central institute can be equipped with powerful hardware and software at a cost ranging from $500,000 to $1 million. Between 10 and 20 staff or training places and 5 to 10 working stations can be financed by this amount. If $200,000 to $500,000 are added for measurement and testing equipment and if the latest PCB technology is added, the upper limit for the central design

institute reaches $2 million. Standard investment in rooms and buildings is not taken into account. In comparison, $150,000 to 250,000 is the minimum investment cost for a small design centre mentioned in Chapter I-B.

The investment costs for the central institute are not so much the main financial concern as the relatively high maintenance costs. Maintenance costs can be divided into three categories: cost of depreciation and replacement of equipment, personnel and chip realization. In order for training needs to be filled, at least 10 designs have to be offered per year. Realized by two multichip project runs, $100,000 to $200,000 is needed, depending on design style and gate complexity. If some gate array runs for commercially interesting projects are added, then the sum should be doubled. Thus, the annual costs of the central institute for courses on chip realization would reach about $250,000. The replacement rate of the equipment is nearly 30 per cent a year. Every three to four years, old software and equipment have to be replaced by newer, more efficient products. This costs $600,000 if the PCB equipment is also renewed. Together with building and machine maintenance, annual costs are expected to be about $1 million excluding salaries for personnel.

A staff of between 6 to 10 grouped under three areas (administration, techniques and engineering) should form the nucleus of such a centre.

Since the courses last only a few weeks, sufficient time would be left to develop commercial ICs and to provide the product centres with the corresponding components.

An additional consideration is the interaction among the different types of design centres and their relationship with other central institutes in the region or in a country.

If the proposed concept worked successfully, then the number of product centres as well as the number of employees should show the highest growth rate. There would be fewer Type II design centres developing the necessary PCBs and ICs for the product centres. These design centres have good links with a silicon factory, if the country has one, but they also deal with various manufacturers all over the world. A single silicon foundry in the

Arab region can never offer all the necessary technological possibilities. On the contrary, one can expect only the fabrication that is concentrated in a small segment of the market to be commercially successful. This also demonstrates that a design centre and a silicon foundry involve different tasks and that one can exist almost independently of the other.

A five-year rate should be allowed for changing the former technological base. Perhaps in the future CMOS will be replaced by another logic family like BICMOS or ECL. Continuous development of design methods and of hardware and software tools is an important task of all design centres.

II. TRAINING COURSE ON IC DESIGN

Chapter I pointed out that the basic phase of education should be undertaken in educational institutions and universities over a certain number of years. If experience in electronics is already substantial, it can be supplemented with the latest IC developments through short-term training. This was underlined in 1980 in the famous book of Mead and Conway (see Chapter II-C), contrary to most expert opinion at that time. After the success of short-term courses, the term "the long thin man" was introduced into the discussion. The goal of such an education is not a broad introduction to each aspect of IC design. Instead, a small segment of only one technology should be focussed on, with all the design aspects of the particular electronic approach discussed.

Following this general idea, it has been demonstrated that highly sophisticated VLSI chips can be designed by inexperienced students. Since n-MOS was the dominant technology in 1980, Mead and Conway focussed on this base. Today n-MOS no longer represents the state of the art, having been replaced by CMOS as the most frequently used technology. One also has to bear in mind that the automatically generated layout (gate arrays, standard cells, silicon compilers) has become more widely used since 1980. The concept of the course, presented in this chapter, is a compromise between the two different approaches - a general basic education in technology and circuit design, and the practical aspect of designing a circuit of moderate complexity, which can be implemented at low cost.

A. General outline

Corresponding to the idea of the "long thin man", the course contents would be restricted to a small segment of the technology but would cover all aspects of electronic system design. The course focusses on:

(a) CMOS technology

(b) digital circuits

(c) (restricted) layout work

CMOS technology now dominates the VLSI design of new ASICs by more than 80 per cent. Nearly all semicustom methods use this base. The only exception in the digital field is the bipolar ECL logic. Because of faster switching time but higher power consumption and costs, ECL maintains a market segment estimated to be about 15 per cent in the future. The remaining 5 per cent is preserved for linear analog circuits.

Analog behaviour is another important aspect of IC design. Our environment is an analog one, and quick and inexpensive solutions to many problems can be formulated especially for applications in consumer electronics like television circuits. Future education should also include analog designs and should be extended to other fields. Starting out with CMOS seems to be a natural result of its actual importance and future needs. An additional advantage is that circuit design with CMOS can be explained easily.

A general trend towards digital solutions instead of analog ones has been observed for some time. Possibly this is because digital circuits can be designed by standard methods whereas the performance of analog ones is difficult to predict due to the influence of parasitics and other high-frequency effects. Thus, the selection of digital circuits fulfills the education and market needs.

The above-mentioned restriction of designing only the metal levels is one possible alternative to a general introduction on the layout of ICs. It is also the simplest one. Chip development always has a two-fold problem: one electronic and the other geometric. Circuit behaviour is dictated by the electrical properties of the transistor, the fabrication of a chip by its geometric size and shape. An introduction to IC design cannot overlook this

geometric aspect. This is in contrast with breadboard development where it is mainly the electrical properties of (standard) devices that have to be taken into account. The relation between the geometric size and the electrical behaviour of a transistor is one of the most fundamental aspects of IC design that needs to be understood at the outset. Most courses explain at length the conditions of layout, which are summarized in the set of design rules. However, two problems arise if this method of full-custom design is used in the accompanying practical training:

(a) Layout work will be tedious and error-prone. Within the defined period of the course, only small designs can be finished. Within the proposed schedule of three weeks, the area is restricted to about 100 transistors or 1 mm^2 of silicon. The system aspect then recedes into the background. To enhance the probability of running chips and to avoid design errors, a special check software and different design rule checks are necessary, also taking up a lot of time.

(b) Full custom chip fabrication will be expensive and time-consuming. ICs are fabricated by masks. Mask production is costly today, for 2 micron design rules costing nearly six times more than the technology run. Therefore, various designs have to be combined with one "super chip" so that mask costs are effectively divided into the number of chips or projects. This well-known "multi-project chip" method is essential in training courses to allow cheap silicon realization. Nevertheless, all 8 to 10 masks of a full-custom design are still more expensive than 1 to 3 masks for a gate array where only 1 or 2 metal levels are individually drawn by the customers, i.e. the course participants.

An additional problem is the fabrication time. At least six months for different multichip projects is the usual time interval between the end of design work and the delivery of fabricated chips. The gap is too long to maintain the interest of the trainees.

For this reason, the initial course should be restricted to manual gate array design. Manual design is necessary to provide an insight into the layout problems. But the design effort per transistor in the gate-array approach is reduced so that the number of transistors or gates being dealt with in the design process could be increased and solve a real logic problem.

About 400 gates are the expected volume to be treated by a group of two to four trainees. In that case logic simulation and testing (the most important aspect of automatic IC design) could be utilized on a scale close to the real one. Additionally, faster and less costly silicon production can be done by using the prefabricated "master" wafer. The theoretical part of the course is not different from that in lectures on full-custom design.

Modern digital IC design is dominated by automatically generated layout. A customer has to develop so many gates, leaving no time to look for the single transistors. CAD tools for simulation and test are the programmes mainly used. Installing such a course on "systems design" is also possible, applying only the automatic tools of the work stations. But then, the transistor as the base of all circuits is no longer visible. The proposed manual gate array design is a compromise between the modern automatic tools and the old and improved manual methods. Another possibility would be to offer different courses - at least two - covering these various aspects of IC design.

B. Content of lectures

The following curriculum, which gives an insight into the fundamental areas and demonstrates the use of modern CAD tools, is proposed:

(a) Introduction to fundamentals of MOS devices
(b) Introduction to CAD design tools
(c) Problems of systems design, design methods and chip engineering
(d) A case study or a practical example

The content of individual courses would be:

(a) Introduction to the fundamentals of MOS (metal oxide semiconductor) devices:
- MOS transistor theory, physics, electrical properties, structure, layout
- MOS processing technology, CMOS technology, fabrication route, layout, design rules, electrical parameters
- Basic logic gates, inverter, NAND, NOR, transmission gate, combinational logic, flip-flops and sequential logic (dynamic circuits)

For the first two topics, each trainee needs one double hour (2x45 minutes). Two double hours should be allowed for the last topic. The basic inverter theory demonstrates the principles of designing gates through the choice of appropriate transistor dimensions. The parameters influencing the behaviour of MOS circuits are also shown.

(b) Introduction to the CAD design tools:

- analog simulation and analog MOS models
- digital simulation and digital MOS models
- layout generation tools, manual, symbolic, automatic placement and routing, and silicon compilation

The trainees are introduced to the fundamentals of CAD tools, including the algorithms and their limits and possibilities. Four double hours should be allocated for this course.

(c) System design, design methods and chip engineering:

- Custom design and semicustom alternatives
- Structured design and testing
- CMOS gate arrays, state of the art and interface with the manufacturer
- Problems of chip engineering, packaging, costs and developing time
- Software and workstation review

These subjects deal with the environment and the logistics of chip design. Four double hours are also necessary as testing problems are involved.

(d) A case study:

- proposed technological base: 3 or 5 micron CMOS gate array for manual routing, e.g. UA4 of AMI, Austria, with a library of about 50 basic functions; upper limit: 600 gates, 48 IO-pads
- possible examples:

adder	(100-200 gates)
multipliers	(200-400 gates)
counter	(100-300 gates)
etc.	

The above-mentioned gate array is used by different German universities. About 100 designs are already fabricated. But any other base is possible as long as appropriate software is available. The software developed by the German universities is not perfect but can be transferred free of charge. So a beginning can be made without large investments.

The examples can be defined by the participants. In order to finish the different tasks - simulation, manual layout and circuit extraction from layout, i.e. resimulation after layout - two weeks of intensive work will be needed.

C. Basic literature

The following five books cover an overview of the course basics:

(a) Mead, Conway Introduction to VLSI systems. Addison-Wesley Publishing Corp., Reading, 1980.

(b) Mavor, K. et al. Introduction to MOS LSI design. Addison Wesley Publishing Corp., London, 1983.

(c) Weste, N. and K. Eshragian. Principles of CMOS VLSI design. Addison-Wesley Publshing Corp., Reading, 1985.

(d) Hurst, S. Custom-specific integrated circuits. Marcel Dekker, New York, 1985.

(e) Davio, M. et al. Digital systems with algorithm implementation. John Wiley & Sons, New York, 1983.

The first book is the classic introduction to the principles of n-MOS design. Even if n-MOS and full-custom design are no longer the preferred methods for today's digital circuits, this book is still strongly recommended.

The second and third books are more recent; they cover the state of the art in CMOS technology. However, modern methods of semicustom design and the possibilities of automatic CAD tools are explained only briefly. So the fourth book complements the other three titles well. The last book is a general introduction to digital systems and components.

Many other good books are available in this field.

III. TRAINING COURSE REQUIREMENTS

A. Basic requirements

The course needs a technological as well as a software and hardware base to be effective. The technological base will be a CMOS gate array for manual placement and routing like the UA4 array of AMI.

For the UA4 array, the corresponding software was developed by the universities and is therefore available free of charge except for certain commercial packages such as the logic and fault simulator. This programme can also be obtained free of charge by non-profit organizations. This software package does not fulfill the conditions for perfect integrated design systems like a state-of-the-art workstation but it covers all the necessary steps of simulation, layout, circuit extraction from layout and test analysis, and would be sufficient for the purpose of the course.

Course participants should later be able to design their own ICs on the basis of state-of-the-art gate arrays or standard cells. Thus, circuit design by simulation and testability is the most important aspect for future practical use. The layout of the UA4 is restricted to one metal level. The basic pattern of IC layout can still be recognized - the transistor structure, different mask levels, for example - but the task involved in manual layout is lightened and the problem of time-consuming design rule check is eliminated. The layout for modern interfaces between user and manufacturer is automatically made by the manufacturer and so the layout exercise is no longer that crucial. Even today's most complex ICs are designed automatically.

B. Educational background of participants

Engineers with theoretical and possibly practical experience in design of digital circuits by standard methods would qualify to participate in such a course. They would acquaint themselves with the special problems and possibilities of CMOS and acquire practice in the use of modern CAE tools. They would learn how to develop a circuit or system through simulation.

C. Duration of the course

The course should cover both theoretical and practical aspects. One week should be allowed for the introduction to the fundamentals and two weeks for designing a 400 gate example. If both aspects are combined, then an initial three weeks is proposed. About two or three months later, depending on fabrication time, one or two weeks more would be required to test the realized chips.

D. Software and hardware requirements

These are:

(a) Hardware for design (e.g. as used by German universities):
- VAX 11/750 or comparable VAX host computer
- Tektronix 4115 machines as graphic terminals

(b) Hardware for testing:
- DAS9100 Tektronics logic analyser (or another kind)
- Supplementary measurement equipment such as voltage sources

(c) Software for design:
- Logic simulator on gate level that allows timing simulation (including library of the used array)
- Graphic editor for the gate array layout (including library of the used array)
- Graphic editor for schematic diagrams, if possible, i.e. graphic input to the logic simulator
- Circuit extraction from layout for detection of errors in manual layout
- Fault simulation for quality calculation of test pattern

The data base for the design and for the transfer of the layout to a mask centre will be CIF. It will be converted to GDS II for mask fabrication.

(d) Software for testing:
- Interface programme to transmit the pattern block developed by logic simulation from the host to the logic analysers' word generator

E. Costs

(a) Installation tools:

If exactly the same hardware described above is available, one week should be sufficient to install all the design tools as used by German universities. Should the hardware be different, a time schedule for the implementation of th UA4 array data base has to be drawn up. For a modern workstation environment, not more than two weeks should be necessary. Presently, a cost estimate should cover one information-gathering mission and two weeks' installation time.

(b) Software costs:

As already mentioned, the software can be obtained free of charge by a non-profit organization. If additional interfaces have to be developed, the costs depend on the task and cannot be specified in advance. An upper limit of $10,000 should be assumed.

(c) Fabrication costs of the multichip project:

Between $10,000 and $20,000 should be budgeted if the following are decided on:

- One metal layer mask allowing for 10 different designs of a maximum of 600 gates per design

- Processing of two wafers by this mask. Shielding of metal lines by SiO_2 is not recommended as thereafter, correction of the chips, e.g. by cutting a line, is not possible.

- Sawing and bonding of chips. This process is performed without any specific testing of the chips. Only the correct functioning of test chips is guaranteed. The chips are delivered in a 48 pin DIL package.

(d) Training costs:

Taking into account a three-week course, a week of testing and two weeks of installation and preparation, a six-week consultancy contract would be necessary. Travel costs for three trips of six weeks in total should be included.

F. Number of participants

The number of participants is limited by the number of terminals and by the number of different possible chips. If enough alphanumeric terminals are available (for simulation), then about eight designs can be done with the help of four graphic terminals. Multiplied by 3 people in 1 group, the upper limit is 24 participants. The most crucial limitation is set by the availability of the terminal room. In order to give the course participants enough time, it should be open till midnight.

G. Summary

It should be pointed out that this is only one proposal for such a course. Many other data bases and software packages are possible. But each proposal has to set out the hardware and software for the technological data base as well as for chip realization. An alternative to the procedure installed in German universities may be a wide-ranging offer by a semiconductor company that includes all the mentioned components.

IV. CONCLUSION

The first Arab multichip project should be undertaken at a centralized location offering the best hardware (and possibly software) opportunities. The course will be open to participants from all Arab countries. If the applied software is available free of charge, then it can be handed over to the trainees at the end of the course and it can then be installed in their respective R&D centres. Since most of these institutions are equipped with VAX machines, software on this base would be preferable to others. The software transfer would guarantee that the course is not an isolated, one-time event but that it could be the starting point for an evolving microelectronics industry.

The other possibility would be to buy a modern workstation to solve the hardware and software problem. The amounts of $100,000 to $200,000 may appear prohibitive today but prices are expected to decrease in the future. It is only a question of time before each design centre gets an appropriate base for IC development. Installing continuous courses like the first will no longer be limited by software or hardware problems. Only chip realization remains expensive, making it useful to maintain a central institution for the collection and fabrication of different designs in multichip projects. The concept of the course presented here allows for a simultaneous realization of both learning chips and commercial chips, an ideal combination of theoretical education and application in the real environment.

The programme of lectures should be extended to cover other design styles and technologies. Organizing the courses initially at one central place also seems to be a feasible approach. But one problem cannot be solved by education alone: identifying market needs and the right people with good product ideas. Training and education in IC design is a prerequisite for future competitive products. Thus, the promotion of centres called for in the study of Type I centres is the most important task towards a viable electronics industry.

Part Two

SILICON FOUNDRIES

INTRODUCTION

Microelectronics is one of today's key industries, fast growing in production and influence. Countless modern products contain silicon chips. It is urgent, therefore, for the developing countries to gain access to this technology, capture a share of the world market, or to at least be more self-reliant in the sector. Through the establishment of a silicon factory, a developing country is introduced to the technology immediately.

However, one must bear in mind that the selling price of microelectronic components is low compared with an electronic system. Thus, utilizing the silicon chips would be preferable to producing them and setting up a design centre rather than a factory would be more desirable as long as access to the state-of-the-art technology is not hampered by occasionally imposed government restrictions.

Of course an indigenous source of chips acts as a catalyst for the development of an electronic industry, but the installation of a fabrication line can be expensive. Existing and future resources and goals should be taken into account. A step-by-step approach seems to be the best solution, starting out with the region's existing institutional facilities with some assistance from outside foundries. As an intermediate step, the present facilities could be upgraded and a pilot line set up. Finally, a full-scale silicon foundry would be proposed corresponding to the knowledge and experience gained and to the growing needs of the Arab market.

I. GENERAL REQUIREMENTS

A silicon factory cannot be specifically defined. First, different technologies exist addressing specific physical needs. Secondly, the production process can be divided into smaller steps which can be done in different locations. Thirdly, the factory has to offer different interfaces

to the user corresponding to current design styles. This range of activities can be likened to a matrix where each element presents a special solution addressed to a specific task, cost and performance.

More than 50 different process lines can be identified today. The material is either silicon or GaAs. MOS transistors or bipolar ones may form the basic elements. The transistors are characterized by different parameters, e.g. geometric size and dimensions. Minimum lengths enhance the speed as well as the density of elements on the chip, making size reduction the most important measure of progress in semiconductor technology. If higher voltages are required, larger distances are needed to absorb the voltage drops and minimum dimensions are no longer crucial. This is especially valid in power applications. Any other parameter can also be changed to fulfill any special need. Every set of parameter values can result in its own production line.

After a review of the fabrication process and the equipment, the main technology lines will be summarized according to application, task and other conditions. To gain a share of the world market, developing countries have to constantly seek additional solutions.

A. The production process

The production of an IC involves three main steps:

(a) mask generation
(b) wafer processing
(c) packaging and testing

1. Mask generation. From the data, stored on magnetic tapes, different masks are produced corresponding to the layout of the circuit. Each mask contains the geometric pattern for a specific step in the technological process. About 8 to 10 masks are necessary today to complete a design. Depending on minimum dimensions, the masks are generated by optical equipment or by electron beam exposure system (EBES). This task is often done in a special mask centre, which may not necessarily be part of the silicon foundry. Independent facilities exist, for example in Europe, offering efficient services.

For 5 micron minimum dimensions, optical equipment is sufficient. Pattern generators and step-and-repeat machines are available for a few hundred-thousand dollars. Modern electronic beam equipment for the 1 micron range, e.g. MEBES or ABEL, costs $5 million to $8 million. The pure optical method is sufficiently affordable to be installed in a factory while the modern electronic beam equipment would be a typical purchase for a specialized company. Except for direct wafer writing, (see Chapter II-3) buying the masks for such a centre is recommended. One set of eight masks in 2 micron rules for a 4-inch wafer costs about $30,000 to $50,000.

2. Wafer processing. The wafers are bought from companies specializing in crystal growth. The wafers are characterized by:

(a) a basic doping level (i.e. by a minimum electrical conductance)
(b) crystal orientation
(c) thickness
(d) diameter

Whereas the first three parameters do not influence the investment costs, the diameter determines equipment cost. Going over from a specific wafer diameter to the next larger one entails renewing all the machines. Today a diameter is already planned for 6 inches. Eight-inched diameters are still available for pilot applications.

It should be possible to install the present 4-inch standard at lower cost. The necessary equipment may be purchased today at, say, 10 per cent of the original price from companies closing their old lines.

Wafer processing is characterized by different steps with each step corresponding to a special mask. After the wafer is cleaned and after other surface treatment, a photoresist is applied. The wafer with the resist is then exposed to UV light through the mask. After development of the resist the patterns of the mask are shown on the surface. The most important and expensive machine in this process is the exposure system. Light is still used until 1 micro resolution. The equipment costs several hundred-thousand dollars. Systems are available according to wafer diameter and distance between mask and wafer.

The structural pattern of the wafer is used in the processes of diffusion, implantation, film deposition, metallization and etching to generate special physical properties in the silicon below the opened holes.

Approximate costs for the corresponding equipment are:

		(Estimates in US$)	
(a)	several diffusion furnaces	20,000	per tube
(b)	one ion implanter	1,000,000	
(c)	epitaxy reactor (for special processes)	300,000	
(d)	metal evaporation	150,000	
(e)	plasma etching	150,000	
(f)	low-pressure chemical vapour deposition	300,000	

All these machines are again characterized by their wafer diameters. Second-hand machines are available at lower prices but installing used equipment is complicated and needs experienced technicians. A compromise between new and used machines should be sought. Technology dedicated mainly to training objectives can be installed for a few million dollars. But this would not be appropriate for a silicon foundry and for mass production, which require a continuous production volume and an excellent quality level to produce sufficiently low-priced chips.

3. Packaging and testing. After the technological run, the circuit is ready from the electrical point of view. The only remaining tasks are making the circuit available to the normal user - this is done by a standard package - and eliminating all circuits that will not work correctly. The last function is filled by special testing machines.

To give an indication of the added cost of these additional steps, a rule of thumb is that for standard devices, nearly one-third of the fabrication costs has to be allocated to wafer processing, packaging and testing. The mask costs are not significant for standard elements since they can be used over a longer period.

Corresponding to its size, a circuit is repeated many times on a wafer. A circuit of a 4 mm^2 area and a wafer diameter of 4 inches result in about 2,000 chips which have to be tested individually to find out the running

devices. The number of good elements compared with the total possible number is called the "yield" of a wafer. The higher the yield, the lower the fabrication cost of single chips. Only high-quality technologies can compete on the world market.

To measure the chips on the wafer, a special testing machine is used. Faulty circuits are "inked" or characterized by coloured spots so that they can be excluded from further treatment. A testing machine including equipment to handle the wafers costs about $1 million.

The wafers are then sawed and the single chips are put into a package. The connection between the "pins" of the package to the input/output "pads" of the chip is normally made by gold wires. The process is called "bonding". Both automatic and manual bonding machines are in use today.

Finally, the packed chips are again tested in detail with the same testing machines used for the wafers. Only the "handlers" are different.

As far as the investment cost of packaging and testing is concerned, the testing equipment is the most expensive. Since every chip has to be tested at least twice, mass production requires several machines. In a memory line, perhaps 50 per cent of the fabrication area is used for testing.

Sawing machines and manual bonders are available for less than $100,000. Fully automized bonders cost about $200,000.

Testing and packaging investment costs vary significantly on a laboratory scale and for mass production. Human control is especially useful for packaging. Nearly all big semiconductor companies operate facilities in East Asia, for example in the Philippines, Singapore and Taiwan, to take advantage of less costly labour. A similar fabrication line in the Arab region would be an interesting possibility. Relative to bonding or packaging, testing requires a highly qualified workforce.

B. <u>The economic conditions</u>

As part of the total fabrication process, four tasks have been identified which may occur in different locations: the mask centre, the wafer technology, the packaging and the testing.

As already mentioned, the mask centre may either be within or outside a silicon foundry depending on the available investment volume and the minimum line width. Obtaining access to modern mask-making machines against payment is not a problem. Since the heart of the silicon foundry is the wafer technology, wafer testing should be included; packaging and final testing can be done outside. Minimum investment for wafer processing on a laboratory scale run into several millions of dollars but this is far from fulfilling the conditions for cost-effective production. Yield is the determining factor for competition on the world market. To reach the desired level of quality, the factory needs the best, dust-free environmental conditions possible. Personnel should be highly motivated towards accuracy and exactness.

If all these conditions are present and the managers are sufficiently experienced, then a last condition is necessary: the line has to run continuously. Normally, 500 to 1,000 wafers have to be processed per month so that millions of chips can be produced. A silicon foundry needs single products in big quantities - the key to a cost-effective operation.

These desired results cannot be achieved instantly. To expand the know-how progressively, a succession of measures should be followed. Links have to be established with manufacturers outside the region. A pilot line should be installed to serve as a training centre in preparation for a full-scale production line. These measures can be implemented using the present facilities by upgrading the existing bipolar lines.

C. The different technologies

The processing stage described together with the economic requirements can be applied to different classes of electronic circuits. Depending on the basic elements used, the bipolar and the MOS technology can be distinguished. Both technologies have had nearly the same market share in 1986. The classic bipolar processes are well defined and used in many analog and digital applications. The more modern MOS processes are applied mainly to the digital field; they cannot completely replace the bipolar devices because of other physical properties. The bipolar technology prevails in analog and high speed application, whereas MOS dominates the memory and the low-power and medium-speed digital business. Both these technologies have been advancing rapidly in terms of better performance so that their relative advantages have become slight. Either one or the other may gain a lead only in the long run as dictated by the market.

Improvements in general performance - especially remarkable for the minimum line width - result in higher speed and transistor density. Nearly every two years, the circuits improve by a factor of at least 2 in the price: performance ratio.

Standard analog circuits have stayed at almost the same technological level during the last 10 years since the higher voltages prevent a decrease in line width, as already mentioned.

Another development has been characteristic of the last five years. Because of advances in technology, the power of CAD tools has been increased to such a level that the design of ICs is no longer the task of a few specialists. People who are experienced in digital design today can develop their own chips. This will enhance the influence of microelectronics in other fields. Progress in microelectronics technology itself is reflected, for example, in the memory price and complexity. Gate array development, on the other hand, signals new possibilities of developing economical ICs of high logic density but low production volume.

This possibility of developing highly specialized chips at a relatively low price boosts support for the establishment of an electronic industry. The business of semicustom IC production requires a fabrication environment different from that of the mass production of standard devices.

II. TYPES OF SILICON FOUNDRIES

Following are proposals for three different types of silicon foundries: the bipolar analog foundry, the digital CMOS foundry and the semicustom foundry. A matrix of technologies can be ordered according to investment needs and desired benefits.

A. The bipolar analog foundry

This type of factory carries out the tasks of a standard semiconductor manufacturer. Many useful applications can be identified. Since the technological process is not highly sophisticated, investment costs for upgrading are not that high; rather, yield and quality are the most crucial elements for competition on the free market.

Characteristics of the technology are:

(a) standard bipolar process
(b) 4-inch wafers, 111-orientation, p-doped
(c) 5 micron minimum line width
(d) epitaxy process
(e) 1-layer metallization
(f) 25 mm^2 maximum chip size
(g) standard I/O-packages of less than 64 pins

These are the basic properties and requirements for analog circuits, characterized by breakthrough voltages higher than 20 V and less than 1,000 elements per circuit. The basic devices are npn- and pnp-transistors, resistors and capacitors. Diffusion dominates the doping process but ion implantation is also used for better definition of resistors. The mask can be produced inside the factory by standard optical equipment. Six mask levels at a minimum characterize the process.

Typical products and applications are:

(a) operational amplifier and related circuits
(b) consumer electronics

Typical fields of application are circuits for radio and television, washing machines, cars and telephones. This wide field of analog applications has established the existing image of electronics. This technology could also be applied to digital designs (so-called TTL-family) without any additional equipment needed.

Investment costs are:

	(Estimates in US$)
(a) main technological equipment (diffusion, oxidation, metal deposition, epitaxy, ion implantation, lithography)	10 million

(b)	packaging technology (sawing bonding, encapsulating)	100,000 - 500,000
(c)	testing (including many, cheaper tools for process control, parameter evaluation of test chips, and one testing machine with special test circuits)	100,000 - 500,000
(d)	design(full custom design, as described in Part One, II-C)	100,000 - 300,000

The investment costs differ greatly between a pilot line of limited output and a standard line for high-yield mass production.

A laboratory, including the buildings with clean rooms as well as the necessary equipment for the CAD-division, can be installed with partially used equipment for $5 million to $10 million. This sum should be enhanced to more than $20 million for a standard production line.

Maintenance costs

These depend heavily on production volume. Excluding personnel costs, a minimum of about $100,000 per year is necessary for a laboratory line to make a few test runs. A staff minimum of 10, at least two of them experienced, is required. For a standard production line the general rule is that maintenance costs per year are the same as the investment costs.

Problems

The big advantage of the bipolar solution is that a continuous upgrading of present facilities, say, in Algeria, can be done. The status of a pilot line as well as future mass production is possible. Many applications can be identified in the region.

Two main problems arise. First, the technology is rather mature. Many companies worldwide offer the same product spectrum. The most automatized lines can produce the cheapest devices, making it difficult to compete on the world market.

Secondly, to achieve an economi . . base, circuits that solve actual problems and can be applied in big quan..tites have to be identified and developed. This is usually possible although experienced engineers are required. The training of the design group is the most challenging task, perhaps greater than the establishment of a pilot line as long as high yield is not necessary.

Training

As mentioned previously, training cannot be undertaken through single courses of a few weeks. The establishment or upgrading of a pilot line should be done in co-operation with a running technology in Europe. Training staff through an assignment of one or two years in a fabrication line would be the best solution. This could be done in co-operation with a university or public research institute. Directly contracting with a semiconductor company is also an alternative.

Summary

This type of foundry/pilot line seems to be an ideal compromise in terms of present facilities, direct needs of the market, and investment and maintenance costs. It would not offer the latest in terms of complexity and speed but it would still be an actual technology because of our analog environment. For it to be successful, a good training programme or a a well thought-out co-operative assistance contract is required. Competing on the world market in standard devices may be a problem but if specialized circuits are invented this objective is attainable. Further discussion of this is recommended.

B. The digital CMOS foundry

The most spectacular progress in IC technology has taken place in computer science and digital applications. In this area, the most important chip is the memory element, dominating MOS production at nearly 80 per cent; it is also the driving force for line width reduction and performance improvement. Related to this technology, digital MOS logic has today reached a complexity of 50,000 gates per chip. The country dominating memory production, Japan, is also leading in microelectronics. The Republic of Korea is also making a headway in the memory market, which should inspire other countries to explore similar paths.

Characteristics of the technology are:

(a) Highly sophisticated CMOS process
(b) 6-inch wafers, 100-orientation p- or n-doped
(c) 1.3 micron line width in mass production
(d) 2 to 3 layer metallization
(e) 150 mm^2 maximum chip size
(f) I/O packages till 256 pins (pin grid arrays)

Smaller line widths and special packages of up to 500 pins are also available today. The typical system frequency reaches 20-50 MHz. Digital television circuits are possible. Only the high-speed range of optical cable transmission is still a bipolar (ECL) domain. Automatically generated layout seems to be the state of the art. CAD tools have reached a standard better than for any other technology.

Typical products and applications are:

(a) digital circuits till 50 k gates
(b) frequency range till 70 Mc/s
(c) computer hardware
(d) telecommunication
(e) any digital control

Low-priced personal computers and other inexpensive products in the computer periphery are the direct result of highly integrated ASICs. Consumer products are affected only if there are digital parts. The driving force is the field of computer science.

There is strong competition for digital bipolar technics. Whereas CMOS seems to replace standard bipolar TTL - and LS TTL-logic, bipolar ECL-logic offers approximately three times more speed but at higher power consumption, lower packaging density and therefore higher costs. The ratio of sales of ECL to CMOS is expected at 20:80. All forecasts point to CMOS as the standard digital technology for the next several years.

Investment costs are:

	(Estimates in US$)
(a) main technological equipment (implantation, local oxidation, multilayer technique, lithography, dry etching)	5 - 100 million
(b) packaging technology (sawing, bonding, modern packages)	100,000 - 1 million
(c) testing (tools for process control, parameter evaluation, general digital testing machines)	100,000 - 1 million
(d) design (full custom design, tools for automatic layout generation)	100,000 - 400,000

It is difficult to specify an investment volume. A 3 to 5 micron technology with a a one-layer metallization is available at th same price as the standard bipolar technology. But smaller line widths resul. in higher speed and higher packaging density and circuits with the latest technology lead in electrical performance. After a brief introductory period, they are also the cheapest ones. Only for (restricted) analog applications can one compete with an older technology.

For automatic layout generation, a two-layer metallization is absolutely necessary.

Including a co-operative assistance contract with a manufacturer, costs for the building, clean rooms and the design tools, the equipment for a 2 micron line would be between $30 and $50 million.

A memory line with the latest technology reaches several hundred-million dollars.

Maintenance costs

In a modern line, the continuous renewal of all equipment will entail the most expense. A small pilot line can be maintained by several hundred-thousand dollars per year, comparable with the standard bipolar technology. In a commercial operation, a rule of the thumb is that an amount equal to the investment has to be spent every year for all costs, i.e. maintenance, personal staff and development. This makes it possible to estimate the annual chip sales necessary to reach an economical base.

Problems

Digital circuits hold the key to progress in microelectronics. All the big semiconductor companies are engaged in this area but few are economically successful. Competing directly with them is not recommended. Access to highly complex VLSI circuits is also possible without owning the technology since the interfaces between designers and manufacturers are standardized today (see Part One: Design Centres). A possible alternative to fabrication abroad is the semicustom factory described below. For future competition in the memory market, mastering the technology at a lower level is a prerequisite. Training is the most important requirement in operating a pilot line on CMOS.

The technological problems are similar to those of the bipolar analog foundry. Additionally, one has to take care of a two-layer metallization. In contrast to the big hurdle of learning the design of analog circuits for the bipolar analog foundry, designing digital circuits is easy and the CAD support excellent.

Training

For the fundamentals of CMOS, special full-custom design courses can be effective. Co-operative programmes and longer on-site training are necessary to maintain the technology without continuous support from outside. Whereas there are only a few possible partners in the bipolar area, several public research institutes work in the CMOS field, facilitating co-operation.

Summary

An analysis of the various pros and cons reveals that establishment of a pilot line cannot be recommended to the same extent as it could for the bipolar foundry. Rather, development of a digital electronic industry should be supported through co-operation with the state-of-the-art companies from outside or by setting up a semicustom foundry as described below. Designing competitive electronic systems requires working with the best available technology, which is not guaranteed by an in-house pilot line.

C. The semicustom foundry

This new concept involves undertaking the final steps of the individual circuitry with in-house technology and obtaining the prefabricated "master" wafer from outside. After rights to the master and to at least two sources for predefined wafers are acquired, self-reliance can be reached.

Characteristics of the technology are:

(a) CMOS masters of 1.2 to 1.5 micron technology
(b) nominal maximum complexity 50,000 gates
(c) 2 to 3 layer metallization
(d) 150 mm^2 maximum chip size
(e) 256 pins at maximum
(f) 4 to 6 layer process (only metallization and contacts)
(g) direct writing or mask exposure system

This technology is characterized by the state of the art in digital CMOS random logic. Only highly regular parts especially memory structures cannot be achieved with the same device density as in the full-custom process described in section II-B.

Processing at least two layers of metallization is necessary since automatic CAD tools do not work successfully for one metal layer. The minimum dimensions of metal and contacts are twice as large as the minimum width (of the polysilicon gate) used for the master fabrication. Therefore, optical equipment for mask generation and projection is still acceptable. Depending

on the production volume of single circuits, direct writing on the wafer also offers an economic solution. The electron beam exposure system is applied directly to the wafer instead of first producing a mask. Prototypes can be fabricated fast and cheaply.

Typical products and applications are:

(a) any digital (VLSI) circuit
(b) computer industry
(c) any digital control part

Applications are the same as those in the state-of-the-art CMOS factory mentioned in section II-B. Only mass production is excluded, i.e. memory and microprocessor chips. Chip size and complexity represent the most advanced state of IC technology available. Highly sophisticated electronic systems can be produced.

Investment costs are:

		(Estimates in US$)
(a)	electron beam exposure system (e.g. MEBES, ABEL)	5 million
(b)	multilayer metallization, dry plasma etching	1 million
(c)	packaging technology	100,000 - 1 million
(d)	testing	100,000 - 1 million
(e)	design	100,000 - 400,000

The last three items are similar to the task of the CMOS silicon foundry mentioned in Chapter II-B. The main difference is that for the semicustom foundry, equipment for mass production and high throughput is not necessary; the conditions would be more similar to those in a pilot line. A total investment volume of $10 million may be sufficient for minimum requirements not only from the technological point of view but also from the commercial one. Since the semicustom foundry offers prototype services instead of mass production of low-priced standard chips, a pilot-line structure can be cost-effective.

Maintenance costs

Applying the general rule mentioned in Chapter II-B that an amount equal to the initial investment has to be spent every year for equipment renewal, personnel and process costs, then $10 million is needed to operate the semicustom foundry on a commercially profitable basis. Excluding buildings and personnel costs, a few hundred-thousand dollars are sufficient during the first phase of installation and learning.

Problems

A requirement is access to a master wafer, which has to be produced in a high-technology silicon foundry abroad. There are two options: buying the wafers and developing them. The first needs a joint co-operation agreement, the second needs time and experience. The master wafer itself has to be developed and the automatic layout tools must be obtained. A joint co-operation agreement may be the fastest and easiest way if there are no government restrictions impeding access to high technology.

The contract to buy the master wafers may also be extended to software tools and to training in the remaining steps of the technology.

Training

As mentioned, training can only be achieved satisfactorily through a co-operation arrangement. In the technology area the most important training is in the multilayer metallization technique. This step determines the yield and therefore the maximum possible chip size. The source of master wafers and the training partner can be different parties. A mastery of two- or three-level metallization can then be applied to wafers of any silicon factory in the world.

Summary

Setting up a semicustom factory is the least expensive and fastest means to gain access to the technology and to establish an economic base in the digital (CMOS) field. After sufficient knowledge has been acquired, the

possibilities can be extended to the full-custom CMOS line. In contrast to the full-custom line, however, the semicustom foundry has only to address a limited number of technological problems.

The impact on the electronic industry is the same as with a full-scale line since the resulting digital circuits represent the state of the art. This can be recommended strongly as the best path to a full-scale factory.

III. CONCLUSIONS

This study presented different types of silicon foundries and ways of gaining access to the technology. Among three possibilities - the bipolar analog foundry, the digital full-scale CMOS foundry, the digital semicustom foundry - the first and the last are especially recommended.

The bipolar analog foundry is an extension or an upgrading of present facilities. The analog chips can be applied to present and future electronic products in the Arab countries.

The semicustom foundry is recommended as the least expensive and fastest path to state-of-the-art digital chips. It should be the nucleus for an information technology and can also be the intermediate step to the full-scale factory.

Training for all three foundries cannot be organized in short individual courses. Co-operation with existing facilities, perhaps in Europe, and longer on-site training there are necessary.