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Technical report: Computer Aided Design of Darlington Power Transistors (Part II) *

Prepared for the Government of India
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SYNOPSIS

This report outlines the results accomplished and the problems encountered in Computer Aided Design of Darlington Power Transistors during the author's UNIDO consultancy in December, 1986, at CEERI, Pilani.

Attention was focused on testing and using the up dated versions of two software packages obtained from the University of Waterloo, Canada (Bipole for CAD of Bipolar Transistors, WATAND for CAD of non-linear circuits and the interface routine W model). These had been installed on the CEERI VAX 11/730 computer in November 86. Some technical results for dynamic behaviour under inductive load reverse base current drive conditions were obtained. An outline of seminars given by the consultant during his visit is also included. The report terminates with a brief section of conclusions and recommendations.

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I. INTRODUCTION

This 2 week UNIDO consultancy covers the period 10th to 19th December actually spent at CEERI, Pilani. This is the second UNIDO consultancy by the author. The first visit was for one month in April-May, 1985.

Between these two UNIDO visits, the consultant came to Pilani for 2 days in December 85 for a brief follow-up on the project. The consultant also arranged for one of his ex-graduate students from Waterloo, Canada to spend two days at CEERI, Pilani, in February 1986, to explain the WATAND computer program for thermal analysis of power transistors.

As part of the UNDP project, two of the CEERI Scientists spent 3 months (7 May to 7 Aug 1986) at the University of Waterloo for training in CAD of power transistors under direct supervision of the author of this report.

The CEERI scientists sent (with the cooperation of the University of Waterloo) up-dated tapes of the bipole program (for computer simulation of bipolar transistors). The WATAND program (for simulation of non-linear circuits), and the WMODEL interface routine from Waterloo to CEERI, Pilani in August. These arrived in Pilani late November and were installed on the VAX 11/730 computer and tested prior to the arrival of the consultant.

Because of the above listed exchanges, there has been continuity of effort on the CAD aspects of the power transistor project. For this reason, there was no delay upon the consultant arrival, in planning and executing a technical programme for

It was decided to focus attention on the following items :

- Testing the Bipole and WATAND software on the VAX computer to ensure correct functioning.
- Testing WMODEL to generate from bipole CAD tabular model files for WATAND.
- Initial computer simulation with WATAND of the 100 Amp. Darlington Transistor pair.
- Attempt to model free-wheeling diode
- Study reverse base drive turn-off to determine dynamic second breakdown conditions of Darlination and effects of the R1, R2 resistors.
- Preliminary trials of thermal WATAND.

In addition to miscellaneous discussions with CEERI Scientists on an ad-hoc basis, it was decided that the author would present three seminars/lectures on bipolar devices.

2. CAD STUDIES

2.1 BIPOLE ANALYSIS

Initial tests on the VAX computer with bipole indicated a bug when analysing the perimeter ring device. The VAX output stopped with no indication of the cause of the error. This problem was circumvented by re-defining the input parameters (starting current factor) RA (precision), NTOT (Number of Current Density Values) to be the same as for the input and output devices. This cured the bug.

No other problems were encountered with the bipole program.

2.2 W MODEL INTERFACE ROUTINE

This routine is used to create interactively the tabular models for use with WATAND. It was recognised during initial trials that best results would be achieved by using default options to all prompt questions (except for choice of base resistance VCB index, which should be selected close to the 0 Volt index for modeling heavily saturated transistors).

It was observed by A. Kumar and S.K. Mahajan during their UNDP work at the University of Waterloo that the value of the extrinsic base resistance for the perimeter ring of the output transistor was incorrectly predicted by bipole via WMODEL in the WIMBED file. The value had been manually altered. This point was investigated at CEERI before continuing. It was found by hand calculations that the value $R_{BEXT} = R_{BSQ} \ E_{SB}/B$ coincided with the value used at Waterloo. This value was therefore retained by manual editing of the WIMBED file created by W model. The reason for the discrepancy was traced to the fact that to simulate this perimeter ring transistor, in bipole, it had been represented as a single base contact integrated circuit transistor (ICI=2). Because of the unusual (for an IC device) geometry (ELEM $\approx$ 2000 micron, B = 10 cm) compared to an IC device (Emitter approximately square) bipole gave erroneous results. Because this perimeter ring is almost

a "parastic" transistor, contributing only 8 Amps. out of a total 100 Amps, no modification to the FORTRAN code of bipole is envisaged to cope with this unusual geometry. An alternate solution to eliminate the need for manual editing would be to treat this transistor as an equivalent 2 base contact discrete device (ICI = 0) with an emitter stripe length B reduced to 0.5 * B and width ELEM increased to 2 * ELEM.

It was decided to attempt to include the effect of minority carrier charge storage in the free-wheeling diode. Inspection of the bipole Fortran code (subroutine BIOMOD indicated that this could be represented artificially by increasing the extrinsic base dimension ESB. The modified output transistor is used in subsequent bipole/W MODEL/WATAND studies.

2.3 WATAND SIMULATION

The complete darlington circuit was set up as a WATAND file with manual editing of the WIMBED files so that three separate transistors (input, output, perimeter ring) could be modelled.

For a reverse base drive of 5 Amps., the current distribution within each transistor was examined. It was established that no breakdown condition occured due to L di/dt. It was further observed that for larger reverse base drive, the input

transistor turned off very rapidly, and the resistance R1 5 ohms.) prevented rapid turn-off of the output transistor.

Since the 300 Amp. design has been modified to include an external base contact, it was decided to examine the output transistor turn-off as an individual circuit (by creating a new WATAND file). It is hoped that this will provide useful information on the dynamic behaviour and RBSOA.

Ringing conditions were also studied by using a low value of inductance (10μH) to confirm that the diode could be driven into forward bias during the transient.

It was found that for high reverse base drive, large differences in collector current between adjacent cells occured in the 5 section Model. It was decided that comparisons should be made with 10 or more sections to determine the accuracy of the results. It was also found that the time increment, DE, used in the transient analysis had to be decreased below 0.1μs for large reverse base drive (e.g. 20A for the output transistor). These factors will be taken into account in future CAD work.

Specific results on storage time were obtained for the output transistor for a range of reverse base drive conditions

2.4 THERMAL WATAND

At the time of writing, it is hoped that initial testing of thermal WATAND will be performed for a two dimensional simulation of the output transistor.

3. SEMINARS AND TECHNICAL DISCUSSIONS

The consultant gave the following presentations :

a) To all CEERI scientific personnel :
Colloquium- Dec.15th : "Dynamic Turn-off behaviour and Thermal Analysis of Power Transistors".

b) To the members of the Semiconductor Devices Area :
Seminar - Dec. 16th : "An analytic approach to modelling current transport in base and emitter regions of bipolar transistors".

c) To the Semiconductor Society of India, Pilani Chapter Lecture : Dec.17th - "An overview of P-N Junction Theory".

In addition to the above, technical discussions took place on an ad-hoc basis with various members of CEERI scientific staff including the following : Dr. WS Khokle (on various aspects of Power Transistor Analysis), Mr. K.L. Jasuja and Dr. D.K. Thakur on details of the 100 and 300 Amp. Darlington Transistor). Interaction occured on a daily basis with the three members involved in the CAD aspects of the darlington transistor (S.K. Mahajan, A. Kumar and Dr. NK Swami).

4. CONCLUSIONS/RECOMMENDATIONS

Concrete results from the computer simulations would have been difficult to achieve in the short time available. Nevertheless, the new versions of the software were tested for functionality, several small problems identified and solutions found. A specific plan was agreed to be carried out in the immediate future at CEERI.

a) Examine accuracy of CAD results for output and perimeter ring transistor by increasing number of sections.

b) Extend the bipole results for the 300A transistor (Vcesat-I_c , BV_{ceo}) for collector doping of Nepi = 1.5E14 , 0.9E14 , 0.5E14 , X_{END}=70, 80, 90 /um.

c) Simulate RBSOA test circuit conditions on WATAND.

d) Explore reverse IB turn-off for various values of I_{B1}, IC (on), Inductance.

e) Study temperature distribution under static conditions using thermal WATAND for (i) two dimensional case (along a radial section), (ii) three-dimensional case, and (iii) above with emitter ballasting.

f) As a result of (e) determine utility of emitter ballasting and how to implement in a future design.

Finally, it was observed that use of the VAX 11/730 computer for bipole is very efficient due to the recent acquisition of the array processor. Without it, some of the more lengthy WATAND simulations would not be feasible. Weekend or evening use of the computer should be encouraged at CEERI to facilitate solution of problems requiring a large CPU time.

Final results with the Bipole-WATAND simulation programmes on the output transistor under inductive load turn-off conditions indicate that no dynamic second breakdown due to L di/dt phenomena occurs upto at least 700 volts. A ten section model was used, with only a moderate (50% at most) increase in collector current density compared to the five section model. Dynamic V(E), $J_n(E)$ remains well below the breakdown curve for this impurity profile obtained by A. Kumar and S.K. Mahajan using Bipole.

The explanation for this very safe operation stems from the fact that at Vcesat = 2V, the current density is less than $J_K/4$ where J_k is the Kirk limit (I_k = 410 Amps.). Even under large reverse base current the centre of the base does not become sufficiently forward biased for Jn to exceed Jk.

This (unexpected) result implies a very robust safe device for dynamic behaviour. Trade-offs could be made in choice of collector doping and thickness to economise in active silicon area at the expense of tighter margins on breakdown voltages. Alternatively operation at higher collector currents (and lower forced gains) should be possible before the critical dynamic turn-off condition for breakdown is encountered.

Notwithstanding the above comments, and in view of the many reports of unexpected failures of commercial power transistors, it is probably better to interpret the simulation results as confirming a well designed device with substantial built-in failure safety margins.