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INDIA

Technical report: Development of LSI/VLSI circuits *

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of P. Jespers,
expert in LSI/VLSI technology

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United Nations Industrial Development Organization
Vienna

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ABSTRACT

With the development of the PWM chip (containing approximately 11,000 transistors) and CEERI's growing competence in the design of integrated circuits, the question arises whether application specific integrated circuits (ASIC's), can be fabricated indoor or if they will require services of some silicon foundry. The recent decision of the DOE to provide substantial support for setting up a design centre at CEERI requires that the question be answered soon.

Further information on testing the PWM chip, CMOS training and a proposal for long term cooperation are presented.

CONTENTS

1. Introduction

Among the objectives stated in the UNDP contract with the Council of Scientific and Industrial Research (CSIR) involving the Central Electronics Engineering Research Institute (CEERI) located in Pilani, Rajasthan, consideration is given to the development of custom designed monolithic integrated circuits dedicated to transportation. The field of electronic control systems for electric vehicles indeed offers attractive features for it allows speed and torque control enabling higher efficiencies of AC motors. Pulse Width Modulation (PWM) furthermore minimizes explosive risks encountered in mines by the replacement of DC by AC motors.

CEERI, in the course of the contract, has set up a 40 KVA locomotive based on a PWM drive controlled by a microprocessor and standard integrated circuits. Even with a powerful microprocessor, some limits are imposed on the system performance which result from the large number of computation to be performed in real time. Hence, an area for Application Specific Integrated Circuits (ASIC's) had been identified during the second visit of the author. Its architecture was carefully planned in order to relieve the microprocessor from most of the repetitive tasks which slow down the entire system, leaving only the control strategies to the microprocessor.

The ADIC was designed later by a CEERI Scientist, Dr. Chandra Shekhar, during his stay at UCL, the author's institution (Université Catholique de Louvain, Batiment Maxvell, 1348 Louvain la Neuve, Belgium) and with the help of several scientists and students it resulted in the design of a large integrated circuit containing approximately 11,000 transistors. For testing purposes, as well as area limitations resulting from the use of a 6 micron NMOS technology, the circuit actually was divided into two chips. A 3 micron technology could have avoided this, but since the possibility to fabricate the circuit at CEERI was equally considered and CEERI had no 3 micron technology available, a rather conservative approach was taken.

The fabrication of the chip was carried out at UCL after e-beam mask making in Switzerland. Five wafers and a numbr of encapsulated circuits were brought by the author to CEERI during the present visit.

Besides the evaluation of the PWM chip performance, the purpose of the visit, as stated in the agreement between UNDP and the author also consisted in training CEERI's personnel in the design of CMOS IC's. Up till now, all design efforts were based on NMOS silicon gate technology only. Since CMOS is likely to become a dominant standard technology, the time has come to develop equal competence in CMOS design as in NMOS.

The next section of this report deals with a somewhat broader topic since it addresses the critical point of fabrication and deals with some strategic issues such as the importance to develop IC design know-how regardless of CEERI's capability to actually fabricate chips. The need for a global approach, including SCL as a potential ASIC manufacturer, will be addressed. The concept of a national Multi Project Chip Organization is proposed by the author and some recommendations made. Access to silicon foundries outside India is also considered but only a temporary basis as long as an agreement with an Indian Foundry has not been reached. The potentialities of CEERI's IC facility then are considered, and a number of proposals made in order to enhance its capabilities so that it could provide later local prototyping for ASIC's. It is not believed, however, that this can happen within a sufficiently short time in order not to hamper the development of IC design strategy. Hence, in view of the expected demand of industrial electronics ASIC's, which is believed to expand rapidly, the recommendation is made to search for external means of fabrication, preferably within India.

A status report on the testing of the PWM chip and a list of topis regarding the CMOS training follow. Recommendations are made on this occasion about the design and test tools CEERI should acquire in order to fulfil the requirements for ASIC development.

2. Semiconductor fabrication houses versus "Silicon Foundries"

Within the course of the last five years, a new concept has evolved regarding fabrication of custom integrated circuits (IC's) or application specific integrated circuits (ASIC's). Whereas mass production of IC's is achieved in semiconductor fabrication houses, ASIC's tend to be manufactured in special facilities called "Silicon Foundries". This trend is justified by the fact that the requirements on ASIC's concerning short turn around times, small quantities, availability of design tools do not comply generally with the objectives of semiconductor fabrication houses which are geared on to the production of large quantities and cost effectiveness in view of the strong competition with other semiconductor fabrication houses. The premises of a substantial market share taken by ASIC's in the future however, has shortly resulted in the emergence of new types of semiconductor fabrication houses that could meet the requirements of system designers. This became possible thanks to two factors: the trend towards very large-scale integration (VLSI) and the increasing availability of powerful design tools. First, VLSI is the result of an ever increasing demand for more transistors on the same chip and the possibility to make fine geometries and to the introduction of more sophisticated fabrication equipment, like direct steppers on the wafer (DSW), e-beam mask writers, e-beam direct writers on the wafer,

low temperature processes, dry etching etc., as well as a tighter control of clean room conditions. The second factor resulted from the work produced by a number of software houses introducing powerful hierarchical design tools, simulator as well as verification tools etc. This trend has resulted in shorter design times less prone to design errors. Cell libraries are also becoming available, some of which include large blocs of circuits, even as large as full microprocessors. Finally, more recently, silicon compilers are being introduced which drastically reduce the design time with error free circuits.

The concept of silicon foundries corresponds to a semiconductor fabrication line geared on the production of custom designed IC's based on a few well defined technologies, for instance: 2 micron N-MOS or CMOS, polygate, double metal. Silicon foundries provide sets of design rules to their customers enabling them to achieve compatibility with the requirements of the available technology. Some silicon foundries moreover provide software tools that enable their customers to deal with the complexity of large integrated systems. These tools span from gate array design tools (logical simulation, automatic routing, critical path determination, cell libraries, cell compilers) to custom IC design tools (behavioural simulation, [illegible]ng simulation, logic simulation, circuit simulation, as well as symbolic layout tools, compactors, mask layout tools, and for verification, design rule checkers (DRC), circuit extraction and verification tools, without mentioning cell libraries as well, and some silicon compilation tools). With the additional availability of an increasing number of powerful work stations or minicomputer based systems like microvax's Apollo, the trend to offer combined software and hardware tools also has emerged. Examples are silicon foundries like VTI (California and ES2 European Silicon Structures, Aix-en-Provence, France). The latter is aimed especially at very short turnaround times for complex circuits and small quantities only. It uses e-beam writing on the wafer to shorten the mask fabrication delay and is supposed to deliver chips within 2 weeks from reception of a mag tape description of the circuits. It also provides workstations and software tools both for gate arrays (Solo 1000) and custom IC's (Solo 2000). Of course it is obvious that the availability of silicon foundries paves the way to silicon system integration and that, in the coming years, more and more engineering effort will be put in the design of ASIC's.

With this evolution, the question should be addressed whether CEERI is going to design ASIC's to be fabricated on its own IC fabrication line or will require the services of a silicon foundry within or outside India. Some of the trends are considered in the next paragraph.

3. CEERI's potentialities for ASIC's

The requirements on the available technology at CEERI (8 micron, NMOS, polygate) in order to meet the demand of IC systems design are twofold.

First, scaling down of the actual technology from 8 to 5 and perhaps 3 micron is an absolute requirement regarding the number of transistors per chip required in order to cope with the complexity of systems (the PWM chip which was conceived in the course of the present UNDP contract contains approximately 11,000 transistors). Scaling from 8 to 3 microns, roughly increases the number of transistors by a factor 6 to 7. CEERI however should not consider smaller geometries than 3 micron, even when 2 to 2.5 micron become standard dimensions. The amount of effort required below 3 micron is too large, and much of CEERI's equipment should be updated. For instance, 3 micron technology yields junction depths well below 1 micron, typically 0.2 to 0.3 micron. With such shallow junctions, aluminium deposition for contact making creates shorts to the substrate if one does not deposit a mixture of Aluminium and 2% silicon. This prevents migration of silicon from the substrate in the deposited aluminium, which in turn fills the depleted regions with aluminium spikes somewhat less than 1 micron long but still larger than the thickness of actual shallow junction thickness. To perform correctly a deposition of silicon saturated aluminium, double e-beam evaporationer S-gun evaporation is required. Such evaporators are not available presently at CEERI but would be required when considering 3 micron technology.

Second, in order to respond to the demand of LSI systems designers, very stringent requirements on the organization of the fab line must be met. The responsibility of the fab line should rest on one single person with a well recognized authority and no access to the technology should be tolerated without the approval of the fab line responsible authority. This, unfortunately, is not the case presently for the lack of qualified technicians has compelled some scientists to take care of entire blocs of equipment (photolithography, diffusion, ion implantation, low pressure chemical vapour deposition, dry etching, etc.) Whereas most of these groups understand the need for co-ordination, some unfortunately, do not. This results in weak points in the fab line that can only be corrected by rearrangements of personnel. It would be helpful to introduce the concept of collective achievements. The management decisions taken in this regard should be implemented quickly.

Hence, while recognizing the advantages that can be gained from an indoor IC fa-. line, one must conclude that several preliminary conditions must first be met before a reliable and fast turnaround fab

line which meets the needs of circuit and system designers can be considered at CEERI. If proper action is taken, however, chances to fabricate IC prototypes may exist provided a single, well recognized individual with the power to run the facility, has been identified.

4. Proposals to meet the objectives of ASIC's development

It is likely that the time span required in order to set up a foundry-like operation will overlap with the demand of ASIC's for two reasons.

First, design expertise has emerged at CEERI during the past years under the leadership of Dr. Chandra Shekhar consecutively to the UNDP contract and the experience gained in the design of the PWM chip. The success of the effort has been recognized recently by the D.O.E. (Department of Electronics of India) for a proposal to open a "VLSI design centre for industrial ASIC's" was approved recently.

With the introduction of efficient design tools CEERI will get started in the course of 1987 with the design of integrated systems of the same complexity as the PWM and even more.

Secondly, the consiousness of the benefits silicon foundries can offer and the clear cut separation it allows between design activities and the running of a fab line, undoubtedly will trigger a large interest among the Indian Industrial community and foster mushrooming of design centre proposals. In a couple of weeks, an announcement was received at CEERI about the presentation in Delhi by the President of a Swiss Company (Mr. E. Uhlmann, Lassaray S.A. Brugg) of a lecture on the manufacturing of ASIC chips. A visit of the chief manager for new projects of the Madhya Pradesh State Electronics Dev. Corp. Ltd. (OPTEL) to CEERI clearly indicated the wish to make also IC design in Bhopal. The Indian Telephone Company already is doing some IC design for telecommunication applications and there is a pressing demand from the Delhi Extension Centre of CEERI to enter rapidly in the field of ASIC's. The wide field of industrial electronics CEERI encompasses, represents an ideal opportunity for crossfertilization between system expertise (power electrical engineering, telecommunications, industrial electronics) and IC design.

Both reasons, very soon will create a demand that should be met in the best possible manner and with the shortest possible delays in order to build on the potential CEERI can offer before similar initiatives are taken somewhere else. The problem CEERI is thus facing can be put

as follows: how to provide fast turnaround silicon wafer fabrication for ASIC's.

Preferably, fabrication should be done in India. There seems to be only one place that would presently offer the kind of service which is required: the Semiconductor Complex Ltd. (SCL), Chandigarh. The question of course arises whether SCL, which is typically a semiconductor fab house, is prepared to accept the increased load which comes along with the introduction of ASIC wafers fab. Hesitation on the part of SCL can easily be understood. One way to overcome this problem at least partially, could be to consider SCL's technology as the only one available (3 micron CMOS, now being upgraded) and the corresponding design rules. Demands concerning chip technology to meet individual demands for ASIC's should be proposed to the users of SCL's technology, with say 3 to 4 runs, per year for instance. Mask making, of course, should be considered carefully in accordance with SCL requirements. To be successful, it may be advisable to set up a central co-ordination centre outside SCL where potential users (CEERI, education institutions like IIT's as well as newly formed design centres) could submit their mag tapes in a well defined format for final chip layout in order to avoid the burden SCL cannot accept.

This procedure offers great similarities with what is taking place in USA, Europe and Australia namely, the multi project chip (MPC) concept. Such an initiative would certainly offer better guarantees for SCL and avoid meeting anarchic demand from isolated users. Special budgeting for the MPC activity would be necessary in order to defray SCL expenses. If this proposal can be accepted, the DOE perhaps could help to set up a nationwide service that would play an important role in the development of India's electronics industry and education institutions.

In case SCL could not accept the proposal, however, an attractive solution may be found through silicon foundries abroad. The cost of an MPC type fabrication consisting of 12 wafers in a silicon foundry like VTI amounts approximately to 12,000 dollars per user when the wafer is shared by 3 users.

The prices of ES2 are not yet known but are likely to be even lower. This of course does not include the cost of design, nor the cost of dedicated work-stations and software acquisition. But, assuming that this is already covered by other means, these figures, as well as the short turnaround, could meet demands for ASIC's.

5. Proposals regarding CEERI's IC fab. line

A lot of effort has been put in the course of last year in order to try to establish an IC fab line at CEERI, separated from the material

science lab. In order to set up a reliable IC fab line for protctyping that could parallel the MPC like operation described above, the following proposals are made:

i) The first priority, as already mentioned, consists in a thorough reorganization of the IC fab. It should be under the control of a single person. Collective achievements should motivate the group working under his responsibility. Objectives should be defined in accordance with reasonable targets and the means to achieve the goals should be made available.

ii) The facility should be run on a permanent basis without shutting down furnaces during idle period and carrier gasses should flow all the time in order to prevent pollution. Special attention should be given to the LPCVD furnaces in order to keep steady state conditions and avoid problems with the tubes, as well as the mass flow meters.

iii) One of the duties of the IC fab responsible should be to check the availability of gas reserves as well as spare parts. Some equipment requires service contracts in order to avoid long idle periods (mask aligner, evaporation, ion implanter).

iv) Updating the equipment should be under control of the fab line responsible in order to evaluate priorities.

v) Mask allignment will be updated soon by means of a new Karl Suss contact printer. Since CEERI has a mask copier, there is a possibility to replace masks in due time before the yield goes down (almost 5 printings). This requirement needs to be fulfilled for LSI design whereas single devices do not suffer from similar/yield problems.

vi) The ion implanter whose current has decreased by a factor of 3 since its installation could be checked by the manufacturer in order to achieve some readjustments of the beam. It would become a bottleneck otherwise.

vii) The LPCVD unit used for poly and silicon nitride deposition is not in operation. Putting it in order is a priority, for without this, there is no way to run the facility.

6. Test carried out on the PWM Chip

A sample of 5 wafers containing the PWM chip and 12 encapsulated circuits are available. Testing under the prober has been carried out on the following items:

i) Two phase clock generator.
Checking of overlap conditions.

ii) Control as well as clock buffers.

iii) 16 bit counters used to trigger the thyristors.

iv) Reset control sequence of the PLA.

All tested parts were found operative. A logical error was found in the control part. Fortunately, it can be avoided by means of external circuitry so that it does not affect further tests. This error, of course, shall be corrected in a further design.

More testing of the encapsulated circuits will be required in order to further evaluate the performances of the circuit, but the available number of contacts on the prober is not sufficient. This will require more time in order to fix an experimental test set. A list of test vectors used at UCL, where the same work is going on was given.

A substantial improvement of the test system is a priority requirement. It is recommended to search the co-operation of the device test group where some work has been done previously when the telephone exchange circuit developed by CEERI has been evaluated. Objectives to meet the needs of this important growing field should be defined rapidly in co-operation with Prof. Maxwell.

The testing of the PWM chip already suffers from the unavailability of test equipment. A test station built around a personal computer such as the IBM XT could fulfil the needs for an amount not larger than 6 or 7 lakhs. UCL is faced with the same problem. Some exchange of information on this issue will take place as soon as possible.

For probing test chips, the actual prober should be equipped by means of standard probing cards corresponding to one or two fixed patterns of bonding pads (24 or 48 for instance). These patterns should be stored in the cell library in order to avoid using other patterns and reduce the cost penalty associated with too many probing cards. Attention should be given to the capacitive load of coax cables when connecting the probing card to the test station. A good practice is to use a second card with buffer amplifiers on the probing card itself.

7. Review on CMOS design topics

Training of personnel in CMOS design took most of the time, in accordance with the UNDP assignment.

In this section we restrict ourselves to the list of topics which resulted from the planning meeting held on Wednesday 17 December 1986. An introduction lecture was given first on Thursday 18 December 1986 on the topic "Why Design Systems with ASIC's" for a large audience in order to create interest among members from other areas. The attendance later stabilized around 10 to 15 scientists.

Date	List of Topics
Friday 19 Dec.	Comparison of CMOS invertor versus NMOS, speed, power consumption.
Monday 22 Dec.	Logic CMOS circuitry, static and precharge (dynamic) logic.
Tuesday 23 Dec.	Synchronous logic, domino logic, nora logic 2 and 4 phase logic.
Wednesday 24 Dec.	CMOS bus organization.
Monday 29 Dec.	Small signal analysis of CMOS basic inverter.
Tuesday 30 Dec.	Comparison with analog NMOS circuits. Differential amplifiers analysis.
Wednesday 31 Dec.	CMOS op amp. trade offs. Frequency response for unconditionally stable circuits.
Monday 5 Jan.	More advanced CMOS op amps. and switched capacitor fitters.
Tuesday 6 Jan.	Bus architecture (2nd part)
Wednesday 7 Jan	Bus architecture Bit slice Adder - Substractor

A number of typical digital CMOS circuit layouts were considered and technical data and layouts were given.

8. Design Tools

This important item needs careful attention. Presently CEERI is running several software programmes for circuit design, like SPICE and SPLICE (with some problems). Layout can be performed at the CEERI extension of Delhi with an Applicon machine. Some work is also being carried out under the direction of Dr. Chandra Shekhar with students concerning a programmable logic array compiler.

A survey of SCL's available software could be made thanks to the information given by a scientist of CEERI. The following items were mentioned:

- Fixed grid symbolic layout package
- Circuit simulation and logic simulation
- Various circuit extraction tools
- Design rule checkers

Also available are:

- an interactive gate array layout tool
- a polygon level interactive graphic tool

Most of the software runs on workstations connected to a PRIME computer.

Comparatively to SCL, CEERI's present software is rather poor and does not represent an integrated set of design tools. Hence much effort is required when a hierarchical design process is initiated.

The acceptance by the DOE of CEERI's proposal to set up a "VLSI design centre for industrial ASIC's" will substantially improve the situation however.

A thorough market analysis must now be undertaken (VTI, SDA, ECAD, SYLVAR-LISCO, ES2 - if available) keeping in mind that servicing also is an important item that should not be overlooked (considering computer software as well as hardware). The trend now-a-days is to utilize one of several inter-connected work stations (Microvax, Sun, Apollo). In the author's laboratory, VTI software tools are used with a VAX 750 computer, two microvax and several Tektronix colour terminals (one 4115).

This is still in an early stage. The author is willing to provide future guidance when the market survey of CEERI will be initiated.

Whatever the results of the survey may be, any decision should not be taken without giving proper consideration to the outcome of the silicon foundry problem.

9. Long-term co-operation (Project between CEERI and UCL)

A draft proposal for a collaborative research "project" was elaborated during the present visit. Co-operation between CEERI and UCL indeed has grown steadily since 1981 thanks to the support of UNDP to CEERI. Several scientists from CEERI have spent 2 to 6 months at UCL in order to get acquainted with the NMOS and CMOS processes. One scientist spent a year at UCL under a fellowship delivered by the CONSEIL DU TIERS MONDE of the University. Further, in the course of his three visits the author has trained CEERI personnel in the design of NMOS and CMOS integrated circuits. The contract with UNDP on "Semiconductor Devices and Electronic Subsystems for Transportation" led to the design of a novel chip which has been processed at UCL and is presently being tested. The chip architecture was defined during the second visit to CEERI of the author and the design took place at UCL during the stay of a CEERI scientist in UCL.

A very active team was formed on this occasion with students and scientists joining their efforts with CEERI. The opportunity to use available design tools at the university not only enabled CEERI to achieve the design of the chip but also may have helped CEERI to identify the kind of design software which should be implemented. The support recently given by the department at Electronics (DOE) now enables CEERI to set up equipment design tools in its own laboratory.

It turned out that the PWM chip contributed to form the basis of a potential long term co-operation between CEERI and UCL. CEERI indeed is offering a 40 KVA transportation model which will be used for testing the chip ultimately under real use conditions. In fact, CEERI's expertise in the testing of high power inverters up to 180 KVA ratings and test facility for 50 KVA AC motor drives can be used for new generations of smart power IC's. UCL in the meantime has undertaken investigations on a new ASIC intended for power applications. A feasibility study of an integrated circuit for the protection of power rectifiers against mains failure has been started during the past year. An investigation on the requirements of power control processors also is being undertaken in order to define specification that could be implemented in a programmable processor, which could be used for PWM drives as well as some other applications.

Hence, some of the ingredients for cross fertilisation do exist which offer means to work out common achievements. Chances that the Indian Government would support such an initiative are real. On the other hand, the Conseil du Tiens Monde of UCL will be approached by the author in order to examine the possibility to support exchanges of personnel in the frame of the project as well as the possibility to fabricate prototypes in the 3 micron NMOS or CMOS technology available at UCL.

The draft proposal already mentioned above has been signed by the Director of CEERI, Dr. G.N. Acharya and by the author on the 2nd of January 1987. It will be forwarded to the relevant authorities both in India and in Belgium for getting their support.

10. Additional Information

An up to date record of the UCL N well CMOS 3 micron process was given to the IC fab. group as well as a notice on UCL clean room procedures (ref. A. Grahay).

A discussion took place with a person taking care of CEERI's buildings on the requirements for IC fab. constructions. A short description of the new Philips facility of EINDHOVEN was given.

11. Conculsion

The PWM chip must be further tested. Ultimately, it will replace some parts of the present 40 KVA test vehicle and enhance its performance.

A number of scientists were exposed to CMOS design techniques.

There is a good prospect that CEERI may set up a design centre equipped with proper design tools. As the demand for ASIC's is increasing rapidly, the necessity to have access to a silicon foundry is underlined. CEERI's IC fab. should be reorganised in order to provide parallel processing facility.

A proposal for long term co-operation between CEERI and UCL was elaborated.

The author wants to thank the Director of CEERI, Dr. G.N. Acharya, as well as the UNDP expert Dr. Amarjit Singh, for making his various stays so fruitful as well as agreeable. He expresses the wish that CEERI may take the lead in the design of ASIC's.

He also expresses his thanks for the support given by UNDP.

Pilani
7 January 1987

Prof. P. Jespers

DRAFT PROPOSAL FOR

COLLABORATIVE RESEARCH "PROJECT"

between

CEERI (Central Electronics Engineering Research Institute,
Pilani, Rajasthan, India)

and

UCL* Microelectronics Lab. (Batiment Maxwell,
Place du levant 3, B 1348
Lauvain-la-Neuve, Belgium).

On the development of
Application - Specific Integrated Circuits (ASICS)
for Industrial Electronic Systems including Transportation

Note: This proposal was prepared during the visit of Prof. Jespers to CEERI, Pilani from 12 Dec. 1986 to 11 Jan. 1987 while under UNDP assignment. It is based on the experience of a growing co-operation during the last 5 years between CEERI and UCL. This document has been prepared in view of the visit of Director, CEERI (Dr. F.N. Acharya) to UCL in May or June 1987 aimed at the establishment of a co-operative project between the two institutions in the above area.

* Université Catholique de Louvain.

1. Historical overview of the co-operation between CEERI and UCL

Co-operation between CEERI and UCL started in 1981 with the first visit of Prof. Jespers to CEERI as a UNDP expert (United Nations Development Programme). The purpose of his one month long visit consisted mainly in training a group of CEERI scientists to learn integrated circuit (IC) design. A survey of the capabilities of the Semiconductor Device Laboratory of CEERI was also carried out and recommendations were made in order to improve the fabrication process of NMOS polysilicon gate transistors. A second visit took place in 1985 after a new contact was established between CEERI and UNIDO following a project proposal entitled "Semiconductor Devices and Electronic Subsystems for Transportation". During this visit the basis for potential long term co-operation was actually laid down. A P.W.M. microchip was defined and specifications were drawn up in order to determine the feasibility of an integrated circuit which would drive a Thyristor Inverter for converting DC to AC three phase power supply for A.C. Motor Drives. The actual design took place between the end of 1985 and the beginning of 1986 at the Laboratoire de Microelectronique of the UCL in a total time span of six months. It was achieved by a CEERI scientist, Dr. Chandra Shekhar, working with three engineering students of the Faculty of Applied Sciences. The actual chip which contains more than 10,000 transistors was fabricated at UCL after Dr. Chandra Shekhar's visit and brought to CEERI during the third visit of Prof. Jespers in December 1986. Testing is still being carried out with success.

Meanwhile several scientists from CEERI came for further specialization in UCL: Mr. R.C. Dubey who obtained a one year fellowship from the Council du TiersMonde (UCL organization for co-operation with developing countries) Mr. O.P. Wadhawan and Mr. Ramachandra both visited under UNIDO for 6 and 2 months respectively. All these scientists were associated with the development of the technology. Another scientist from CEERI is supposed to stay in UCL for 2 months in the beginning of 1987. The Director, Dr. G.N. Acharya is also likely to visit the University during his study tour in May - June, 1987 under the UNIDO funded project.

2. Activities of Common Research Interest of CEERI and UCL

CEERI is one of the National Research Laboratories of CSIR aimed at the development of Industrial Electronics Systems and Microwave Power Tubes. It has a strength of approximately 700 employees. Its activities cover a number of applications including modernization of Sugar and Paper

Industries, Transportation involving Electric Vehicles and electronic devices and systems for various applications including Space and Museums Electronics. A large semiconductor device group (approximately 60) is active in fields such as power transistor development, Hybrid Microcircuits and IC fabrication. The main purpose is to transfer know-how to industrial undertakings located in India and also provide specialised training facilities such as computer training.

CEERI has received in the past substantial support from the United Nations Organization (UNDP) for development of semiconductor devices. The present contract which ends in October 1987 is aimed at the development of Electric Vehicle Drives using three phase asynchronous A.C. motors fed from DC power. The use of power thyristors or transistors in the pulse width modulation mode (PWM) offers attractive features for it allows proper torque control and enables higher efficiences. P.W.M. furthermore minimizes explosive risks encountered in mines by the replacement of DC by AC motors.

Presently, an experiment is carried out with a 40 KVA locomotive using a PWM drive built by means of standard integrated circuits and a microprocessor. The chip already mentioned above, should be substituted later to some parts of the present hardware system in order to enhance its functionality and improve reliability.

The microelectronics laboratory of UCL headed by Prof. P. Jespers, is part of the EE department at UCL. There are more than 40 people working in areas such as solid state devices, IC technology, IC design tools, and ASIC's (Application Specific IC's). A full operational NMOS and CMOS fab line for 3 micron devices is available for prototyping ASIC's and research purposes in 2D (two dimensional) process simulation. Also, design tools are available, a VAX 750 and two Microvax stations are used in conjunction with available VTI software. Research on specific power IC's began in 1985 with the design of the PWM chip and its fabrication. A second project was started in 1986 with Prof. Garrido (UCL + Lisbon Research Institute) concerning the feasibility study of an IC for protecting semiconductor power rectifiers under failure conditions. On the basis of an algorithm developed by Prof. Garrido, the projected chip is supposed to predict the evolution of current and voltages so as to determine whether or not switching of the semiconductor rectifier is required. Presently, the decision is taken always to switch off in order to avoid the destruction of the power rectifiers. The purpose would be to avoid such decision in the future whenever it is useless. A major problem one has to deal with is the extremely large number of computations required in a very short time, well out of the reach of microprocessors, but perhaps within the possibilities of an (ASIC) tied to a microprocessor. If so, it would be possible to provide low cost hardware suitable for the protection of large numbers of semiconductor power rectifiers. Presently, only the feasibility study is underway with the help of two of the designers who worked in the past with Dr. Chandra Shekhar (Scientist CEERI) on the design of the PWM chip, now assistants at the microelectronics lab.

3. Proposed Collaborative Research Programme for ASIC Design and Fabrication

Large developing countries like India need expertise in some most advanced technologies in order to foster the development of their own industries and reduce the dependance on the developed countries. Microelectronics plays an important role in this respect for it is believed to have a major impact on many other activities. If we consider only the case of electronic devices and systems for A.C. motor drives, there may be spin-offs such as solar pumps, agricultural water pumps, centrifugals in Sugar Industry, airconditioning controls and a host of other A.C. motor drives for domestic as well as industrial applications.

On the other hand, smart power IC's have been considered by the EEC in the ESPRIT program. They offer interesting opportunities for Belgium industries such as ACEC which already has a project in this field with SdM (Societe de Microelectronique, Loverval).

A common program for long term research would be beneficial both to India and Belgium. As an example, consider PWM drives CEERI is offering a 40 KVA model which can be used for testing the chip under real use conditions. In fact CEERI has a good Power Electronics Laboratory capable of testing High Power Inverters up to 180 KVA ratings and a test facility for 50 KVA AC Motor Drives. CEERI also provides expertise in the power aspects and has an IC design team geared on this problem. UCL, through its software tools for IC design as well as its fab. line has the potential to actually design and fabricate prototypes. It can also benefit from the expertise of members of the power EE unit like Prog. Garrido.

In short, the ingredients for cross-fertilization do exist and it would be appropriate to offer means to work out some common achievements. Chances that the Indian Government would support such an initiative after the completion of the UNIDO contract are real since, recently, a proposal for acquisition of work stations and appropriate software was accepted. The Council du Tiers Monde could provide also an adequare contribution by providing means for short term exchanges of scientist from both insititutions.

4. Guidelines for future co-operation

The purpose of this proposal is to underline some initiatives that could benefit from the support from both the CSIR (Government of India) as well as the Council du Tiers Monde.

1) Fabrication of prototypes of Application Specific Integrated Circuits (ASICS) for Industrial Electronics Systems designed in one of the institutions or developed under a common research programme.

   This would refer to fabrications within the microelectronique Lab. of UCL as well as to fabrication in an outside silicon foundry. The latter should be considered unambiguously after completion of successful testing of prototypes and the existence of a market has been demonstrated. The cost associated with the fabrication may vary substantially from 12 k$ to 30 k$ per run depending on the number of users (considering both mask fabrication and processing for a similar Silicon Foundry in the U.S.).

2) Exchange of information regarding available microprocessor software developed by CEERI to operate the PWM/ASIC on an actual A.C. motor drive.

3) Collect information on users experiments of the PWM ASIC in order to establish specifications for new systems with improved characteristics aiming at a product that could be used by industry in both countries for applications such as transportation (involving advanced Electric Vehicles using A.C. Motor Drives).

4) Exchange information on Cell libraries for IC design as well as on architectures suited for Industrial electronics. Develop joint efforts regarding ASIC's through student projects.

5) Exchange information on testing tools for evaluation of ASIC's and on the requriements regarding test equipment.

6) Assist CEERI in the choice of work stations and design tool software packages required in order to improve its design turnaround time and efficiency.

7) Enhanced communication between CEERI and UCL by promoting mutual visits of scientists regarding ASIC archtectures, establishment of specifications, etc. as well as requirements regarding the compatibility between Mag. Tape support vehicles, design rules, software packages etc.

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