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SEMICONDUCTOR DEVICES AND ELECTRONIC SUB-SYSTEMS FOR TRANSPORTATION

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INDIA

Technical report: Power semiconductor devices for transportation equipment (Part III)*

Prepared for the Government of India
by the United Nations Industrial Development Organization,
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1. ABSTRACT

The present mission consisted of giving lectures, participating in discussions and initiating experiments. Lectures were given on lithography for VLSI technology, latchup in CMOS and epitaxial silicon substrates, and intrinsic gettering. Discussions were held on 15 HP AC motor drive for electric road vehicles, device specifications as defined by the application, device design, and issues related to processing. Problem area was identified in the alloying step and a number of options and experiments suggested. New masks for the modified 100A darlington with finer geometry have been fabricated. Design work for the 40 mm device has been initiated. Package design and requirements have been established for both 33mm and 40mm devices. Majority of the equipment for large diameter wafer processing are operational.

2. INTRODUCTION

The project is aimed at developing semiconductor devices and electronic sub-system for transportation. This includes four major tasks, which are power devices, hybrid circuits, monolithic integrated circuits, and inverters for the electronic subsystem. The present mission was primarily concentrated on power devices, specifically the issues of the transistor design and specifications for a 15 HP AC motor drive, and related to process development problems for the power transistor fabrication.

The four tasks on which investigation has started are:

Task 1 : Design of 100 A Darlington Transistor
(Nov. 1984 - June 1986)

Task 2 : Fabrication of 100 A Darlington Transistor
(Feb. 1985 - Sept. 1986)

Task 3 : Process Capability for Large (2 inch) Devices
(Nov. 1984 - May 1986)

Task 4 : Design of 300A Darlington Transistor
(July 1985 - Dec. 1986)

3. DESIGN OF 100 A DARLINGTON TRANSISTOR

In order to improve the switching behaviour and thermal stability of the 100 A darlington the emitter finger width has been reduced from 500 /um to 350 /um. The mask layout for the new design has been made and the masks have been fabricated. They are being inspected for defects and errors.

4. FABRICATION OF 100 A DARLINGTON TRANSISTOR

Fabrication of the 100A darlington is hampered due to the unavailability of two key process equipments, namely the alloying furnace and the spin etcher. Their status will be discussed under item 4. Alloying of the silicon wafer to molybdenum disc is a critical process step. The wafer alloying has been done on an equipment which is not adequate in temperature control and flat zone resulting in voids and non wetting of alloyed samples. This has been confirmed through ultrasonic scan method. Hopefully, some of the problem of ambient gas and temperature non- uniformity will be removed with the new furnace being installed.

Following the alloying operation, the fusion needs to be bevelled for edge contouring. This is being done by sand blasting. Due to the unavailability of finer powder initial bevelling was done with 50 /um powder. The bevelled surface was then etched to remove all mechanical damage and then passivated with an organic material. This process resulted in devices with high leakage current. Possible reasons for high reverse leakage current are inadequate removal of mechanical damage, surface contamination by metals (solder) during etching, and microcrack in silicon due to poor alloying. Experiments were made using 27 /um and then 12 /um (preferred particle size) particles. This sequence of experiments was necessitated due to the unavailability of the proper particle size at the time of experiment. All bevelling and etching experiments resulted in devices with high leakage current. At the present, the most likely cause is that the poor alloying process, leaving large areas of unwetted and unsupported silicon near the edge, and the bevelling process as well as stresses due to uneven alloying are causing microcracks in silicon.

The process of removing the sand blasting damage by dip etching could also cause surface contamination that could result in high leakage. This problem will be overcome through use of spin etching which is a relatively clean process, and does not require wafer masking with wax and keeps all dissolved solder metals away from the bevelled surface. As soon as a few adequate quality alloyed fusions are produced attempts will be made to spin etch and passivate the devices using BHEL facilities in Bangalore.

5. PROCESS CAPABILITY FOR LARGE (2 INCH) DEVICES

Significant progress has been made in the installation of equipment for large diameter (2 inch) devices since my last mission in November, 1985. Open tube diffusion, pyrogenic oxidation, and sintering furnaces have been installed and are operational. Tube sealing facilities for closed tube diffusion have been installed and are ready for verification runs. This was made possible by fabricating the tube sealing attachments inhouse at CEERI. The vacuum alloying furnace has been received and the installation to be completed. The operation of this furnace is expected in the April - May time frame. The other critical equipment that remains is the spin etcher, which has been shipped from USA in mid-February. Two important items remain to be added to the facilities. These are a mask aligner and a super Q system for D.I. water polisher.

6. DESIGN OF 300 A DARLINGTON TRANSISTOR

Extensive discussions were held with the power electronics group to establish the device requirements for 15 HP AC motor drive. For the 12 KVA drive, a starting current of 225A and a sustaining voltage ($V_{CE\,(Sus)}$) of 350V are the major requirements of the darlington transistor. Other parameters, such as the base drive, transistor gain, turn off time and thermal impedance were discussed and tentative values established. Protection against surge current is not important because of inductive load. Protection against surge voltage is provided by an external free wheeling diode. The free wheeling diode should be capable of switching on before V_{CE} reaches 400 V.

The removal of charge from the transistor during turn-off is of concern and was discussed in detail. For the removal of the charge carriers rapidly, a negative base drive can be provided through an extra base terminal. This generally needs two base terminals, one is used for turning on the transistor through the darlington pair, and the other for removing the charge carriers from the output transistor by giving a negative pulse directly at the base of that transistor. Alternately, either gold diffusion or electron radiation can be used for fast recovery of the transistor.

Tests on available low current commercial two-base transistors have been planned to evaluate the requirements for two bases.

With these inputs design for a 40mm device has been initiated. The darlington pair will have two base leads. This approach will provide us valuable information on the dynamic characteristics of the transistor. Regarding processing of the larger diameter device, once we have the 100A darlington process optimized it will be a straightforward extension. Of course, all the new equipment must be operational and calibrated.

Package for the 40mm transistor with two base leads has been designed and discussions will be held with the supplier after the author returns to USA. No difficulty in obtaining the package is anticipated.

7. MATERIALS, DEVICES AND EQUIPMENTS

In the previous report it was mentioned that Wacker Chemitronic was reluctant to supply the epitaxial silicon wafers needed for transistor fabrication. This problem has been overcome and Wacker has accepted the order for the material. Information on the 33mm and 40mm device packages has been obtained and an order will be placed in the near future.

A number of darlington transistors and GTO's have been identified for purchase to provide the power device and power electronics groups with experience in testing and using these new devices for inverter applications. These devices have been ordered.

Previously, a mask aligner was identified for the facilities from Oriel Corporation. Unfortunately, they were unable to provide the capability for back slide alignment. A new supplier has been identified and quotation and literature will be obtained as soon as the author returns to USA. Quotation is also needed for the DI water super Q system polisher from M/s Millipore, U.S.A. and will be expedited by the author.

8. LECTURES AND DISCUSSIONS

During this mission the First National Symposium on Microlithography was held in CEERI. A plenary address was given on lithography for VLSI technology.

Lithography requirements can be broadly divided into two categories. One is for the high volume memory and microprocessor circuits, where millions of chips are required and the other is for the application specific integrated circuits needing only a few hundred chips.

Optical lithography should offer adequate resolution (0.6 /um) and throughput for volume production of IC's through 1990. Significant research and development activities are in progress on

both equipment development and resist technology. Optical lithography could continue to dominate down to 0.25 /um through improved optics (eg. vacuum uv-illumination and immersion lenses) and photoresists. Resist technology (eg. trilevel resist) thus far has played a major role in bringing optical lithography to the submicron range.

For low volume custom IC's and for fabrication of masks, electron beams are the optimum choice. Exposure cost with electron beam is at least an order of magnitude higher than it is with optical method, and therefore electron beams are restricted to tasks where high cost can be offset by other savings in the process.

X-ray lithography offers the best advantage over other methods in that the exposing radiation is not scattered in the resist or diffracted. This leads to higher aspect ratio resist patterns than can be produced with optics, and no proximity effect as with electrons. Significant equipment development activities are in progress and X-ray lithography could dominate in the range of 0.25 /um and below for high volume production.

A lecture was given on materials and process issues of CMOS technology. CMOS is emerging as a leading VLSI technology because of its inherent advantages such as low power consumption, high noise margin and higher packing density. One of the main drawbacks of CMOS technology is its susceptibility to latchup. Latchup can be prevented by either completely isolating the two transistors of the CMOS structure and/or providing a shunt path for the carriers to flow through a highly conducting substrate. Various developments in the substrate materials were discussed. These include Czochralski silicon with denuded zone for active region and oxygen precipitation for intrinsic gettering, epitaxial silicon, silicon-on-sapphire technology, and silicon on insulator (SIO) technology. Current status of these technologies and development trends were discussed. The processes and equipment for these emerging materials were outlined in some detail.

A lecture was given on intrinsic gettering, an important technique that provides substrates for high quality silicon (or epitaxial layers) for VLSI as well as for power devices. Oxygen content and its distribution in silicon are critical to the intrinsic gettering process. Method of achieving this in Cz silicon using magnetic field was discussed. Various heat treatment cycles for effective oxygen precipitation were outlined. Processes for the growth of defect free epitaxial silicon, and evaluation techniques were discussed. Some of the useful measurements are impurity profile by spreading resistance technique, carrier lifetime by MOS, and non destructive surface photovoltage method for diffusion length measurement.

A discussion was held on isolation techniques for VLSI, in particular, for CMOS structures. Some of currently used isolation techniques are the LOCOS process and the trench isolation. LOCOS process uses selective oxidation for the growth of field oxide and is not scalable to submicron dimensions. In addition, one has to be concerned with inversion layers under the field oxide and its prevention. Trench isolation is scalable to submicron dimensions and is done by etching a trench between two adjacent transistors by reactive ion etching (RIE). Methods of trench etching, its effects on defect generation and some process optimisation were discussed. A number of new methods of isolation techniques, such as, selective epitaxial growth (SEG), silicon on insulating substrates, and other futuristic concepts were discussed.

9. TASK SUMMARY

The masks for the improved design 100A darlington having, 350 /um wide emitter fingers have been fabricated. These masks are being inspected for defects and possible errors.

In the processing area major problems with alloying and the subsequent etching of the bevelled surface remains. With the installation of the new alloying furnace and the spin etcher these problems are expected to be solved rapidly.

For the fabrication of large area wafer majority of the equipment, such as, diffusion, oxidation, and sintering furnaces, vacuum tube sealing, bevelling and lapping facilities are all installed and operational.

The device and package requirements for the 300A darlington have been established, and work on the initial design for the transistor has begun.

10. CONCLUSIONS AND RECOMMENDATIONS

Progress has been made in the modified design of the 100A darlington and a set of new masks have been fabricated. Fabrication work is being delayed due to laboratory renovation and missing key pieces of equipment that are to be either installed or received. A major problem in alloying step has been identified to be the presence of extensive voids. This may also be causing problems in down stream steps, such as,

bevelling and etching. Devices fabricated to date show excessive leakage probably due to poor alloying, particularly in the device perimeter.

The problem would hopefully be solved on installation of vacuum alloying furnace and spin etch machine. The power device work has slipped by about 6 months due to non-availability of this critical equipment. Design for the 300A darlington has been initiated with inputs from the power electronics group. Packaging requirements have been established and a modified package has been designed.

The recommendation essentially remain the same as in the author's last report. These were related to:

1. Super Q system for DI water.
2. Mask aligner to handle large diameter wafers with provisions for back side alignment.
3. Assured source of epitaxial silicon wafers.

Actions on these items will be taken as soon as quotations can be obtained from equipment vendors. On the supply of epitaxial silicon wafers it is recommended that a second source of the material be established.

It is also recommended that the alloying team be strengthened to overcome the problems associated with alloying, so that, this does not become a bottle neck in the future.