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DP/ID/SER.A/697
14 May 1986
ENGLISH

15561

SEMICONDUCTOR DEVICES AND ELECTRONIC SUB-SYSTEMS FOR TRANSPORTATION

DP/IND/84/015

INDIA

Technical Report: Fabrication Technology of LSI Circuits*

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of K.C. Saraswat

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1. INTRODUCTION AND BACKGROUND

This is a summary of my UNIDO sponsored visit to India, primarily to CEERI, Pilani during the summer of 1985. The purpose of this visit was to enhance the capabilities of CEERI in the aree of the fabrication technology of MOS integrated circuits.

Under the TOKTEN scheme funded by UNDP I had visited India during the summer of 1981. The bulk of my time was spent at CEERI, Pilani. During that visit I worked with the entists of CEERI and installed a 5 m silicon gate MOS technology. I took the test masks and details of the fabrication technology from Stanford and was successful in teaching the basic principals of the silicon gate MOS technology to the CEERI scientists. We were able to fabricate some 5 m NMOS devices successfully.

During the time between the two visits I had continued correspondence with many CEERI scientists. They kept me posted regarding their progress and requested help in many areas. I sent them relevant information whenever it was possible. It appeared from their progress that they were ready to update the fabrication technology. As a result at the request of CEERI I decided to go back during the summer of 1985 to educate them regarding the recent progress in MOS technology and perhaps install a 2 m MOS technology.

I arrived in Delhi on August 22, 1985. Despite the Delhi office of CEERI worked very efficiently (especially Mrs. Bhalla) and arranged for me to have a briefing at the UNDP office the next day. The UNDP people were very efficient and they immediately arranged my trip to Pilani and the remainder of the stay.

I reached Pilani on Sunday, August 25 and stayed there untill September 17. I spent the next four days in Delhi and left for USA on September 21. The next section will desc be the technical activities, main achievements and a critique of my visit.

2. TECHNICAL ACTIVITIES

Before reaching CEERI I had communicated to Dr. Amarjit Singh that I would like to work with his group to teach them the details of the fabrication technology of 2 m NMOS and CMOS integrated circuits. He had provided me with a list of equipment which they had acquired subsequent to my 1981 visit. He had also discussed the details of their progress in his several visits to Stanford University. He had a chance to see our new research laboratory in the Centre for Integrated Circuits, meet with many researchers and have discussions. The intent was to show him the construction details of a world class facility and the research which goes on in it. Several other CEERI scientists visited our laboratory for the same purpose and gained valuable knowledge.

vUpon my arrival I found that mentally the people were anxiously waiting to work with me. I had detailed meetings with Dr. G.N. Acharya, Dr. Amarjit Singh, Dr. W.S. Khokle, Dr. Lahiri and their scientific staff. I reviewed the status of their 5 μm MOS fabrication process and suggested some improvements. The next step was reviewing the status of the fabrication facility. I found that subsequent to my 1981 visit they had acquired lots of high quality new equipment and the facility also had some marginal improvement. The maintenance of the facility, however, was a different story.

Problems related to cleanliness of the environment were encountered, e.g., the photolithography area had inadequate ventilation and high humidity. In some cases immediate availability of spare parts to do maintenance was not there, and hence equipment was not operational. In some cases the equipment vendors had not kept up their end of the bargain and therefore the equipment was not functioning as it should. Availability of some chemicals was a major problem in some cases. Small quantities required by CEERI do not get any significant attention of some suppliers.

IC fabrication requires a large number of steps done in sequence and if one of them falters the progress is halted immediately. To be able to have a meaningful turnaround time the facility should be fine tuned to its best ability. I was hoping to fabricate two to three batches of NMOS and CMOS devices during my stay. I had brought with me details of 2μ NMOS and CMOS fabrication technology. However, I quickly realized that given the time constraint of about four weeks and the status of the facility it will be difficult to achieve my goals. As a result I decided to teach the details of the technology to the CEERI researchers by giving formal seminars followed by detailed discussions. This was carried out in parallel with the experimental effort. Following topics were covered in the seminars.

Research at Stanford University Center for Integrated Systems

The Center for Integrated Systems is a unique form of university, industry and government co-operation that promises to have a significant impact on the microelectronics and computer information revolution. *Integrated Systems* refers to the confluence of the applications, algorithms and architectures of information science and engineering ("computers") with the materials, processes and devices of physical science and engineering ("microelectronics").

A major goal of the Center is to bring together representatives of these disciplines to work on a variety of vertically integrated projects of fundamental interest to the microelectronics and computer science communities.

Trends and Limits of ULSI

Ultra-large scale integration is governed by a hierarchical matrix of limits. The levels of this hierarchy can be codified as:

- Fundamental
- material
- device

- circuit
- system

Each level includes both theoretical and practical as well as analogical limits.

Theoretically, thermal fluctuations impose a fundamental limit of several kT on switching energy. Scattering limited velocity and critical electric field establish a material limit on switching speed. Avoidance of punchthrough sets a device dimension limit. CMOS power-delay product defines a circuit limit, and clock skew represents a systems limit on ULSI. For conservative design margins, circuit limits project MOSFET channel lengths in the 0.4-0.2 μm range.

The totality of practical limits is described by three parameters which collectively measure the overall rate of progress in ULSI:

- minimum feature size
- die area
- packing efficiency (i.e., the average number of transistors per minimum feature area) of a complex chip. Approximately one billion transistors in a single silicon substrate (or Gigscale Integration) are projected by the 2000.

To forecast beyond this time, it is helpful to study history as a guide to forming analogical limits. Today, iron, steel ingots, cast steel engine blocks and automobiles epitomize the mature industrial revolution. Silicon, doped single crystal ingots, integrated circuits and Computers are a parallel progression of the modern information revolution. An intriguing analogy between structural and electronic materials suggests a very long term high level of utilization of Si integrated electronics as well as rapid advances and volume applications of complementary technologies.

Effects of Scaling of Interconnections on VLSI Circuits

Continuous advancements in technology have resulted in integrated circuits with smaller device dimensions and larger area and complexity. The overall circuit performance has depended primarily on the device properties. However, the parasitic resistance and capacitance associated with interconnections and contacts are now beginning to influence the circuit performance and will be the primary factors in the evolution of submicron VLSI technology. Results of theoretical modeling to assess the impact of these factors on the evolution of integrated electronics will be discussed. Recent work on materials technology involving aluminum and its alloys, polycrystalline silicon, refractory metals and their silicides was reviewed in the subsequent talks.

Physical and Electrical Properties of Polycrystalline Silicon Thin Films

Chemical-vapor-deposition of polycrystalline silicon films and their physical and electrical properties was discussed. Effects of deposition parameters, doping and high temperature processing on grain size and orientation, carrier concentration, carrier mobility and electrical resistivity, was discussed. It was shown that electrical conduction is controlled by dopant segregation, carrier tunneling and trapping at grain boundaries.

Effect of hydrogenation on the electrical properties, such as, resistivity and possible implications for SPI device fabrication was discussed. Influence of grain boundaries on thermal oxidation and dopant diffusion in polycrystalline silicon was discussed.

Al and its Alloys for Interconnections and Contacts

Aluminum has been and continues to be a widely used material for IC metallization. This talk will discuss the properties of Al and how its interactions with silicon determine the properties and reliability of Al interconnects and Al-Si contacts. The limitation of pure Al that restrict its use in VLSI are overcome by using Al-alloy with Si, Cu and Ti. The effects of these alloying elements on the properties and reliability of Al interconnects and contacts were discussed from the point of view of hillocks, electromigration, junction spiking, dry etching etc.

Refractory Metals and Silicides for Interconnections

During the last decade, polycrystalline silicon has been used as one of the materials to form MOS gate electrode and the associated interconnection layer in integrated circuits. However, for VLSI applications its high resistivity (>500 $\mu m\ \Omega$ cm) degrades the circuit performance because of large RC time delays and IR voltage drops in the interconnection lines. A large amount of work is being done in the area of new and innovative materials, processing technology and device structure involving refractory metals and their silicides to overcome this problem. In this talk, first, the necessity of this approach was justified by theoretical modeling and then various approaches being pursued were reviewed. A comparison of the properties of the silicides from the point of view of their compatibility with IC fabrication processing were done. Various techniques to deposit these materials and the resulting quality of the films were reviewed. Low pressure chemical vapor deposition technology was discussed in detail. Properties of the CVD films were reviewed. Problems impeding the incorporation of refractory materials in manufacturing of ICs with multilayer Interconnections were addressed.

Refractory Metals and Silicides for Contacts

Theory of metal/silicide contacts to silicon will be briefly reviewed. Problems of Al contacts to silicon will be again briefly reviewed. Problems of Al contacts to silicon will be again briefly described. Alternative contact schemes involving refractory metals (e.g. CVD tungsten) and silicides (e.g., Pt Si) for VLSI in light of an improved understanding of the metallurgy of Al and Al-alloys with silicon were discussed.

A review of the test structures to measure contact resistance and extract specific contact resistivity will be done. The MOS salicide technology (silicided source drain) will be discussed. Finally, techniques to planarize contacts using CVD of tungsten were discussed.

All these talks with the exception of the first talk were video recorded for further dissemination in India. The video recording was done in separate sessions. The seminars were spaced a few days apart. In between discussion sessions were held with various researchers on the topics covered in the seminars as well as other topics pertaining to the MOS technology. Some of these "other topics" are

- Plasma etching
- Ion Implantation
- Chemical Vapor deposition
- Thermal Oxidation
- Test Structures and testing equipment
- Photolithography
- Design rules
- Facility construction, especially clean rooms.
- Safety requirement
- Equipment maintenance

During these discussions many interesting and important issues surfaced where I was able to help them.

Meanwhile the experimental fabrication work continued, however, there were numerous delays because of one or the other reason and finally it hit a major roadblock when the low pressure chemical vapor deposition (LPCVD) system to deposit polycrystalline silicon thin films developed a big leak in the exhaust which could not be repaired in time without compromising the safety of the operators.

Since the fabrication of the MOS test chip came to a standstill I decided to spend the rest of my time in educating the young researchers the finer details of the individual step of the CMOS technology. This involved conducting well defined small experiments and discussing the results obtained. In most cases I gave them a large number of references of papers published in the literature. After reading the papers these young and highly enthusiastic researchers always came back with a barrage of sharp questions leading to further discussions. This kind of interaction continued very successfully 'till the end of my stay and I believe I was able to give them very valuable guidance to continue further work to update their technology.

I had similar discussions with the senior staff, however, they were more global. Stanford Center for Integrated Systems (CIS) was used as a role model for these discussions. At Stanford we went through two stages:

- Renovation of a 15 year old facility in 1980 to allow us to go from MSI to LSI level.
- Installation of a new facility by 1986 for VLSI and ULSI.

Since I was involved in the upgrading of the old facility and planning and installation of the new facility in CIS and now I do research in it, I was able to give them firsthand information on how to plan a new facility and how to run it. As I have pointed out earlier Dr. Amarjit Singh has visited our facility several times. Through him I was able to relate to others with ease.

This information should help CEERI tremendously in planning and execution of

their future activities.

During this stay I visited many local educational institutions and gave seminars at the Birla Higher Secondary School and the Birla Institute of Technology and Science. As a result of these seminars a large number of students as well as the teaching staff came back to have more discussions, largely involving technological trends in India and abroad. Typically these took place in the evening and at times stretching into the late hours of night. Through these discussions I was able to reeducate myself on the problems faced in the area of high technology by a developing country. This gave me fresh insight into the reasons for the slower progress rate of India in the area of high technology. As a student in India I had lots of similar discussions but now I was on the other side of the fence and hence was able to have a better objective outlook.

On September 17, I left Pilani and spent the next four days in Delhi. One day was spent at the Indian Institute of Technology. I had discussions with Prof. A.B. Bhattacharyga and his group on their activities. During the subsequent three davs I met Mr. Shivraj Patil, Minister of Science Technology and Electronics: Prof. Yashpal, Secretary, Department of Electronics: Secretary, National Microelectronic Council and Dr. S. Varadarajan, Director General, CSIR. The purpose of these meetings was two fold: first, to learn from the top policy makers the future direction of electronics and India and second, to assist them in decision making process. This interaction was very fruitful. As a result of the keen interest I had taken in the problems of India in making advances in electronics during this and previous visits. I was asked to meet Mr. Rajiv Gandhi, the Prime minister of India during his visit to Washington D.C. on October 24, 1985. During this meeting I made specific suggestions regarding the future policies involving electronics in India. Much of my information was derived from this trip and the 1981 trip to India. As a result of my meeting with Mr. Rajiv Gandhi and a subsequent meeting with Dr. Sanjeevi Rao, Mr. Vivendra Mohon and Dr. Nirurkar a joint scientific advisory committee on microelectronics has been set up and I have been appointed a member of it. Through this Committee I expect to help India in the area of Electronics.

In conclusion through this visit to India I was able to help her on many fronts involving electronics and I hope to continue that in the future.

3 Recommendations

Pilani is too isolated from the rest of the world from the point of view of physical as well as electronic communications. As a result the flow of information as well as people is impeded between CEERI and rest of the world. For a fast moving high technology field like electronics this should not be tolerated. Therefore my first recommendation is that physical communication should be improved. An air link between Delhi and Pilani will cut down the travel time from half a day to less than an hour. CEERI should consider running an air conditioned minibus on a regular basis between Delhi and Pilani, perhaps a daily service. We run a similar service between Stanford University and University of California at Berkeley and we have found it to be very effective. Since CEERI people have to run to Delhi for every little thing, why torture your staff by making them use the run down overcrowded buses of the public transport system?

Electronic communication between Pilani and the rest of the world needs improvement. I tried to make a telephone call from USA to CEERI for many days to straighten out my visit however, I could not get through to Pilani. I was fairly easy to get through to Delhi. Somehow the electronic communication has to be improved if things have to move faster and efficiently at CEERI. Perhaps the Indian government should tie up CEERI to the Delhi telephone exchange permanently using a microwave satellite link. The things which take days or weeks could take only a few minutes. While I was in Pilani I tried to arrange a visit to the Semiconductor Complex, Chandigarh, however, due to slowness of the communication I failed.

The facility at CEERI needs major improvements. Although they now have a good amount of modern and sophisticated equipment, however, the facility itself is not up to par. If their major objective is to do research in VLSI and provide India the state of the art technology they should improve the buildings, the clean air, clean water, guaranteed electricity supply. This will require a major expense on the part of the Indian government, however, it is the only way to do research in a technology which changes totally every five years.

The availability of spare parts for equipment maintenance and chemicals which have to be purchased outside of India is too slow and at times consumes too much time and effort on the part of the scientists. The Indian government should make the procedures more streamlined to improve this. At times the chemicals have arrived at CEERI after their shelf life has been nearly over. Spare parts could be stocked in ample quantities to avoid delay in procurement after the need arises. As it is the research is difficult to do because of many other problems, these things make the life of scientists even more difficult.

There should be more interaction between the CEERI scientists and the rest of the world. I have rarely seen a scientist from CEERI in major conferences held in USA, Japan and Europe. In the same conferences I see increasing numbers of Koreans and Chinese. I am not sure how to provide funds for that, but attending conferences is one of the best ways of getting state of the art knowledge in a field CEERI must cover at least a dozen conferences per year outside India. At the same time the CEERI scientists could visit sister organizations and meet other scientists and make contacts. Otherwise the only information they get is by reading journals which is at least two to three years old by the time it reaches them.