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DESIGN AND PRODUCTION OF MICROELECTRONIC SYSTEMS AND COMPONENTS*

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Introduction

Electronics are often defined as electrical engineering of small currents and voltages as opposed to heavy-current engineering. In this case, electrical energy does not have to do the mechanical work but exchange signals and messages to control systems. After engineering replaced human or animal manpower by electrical energy, control functions and data transmission have today turned electronics into a key industry of modern industrial societies. There is no branch of commerce which does not use electronic products to a greater or lesser degree. As to the gross national product, e.g. the segment of electronics in the Federal Republic of Germany, this was 2.5 per cent in 1982 or 39 billion DM (Deutschmarks) out of 1,600 billion DM when expressed in absolute figures.

Microelectronics, or rather the technology of integrated circuits, is the branch of electronics with reduced classical circuit components, transistors, resistors and capacitors, assisted by silicon technology to less than 1/1000 of its area or to less than 1 millionth of its volume, and/or weigth. In 1982 consumption of microelectronic components in the FRG was 1.3 billion DM, which is only 8 per cent of the total returns of the electronic industry. Although this is a small part of the total, it underlines the quality, performance and success of modern products. Not only is computer technology being influenced by microelectronics but increasingly also communications systems.

There are two characteristics for microelectronics:

- Circuit components are cheap compared to the selling price of the system made by these components;
- Because of its light weight transport charges do not play a ignificant part.

The market for components is a free one, i.e. the world market. At present the production of components is concentrated in a few countries, mainly in East Asia and the United States of America. The European segment of highly integrated silicon circuits production is minimal (only a few per

cent). The two above-mentioned characteristics do not exclude the existence or development of an electronics industry. This general development is of great importance to the Third World as well. It is considered necessary to build up an indigenous industry since the steady advance of information technology cannot be stopped.

With regard to the European economy, an increasingly important part of the gross national product is expected to be spent on importing information systems. It is anticipated that in the early nineties the net import of information technology will exceed the net import of primary energy. Since components or ICs can be obtained for a low price on the world market and profit mainly begins at the system level, attention should be directed especially at developing systems. The adjustment of systems to the special demands of the market offers a chance for finding products not offered by the big companies of the industrialized countries.

This report examines the different possibilities of realizing indigenous electronic systems, and/or components, from laboratory development to production. The different design methods and techniques will be analyzed with regard to tools, investments and cost.

1. DESIGN METHODS FOR ELECTRONIC SYSTEMS

An electronic system receives signals from the environment, processes them with the help of the information stored in the system and finally sends corresponding answering signals.

In measuring and control circuits, as well as radio and television systems, input and output signals are mainly analog electrical signals that are continuous current and voltage values.

In computer techniques nearly all signals are digital, i.e. a collection of zeros and ones. Additionally there are systems which send the analog signal through an analog-digital converter, processes it digitally and finally transforms it back into an analog signal. For the engineer the demands are different, depending on the system to be developed, whether analog or digital.

The analog system in general requires a well-founded knowledge of classical electrotechnology. These circuits are used where analog tasks have to be realized at low prices or at very high circuit speeds. Today, however, digital signal processing is preferred to analog processing because it does not require such a profound knowledge of electrical properties. The signal which exists as a number after AD-conversion can be further processed in a digital circuit with the help of standard methods. For many applications high-frequency effects such as noise and cross talk are not important so the design of these systems will in general be easier than the design of analog systems.

Digital systems are developed in two directions. The signal can be processed either in the direct way by a specific circuit adjusted to the problem, or by a microprocessor. Signal processing will then not be determined so much by the circuit as by the software of the processor. Implemented systems are somewhere between these two limits, which can also be called the hardware or software solutions.

Every method has its pro's and con's. Pure analog processing results in the fastest signal flow. Conversion from analog to digital and the subsequent processing by a specific digital circuit is at least one order of magnitude slower. The software solution with the help of microprocessors can be even slower by a factor of 1,000. The opposite can be said as regards flexibility. A very important advantage of software solution is the adaptation of the circuit to different tasks by only changing the programme.

Digital circuits are the most important ones in solving todays' electronics problems. In general, however, a system often contains all three components, and the corresponding design centre has to be familiar with each of the three methods.

1.1 Hardware

In the development of prototypes the strength of the laboratory will be determined by two factors: on the one hand by the more or less extensive component stock and on the other by the possibility of assembling these components to circuits ("breadboards"). Nearly every system begins as a breadboard, i.e. a laboratory assembly made with the help of standard ICs.

The software required for the microprocessors is written with the help of special development systems. Also very important today are the programmable devices, ROMs and PALs which can be programmed by the developer with the desired attributes. The third factor for the laboratory is the equipment for measuring and testing. A component stock for digital application costs about US$2,500; a microprocessor development system can be obtained from US$20,000; the measuring equipment should be estimated at no less than US$40,000. The minimum equipment for such a laboratory, without the microprocessor development system, amounts to US$10,000 while the most desirable equipment including analog developments, amounts to US$50,000. Annex I indicates the necessary equipment.

Laboratory assembly and the production of a few systems involves the same process, but for a greater production volume suitable production methods have first to be developed. The design of printed circuit boards becomes necessary, including the design of custom integrated circuits, depending on the number of pieces. For this the rule of thumb is the higher the production volume, the more custom ICs will be required to reduce the number of components and therefore the costs. Custom ICs are the most economic option if at least 1,000 systems are to be produced. Nonetheless one or more printed circuit boards must always be developed. This task has to be accomplished either by the design centre itself or by one of the specialized companies. In general, industrialized countries have a specialized company to develop the printed circuit boards according to the circuit diagram furnished by the customer, at a price. Production and mounting of printed circuit boards can be carried out by a third company which also often tests the components and PCBs.

Chapter 2 is dedicated to the problems of breadboarding and printed circuit board design, whereas Chapter 3 deals with the problems of custom design. In Chapter 4 the necessary CAD tools are discussed while in Chapter 5 the problems of producing ICs are tackled.

1.2 Software

Software equipment for a design centre will be required to undertake two different tasks, i.e. the development and testing of microprocessor programmes and computer-aided circuit design. While in general for the first task

special microprocessor development systems will be installed, for the second, general purpose computer systems ranging from personal computers to large main frame computers may be preferred. These standard computer systems solve the three main tasks: the printed circuit board design, the programming of ROMs and PALs and the development of custom integrated circuits.

For some years now dedicated computer systems called "workstations", are being considered which are able to solve some, if not all of the tasks and which could be locally installed in the office of the designer.

As this study is concentrated on the methods of microelectronics hardware development, the equipment of microprocessor laboratories need not be discussed further. However, it must be pointed out that a microprocessor laboratory is a necessary part of the design centre for electronic systems. Development systems for normal microprocessors can be ontained for about US$20,000, but special software (which emulates the behaviour of microprocessors) is available for standard computers.

Programmes and computers for circuit design are described in Chapter 4., sub-divided according to simulation and layout. Layout is the physical realization of the circuit, whether as a printed circuit board or as an integrated circuit. Software to programme the ROMSs and PALs will be treated in section 2.2 after describing the components. This software is not very complex and can be carried out on every standard computer system.

2. BREADBOARDING AND PRINTED CIRCUIT BOARD DESIGN

Between the specification of a digital circuit and the reproducible hardware prototype is the circuit design. Criteria for design are not static but are closely linked to the innovation of component technology.

Nowadays the development engineer has a number of possibilities when selecting a specification. He can choose between different technologies (bipolar, MOS), between a modular assembly with standard components or a special IC design. Design itself also has a spectrum from simple "paper design" to complex timing analysis. In future, so-called silicon compilers will automate the whole design process.

In considering the wide span of alternatives for design, not only technical but economic aspects have also to be considered by the development engineer. Development costs such as cheap reproducibility, power consumption, independence of component manufacturers, testability, etc. all play an important part.

The following section deals with current possibilities of design technique in the laboratory. In practice, these do not have to be examined in isolation as they follow one another without interruption.

2.1 Design with standard logic families

The standard logic components are monolithic ICs within the range of SSI (small-scale integration) and LSI (large-scale integration). On these ICs functions such as logic operations, multiplexers/demultiplexers, latches, registers, buffers/drivers, adders, comparators, complete ALUs (arithmetic logic units), memories and simple bit slice processors are integrated.

The component determines the functions and cannot be modified. By connecting these standard components a prototype is constructed and tested. This process is called breadboarding. Later on, for production purposes, a special PCB (printed circuit board) is designed which is equipped with the chosen ICs.

At present, breadboarding is the most common design technique. Above all, it is well-suited to small- and medium-sized companies, as apart from a well supplied stock of standard components, only a few cheap tools are required to develop, construct and test digital circuits (section 2.3).

The wide dissemination of these design techniques depends above all on the large number of available ICs which exist in bipolar and MOS technology, mostly in CMOS.

TTL is the most famous circuit family. TTL means transistor-transistor-logic , a circuit design technique that works with the help of a unipolar supply voltage of +5V. Texas Instruments is the dominating manufacturer of this family (SN54/74 serial). With about 800 different functions at present, this serial represents industrial standard. Characteristics of the functions

have been adopted by nearly all manufacturers so that the user is able to work out the implemented functions independently of the chosen manufacturer (e.g. 7,400 = quadruple 2-input positive NAND gates).

During the last decade the TTL family has been considerably improved by using Schottky diodes which avoid saturation of transistors - a requirement for fast switching. The standard TTL family has now been completely replaced by low power Schottky (74LScc) and Schottky (74Sxx) families which on the one hand stand for lower power dissipation and on the other for shorter gate propagation delay. These types follow advanced low power Schottky (74LSxx) and advanced Schottky (74Sxx) ICs which have even shorter gate propagation delays.

Other manufacturers have developed their own processes for the TTL family which in all cases are aimed at reducing the product of gate propagation delay/power dissipation and at increasing the output current (fan-out). The Fairchild company has thereby developed the FAST-TTS serial which in the case of identical functions shows the shortest gate propagation delay of the TTL family at present. Companies like Motorola, National-Semiconductor, Valvo/Signetics, SGS, Siemens, etc. all have their self-developed TTL families which, in some cases, differ from gate propagation delay and power dissipation but are however compatible to one another. This can be applied to the individual families (LS, ALS, S, FAST etc.) as well as to the different companies.

The following table shows the different TTL families, their typical gate propagation delays and power dissipations. For more detailed specifications the corresponding data manuals (references 1 to 6) should be used.

Table 1. Data issued by Fairchild and Texas Instruments refer to a NAND gate at 25 degress Centigrade and 5V

TTL family	t-delay in ns type	max	Pstat in mW	td * Pstat
Standard	9	19	10	90
74LS	9.5	15	2	19
74S	3	6	19	57
74FAST	3	5	4	12
74ALS	4	11	4	16

Another bipolar family, mainly known for the construction of main frame computers, is the ECL family (emitter coupled logic) which works along the principle of current mode logic. This family achieves even shorter switching times than the TTL series. Available functions can be compared favourably to those of the TTL series, and are nearly as extensive.

The dominating manufacturers in this field are Fairchild and Motorola who offer components with gate propagation delays of 0.75ns (NOR gates, F100K serial, Fairchild). Logic levels and supply voltages of the ECL family differ to those of the TTL family. However, they cannot be easily combined within a circuit. In this connection ECL manufacturers offer special converter ICs.

The following table shows the technical data of ECL families. For further information see the detailed data and design manuals (references 7 to 9).

Table 2. Typical data of gate OR/NOR at 25 degrees Centigrade and -5,2V (with the exception of F100K: -4,5V) supply voltage

Company	ECL family	td in ns	Pin mW
Motorola	MECL 10000	2	25
Fairchild	F10K	2.2	26
Fairchild	F95K	2.0	24
Motorola	MECL 3	1.1	60
Fairchild	F100K	0.75	40

Further bipolar circuit families are the DCTL (direct coupled transistor logic) - and RTL (resistor transistor logic) families which are not used today.

Apart from the bipolar circuit families there are families with the same function in MOS technology, mostly in CMOS. Digital ICs in CMOS, compared with bipolar ICs, have the advantage of a very small power consumption, a high noise immunity and a wide temperature range.

Because of the rapid improvement of CMOS technology during the last five years, CMOS circuits are increasingly penetrating the field of bipolar circuits. With the introduction of HCMOS circuits (high-speed CMOS), a partial repression process of LS-TTL ICs has begun. These HCMOS families, which can be obtained from all large manufacturers, carry out the same functions as the LS-TTL ICs. With the advantages of CMOS, LS-TTL ICs can be directly substituted for HCMOS ICs if they are similar in function. Both can also be integrated in the circuits.

Due to the rapid innovation in HCMOS technology, it is expected to penetrate the domain of bipolar circuits in the near future, particularly for high-speed applications. Fairchild and Integrated Device Technology have announced TTL compatible HCMOS families to replace the fastest TTL components with the help of typical gate propagation delays of 1-2ns at a power consumption of a hundred times less (FACT of Fairchild). For more detailed information see the corresponding data manuals of the semiconductor manufacturers (references 10 to 11).

For some years ICs with logic functions in GaAS technology will be offered for sale on the market. At present the fastest gate propagation delays can be achieved in this technology (40-250ps) at a considerable increase in price when applied to bipolar or CMOS circuits due to the use of another material (gallium arsenide instead of silicon). The fast switching time also indicates the limits of conventional design techniques, as shown in the following:

In the first design phase the engineer designs the circuit diagram on the basis of the available functions. He then chooses the ICs for circuit configuration according to the characteristics: gate propagation delay, functions, fan-out and power consumption. The circuit must be laid out so that can also work with the worst-case conditions of IC manufacturers.

After functional reliability of the circuit has been guaranteed, the second phase begins with the optimization of IC exploitation. The aim is to use as few ICs as possible in order to keep power consumption, connections (printed-wiring conductor lengths) and fault liability at a

minimum. Therefore, the best possible use of the functions on individual ICs are examined. If necessary, individual functions must be replaced by others (e.g. an AND gate by a NAND gate and an inverter), or if possible, ICs with a higher integration density have to be applied. Even available package styles are an important factor relating to surface utilization. With regard to economic optimization the rate of price/efficiency of comparable ICs (HCMOS compared to LS, FAST to S) has to be considered. Availability is also an important aspect, i.e. whether a second source exists for the used ICs.

In the third phase a prototype of the circuit is assembled. For this either the solderless wire wrap technique can be used or a prototype PCB can be manufactured directly. At the final test the circuit will be examined to see whether it works in a real environment. Real environment in this context means the connecting wires between the ICs which give the technique additional capacities, inductances, propagation time and cross talking.

For circuits with a system frequency greater than 25 MHz these parasitics can no longer be ignored. These problems also show the real disadvantage of bread-boardings and of the PCB technique. Complex high-speed applications are therefore not boardable from a system frequency above 150 MHz. The capacity alone of an IC pin and the signal propagation time of the connected line can result in a signal propagation delay to the order of one gate propagation delay, as to GaAS ICs a multiple of them. Circuits with very high system frequencies should therefore be designed only on a chip.

Demand for such a high-speed application is increasing rapidly. Minicomputers will attain this limit within the next five years and because of this everyone is anxious to raise the packaging density of PCB designs in order to minimize parasitics. This may be attained on the other hand by smaller package styles of the ICs. Thereby dual-inline packages will in a few years' time be replaced by SMD packages (surface mounted devices) which are smaller by a factor of 2-3. On the other hand, parts with small switching times will be laid on the chip.

Within the above-mentioned limits, the design of digital circuits with conventional logic components is at present the most widespread and cheapest procedure.

For high system frequencies there is a need for chip design. This also applies to very high production volume applications.

The transition to user design chips may by achieved gradually. The PAL-devices in the next section are examples of this.

2.2 PAL devices

The PAL family (programmable logic array)[1/] was first introduced by the Monolithic Memories company in 1977/78 (reference 12). The devices are programmable ICs which can be classified according to their functionality between PROMs (programmable read-only memory) and FPLASs (field programmable logic array).

Solutions to problems with the help of programmable logic devices were introduced to circuit design techniques some time ago. High integration density of these devices makes it possible to replace several MSI and SSI chips by only one of these devices and therefore economize on printed circuit board surfaces. The flexibility won by programme capability also permits a widespread coverage of the fields of application with only a small stock.

As any combinational logic circuit can be described as an AND/OR function, PAL devices are normally considered to be equivalent to other programmable logic types. In recent years however, type variety and integration density of PAL devices have increased to a potential which compares these devices positively to other logic types.

With the introduction of one-chip latches and feedback of output signals in the programmable AND matrix, PAL devices are not only applied in combinatorics but also in the range of sequential digital circuits as, for example sequence control. With a family of 45 different PAL types at present and a complexity of between 150 and 5,000 gate equivalents a wide field of

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1/ PAL is a registered trademark of Monolithic Memories Inc.

application is made available. In the meantime PAL devices will also be manufactured by the AMD (reference 13), National Semi-Conductor, Texas Instruments (references 1 and 2), Harris and Altera. They can be obtained in TTL, ECL and CMOS technology. CMOS versions of Altera can, in addition, be erased by ultraviolet light.

The rather long propagation time of programmable logic devices (propagation delay input to output) has been considerably improved. TTL PAL devices which are manufactured on the basis of advanced Schottky technology show in its fastest version a typical delay time of 7,5ns and a maximal one of 15ns. ECL PAL devices even show a typical time of 3ns and a maximal one of 7.5ns. These times represent gate propagation delays of four gates on the chip (input driver, AND gate, OR gate, output driver).

With the introduction of PAL devices a corresponding software aid has also been offered in the form of the programme PALASM. The FORTRAN source code of PALASM has been reprented in data manuals and can be obtained free of charge for the majority of PCs in object code. Input format of PALASM are Boolean equations which can be compiled into PAL programming code. Furthermore, PALASM contains the possibility of logic simulation. The nominal characteristics of the logic circuit have therefore to be laid down by the designer in a function table. PALASM checks the logic equations to see whether they are equivalent to the function table.

Meanwhile the second generation of design software can be obtained on the market, such as for example PALASM2 of Monolithic Memories Inc., LOGE of the University of Karslruhe (FRG) and ABLE of Data I/O. This second generation mostly offers a more comfortable user state and allows a problem-oriented input which partly reaches the quality of a silicon compiler. By that, a function description which is independent of implementation will be entered in the LOGE programme and the user is able to decide by means of the evaluation whether PAL or FPLA will be used for implementation.

Together with the above-mentioned points, PAL devices represent a link between conventional logic families and semicustom ICs. The advantage as opposed to standard ICs is that several standard ICs can be combined in one PAL IC, despite the high-speed applications, without loss of performance.

Compared to semicustom ICs the advantages of PAL devices are low development costs and quick availability of desired functions. Between input of the functional description and the programmed device an average of 30 minutes is required, contrary to the four months for semicustom ICs of the same complexity. This is also one of the reasons why PAL technology is progressing more towards the semicustom range of ICs.

Initially PAL devices were mainly used to combine badly used ICs in standard IC designs with one PAL; now a two-level-design-technique has been developed from this. Core functionality of a circuit can be developed straight away at the computer by circuit diagrams in the form of PAL equations. The PALs resulting therefrom are assembled with the help of additional standard ICs on the total circuit and tested by breadboarding. Errors in circuit design are improved by exchanging programmed PAL devices rather than by difficult wiring of connections.

With this process a very short development time between circuit specification and a reproducible functional pattern can be obtained at considerably low development costs. The required number of devices, and therefore the required area, will be reduced, as opposed to standard IC design by a factor of 2-4. Additionally, PAL devices dispose of so-called security fuses which avoid a reading out of PAL after programming and represent an effective copy protection.

With regard to high speed and development costs of circuit design with PAL devices, this is an important alternative to design on a semicustom basis or to conventional logic devices. For a large production volume the advantage in price of semicustom ICs is however effective.

2.3 Layout of PCBs

Layout is the conversion of a circuit diagram to a two-dimensional intersection-free multilayer. According to the complexity of the circuit there exist one or more layers. These layouts will be copied at a scale of 1:1 on special exposure foils serving as masks for printed circuit boards. Two layers will be combined into one printed circuit board (coating on both sides). The connection lines will be copied directly on the base material,

pertinax or expoxy resin, or etched on to unused copper. To obtain PCBs with more than two layers several two-sided PCBs will be stuck or pressed together. Drilling for the components will be made with the help of a CNC drilling machine.

The most time consuming process is the creation of the layout. Starting from the tested circuit diagram, the layout can be divided into three steps: the placement of components; the routing of connections on one or more levels; and the creation of a film pattern which can be copied.

These tasks can be done manually or with the aid of a computer. For the purely manual method, persons with sufficient knowledge and experience will be needed in order to minimize the parasitics caused by the PCB compound technique.

The longest process is that of routing, i.e. the intersection-free design of signal connections on one or more levels. The layouter has to lay every signal line taking into consideration the electric boundary conditions. The number of layers and width of the lines is a matter of choice. So-called finest lines have a width of 1/60 of an inch. For such small structures routing patterns have to be created on an enlarged scale of 1:2 or 1:4. On transparent foils the connections are fixed with the help of special opaque foil. Drillings for the terminal pins of the components are marked. These foils are reduced in size if necessary and copied onto the film patterns which are then sent to the PCB manufacturer. The material for this process costs about DM 200 to DM 400 per layout. Manpower time will be between one to four months per person, depending on complexity and experience.

Manual layout generation of highly complex circuits can often take as long as circuit development, therefore computer-aided layout systems are necessary to reduce time and effort.

Such layout systems have automatic programmes at their disposal to perform component placing and routing in a short time. Additional specifications, such as maximal PCB lengths, can also be taken into account. The user can at any time interfere in the dialogue mode and can specify critical paths by hand with the help of a graphic input.

Furthermore, modern layout systems generate the magnetic tapes needed for CNC drilling machines of PCB manufacturers as well as the data formats for so-called photoplotters which directly expose the film patterns for PCB production. Additional programmes alsc generate the control data base which are used in assembly automats of production lines.

Without this fast layout realization and data processing which corresponds to the needs of production engineering, a prototype design on a PCB basis cannot be conceived. The use of PCB software requires that the designer enters his circuit diagram at a graphic workstation in the form of a schematic entry or a connection list. According to this data base the layout will be generated. In this way, redesigns can be made possible very quickly and documentation and filing of circuit designs have a high standard. Prices are between DM 350,000 and DM 750,000 for complete PCB systems (DM 350,000 for the Calay V03, DM 750,000 for the Racal Maxi on a VAX computer).

2.4 Assembly of prototypes

To assemble a prototype in the wire-wrap technique, special wrapping tools, wire and wrap sockets for the ICs are required. The wrapping tools are a motor-operated wire-wrap connection which isolates the special wrap wire in one operation and winds it round the terminal pins of the wrap sockets. With the help of a special unwrapping tool these connections can again be untwisted. The wrap sockets are soldered onto the laboratory cards. It is recommended that a two-sided copper laboratory card be used in order to obtain a ripple-free power supply. The supply connections of the ICs are soldered directly. In all cases, a wrapping of the power supply must be avoided.

Measuring intstruments and a power supply are necessary in order to test the prototype. For the measuring of static factors a multimeter is used. An oscilloscope is used for the dynamic measuring of signals. This should have at least two channels and two trigger time bases. The frequency bandwidth of the oscilloscope depends on the logic family which is used and on the system's frequency. For circuits with LS TTL components the minimal bandwidth should be 50 MHz; for FAST and S-components it should be 100 MHz; and for ECL designs it should be at least 250 MHz. To register singular or random events there are special oscilloscopes to permanently store the signals. For complex

circuits with a lot of signal lines, as for example microcomputer circuits, so-called logic analyzers are used to indicate and store the different signals. Modern logic analyzers have up to 64 channels and reading rates of up to 500 MHz.

In addition to the qualitative registration of events, event counters are used for quantitative evaluation which can accommodate digital events up to frequencies of 150 MHz to some million MHz.

With the exception of the logic analyzer, the above-mentioned measuring instruments can also be used for analog design techniques. Signal generators are required in addition. For the different applications, a multitude of specialized measuring instruments exist for analog techniques. Additional equipment for an analog laboratory include tools for veroboard connection techniques.

In order to install and test PAL devices the same equipment as for conventional logic devices is necessary. To develop and programme the internal functions of a PAL, however, additional equipment is needed. The programming of devices is done by special units which are manufactured by companies such as Data I/O, Monolithic Memories Inc., Kontron, Scantec and Digilec. They differ according to the number of PAL types which can be programmed by them. The PAL programmers are loaded by a host system with a special code. This host system can, in its simplest form, be a standard PC with a floppy disc memory. On this computer the PAL equations are edited in the form of Boolean algebra and stored on a floppy disc in the form of files. The floppy disc is also the backup medium. The text files are compiled with the help of PALASMs or the more powerful programmes such as CUPL, LOGE and ABLE, into the data format of the PAL programmer used (often JEDEC format). This data will be transmitted over a serial conduction (RS 232). If a simulation table has been added to the text file a logic function test can also be applied to the programmed PAL device.

Annex I lists standard laboratory equipment according to the fields of application, including costs.

3. CUSTOM DESIGNED INTEGRATED CIRCUITS

The active components required for the breadboad or the printed circuit board are more or less highly integrated silicon chips which were developed in the design centres of the semiconductor manufacturers. These components were designed as custom circuits (see section 3.4). The costs of such developments range from about US$50,000 to some millions of US dollars, depending on complexity. This only becomes profitable if a million pieces can be sold. Therefore some years ago it became obvious that the user had to be satisfied with standard components. The few custom applications reaching a high production volume had been directly arranged with the manufacturer. With the availability of semicustom ICs in recent years new design and production methods were introduced which permit the drastic reduction of the entrance price for the user. The cheapest technique, with gate array designs (section 4.2) presently begin at development costs of about US$15,000. If considerable complexity is involved, a price of approximately US$60,000 can be expected instead of about one million US dollars for full custom design. For the flexible standard cell method, about US$40,000 has to be regarded as the minimum price. In general, this leads to lower chip prices than the gate array solution. Plotting development cost versus the number of pieces reveals the following results for the design of electronic systems:

- Prototype design, breadboarding and small production volume can be carried out with standard components. The fixed functions of standard logic families and the programmable functions of ROMSs and PALs may be used;

- A higher number of pieces beginning with some hundreds and going up to several thousand permits the additional use of gate arrays;

- The standard cell process is the cheapest from about 10,000 pieces upwards. However, between automatically designed gate arrays and standard cell design there is often no difference in cost. Other attributes such as flexibility will then become decisive;

- The classical full custom design does not become economical under some 100,000 pieces.

For the production of electronic systems printed circuit boards have always to be developed. For large numbers of pieces this printed circuit board will always contain highly integrated standard components, e.g. microprocessors, RAMs and ROMs. The part of custom ICs on the printed circuit board should not exceed an upper limit of about 25 per cent. It is therefore essential that every design centre to be build has at its disposal the methods and possibilities of printed circuit board techniques described in Chapter 2. User designed silicon chips are only a part of an electronic system.

3.1 Technological boundaries

The possibilities of the user designing his own silicon chips at a reasonable price are relatively new and closely associated with the gate array technique. Customer conditions have improved in recent years whereas the economic background for the manufacturer has been aggravated (section 3.1.2). Considering a chip from the complexity of a 16 bit computer with 10-15,000 gates, the development time for the chip design alone has decreased from two or three years to six months and the expense from perhaps four million US dollars to one tenth. Today the technologies offered are numerous and CMOS technology will dominate in future. For this technology alone 80 per cent of the market for custom ICs has been forecast for 1990.

3.1.1 Technologies

The technologies offered to the customer do not generally differ from those of the families of standard components described in Chapter 2. The bipolar process exists with the npn and pnp transistor and the MOS process with the n and p channel transistor. Production lines are offered for the analog and digital circuits which are specialized in the corresponding application.

Classical bipolar technology is well suited for analog circuits. Typical fields of application are radio and TV circuits, control circuits for electrical machines as well as electronic appliances for cars. The minimal geometric resolution is about 7.5 micron which is considerably above the present optical exposure limit of 1-1.5 micron. The number of components on one chip rarely exceeds 200 transistors or 1,000 components altogether which

corresponds to a maximum silicon area of about 25mm^2. The standard components of this technology are operational amplifiers and related circuits. At best LSI complexity will be achieved but most of the applications are in the range of MSI. The technology can be obtained as gate array, standard cell and full custom design. In Europe, about 10 manufacturers are at the customer's disposal.

Two digital circuit families are implemented in the same analog bipolar technology. The most important one is the TTL family with the low power Schottky improvements mentioned in Chapter 2 which is already a specialization of the standard analog process. The standard logic chips manufactured by these technologies are the most wide-spread components, but they will be increasingly replaced by CMOS ICs. The mini- and midicomputers of the 'seventies were provided with TTL circuits and as a result of the progress in CMOS technology it is expected that after 1990 TTL will nearly disappear from the semicustom market. In Europe each of the three design methods (gate array, standard cell and full custom design), are presently being offered for TTL by about 10 manufacturers.

Concerning mixed analog-digital bipolar applications, I^2L technology has been approved for the digital part. Packing density is one order of magnitude higher than TTL, however the switching speed is slower by the same factor while the power consumption per gate is still lower than that of MOS circuits. The technology however does not have an important share of the market; about five manufacturers exist who offer all three design methods. Standard ICs do not exist.

At present, the fastest of the logic families in silicon is the bipolar ECL logic with a switching speed of up to 0,25ns. ECL logic can be obtained in standard components and also in each of the three design methods. This technology is particularly offered as gate arrays by about 10 manufacturers. The ECL technology is three times faster than the best MOS process. Forecasts for 1990 show that this will be the only bipolar technology in the field of digital custom circuits which will not be replaced by CMOS, but the high price and complexity which is nearly one order of magnitude less when compared to CMOS, reduces the expected portion to 15 per cent.

In the range of bipolar technology there are also many more specialized processes, e.g. for high breakthrough voltages or for low noise components. They can also be partly utilized as gate arrays. Due to their small market share they will not be discussed further.

Only two technologies have prevailed on the market, i.e. nMOS and CMOS in both variants (metal gate and poly silicon gate), out of the different MOS processes presented in the course of time, but these control the digital circuits market all the more. In 1985, as a result of considerable sales in TTL, the bipolar and MOS market shares remained nearly constant.

The nMOS technology as opposed to CMOS has the advantage of a higher packing density and more speed, but it also has the disadvantage of more power dissipation. Today it is still the technology with the largest and most complex ICs; Microprocessors in particular, will be manufactured by this method. In full custom design 400,000 transistors per chip have been reached. For custom ICs the standard cell technique will be offered apart from the full custom design. nMOS are not suitable for gate arrays and are hardly ever used. This also applies to standard components. About 10 manufacturers offer standard cell trechniques and full custom design.

In recent years, CMOS technology has made a triumphant advance. Its standard components are beginning to replace the fastest TTL components (Chapter 2). Its power consumption is much lower than that of TTL and lower than that of nMOS. CMOS circuits do not take steady state current. The CMOS circuits are the ideal technology for gate arrays. Nearly all of the approximately 40 silicon manufacturers throughout the world have CMOS arrays on offer. Today these arrays are the technology to be chosen for digital applications up to a switching time of one ns. Some manufacturers list about 30 different CMOS arrays in their catalogues in order to meet customer demand.

For analog applications the MOS technology is inferior to the bipolar one and in this case only full custom design and/or standard cell methods are possible. The standard components in analog CMOS are confined to analog-digital and digital-analog converters.

A new technology, BIMOS or BICMOS, tries to unite the possibilities of bipolar and MOS technologies. Up to now this technology has not been offered as a process of semicustom ICs.

To start up a microelectronics activity technologies should be restricted to a few methods. The following preferences result from this viewpoint with regard to semicustom designs. The main technology is CMOS for probably 80 per cent of all applications. Standard bipolar technology should be taken into consideration for consumer electronics and perhaps ECL also for fast ICs in the field of communications or computer technology.

3.1.2 The manufacture of silicon chips

Different process lines for bipolar and MOS technology may exist in a silicon foundry alongside one another. In order to find optimal conditions for analog circuits other process parameters than for digital circuits are necessary. An optimization of analog as well as of digital parameters results in an additional line. This is also applicable if only one parameter, e.g. the breakthrough voltage, should be optimized. In addition to this, every process will be different according to the minimum tolerable line width. Therefore, in semiconductor factories throughout the world perhaps several hundreds of different manufacturing lines can be found today.

Such a process is called a line which for some time has constant characteristics and which is reproducible. The closer the limits for reproducibility of parameters, the more safely the developer can design a circuit and the higher is the yield. Conversely, the designer tries to make the circuit as insensitive as possible to the unavoidable process fluctuations, but this is often only possible in restricted cases and in any case it prevents the optimal use of the silicon area. The transfer of designs out of one company line to a nominal identical process of another company cannot in general be done because of differences in parameters. The design has to be fitted to the new conditions.

The manufacture of an IC is a complicated process involving about 10 to 15 main steps which can be subdivided into 100 to 150 single operations. Since a lot of these operations are not completely understood, the transfer and/or the sale of a line to another company is very difficult. In orde to

keep the risk small, the old process should be copied as precisely as possible. This means that the same equipment should be used down to the last screw. Even if complete information and support by the vendor and enough specialists are provided, the process may not work at the very beginning due to environmental conditions, i.e. atmospheric pressure, humidity, temperature etc. The minimum time for adaptation is from six to nine months. If the equipment is a little different and if the employees are not so experienced, at least two years should be anticipated for development up to the start of production.

Technological progress is fast. This is particularly marked in the reduction of the minimal line width which, for example in MOS has been reduced in the last five years from 5 um to 3 and 2 um, and recently even to 1.5 um. The latter level will only be achieved by a few companies, mostly in Japan. A newly established silicon foundry will have considerable difficulty in beginning an economic manufacture because the technology chosen may already be out of date before production starts .

A small factory has a volume of about 500 silicon wafers which per day will be put into the line in, for example 20 slots with 25 wafers per slot. Thus about 50 to 100,000 circuits can be manufactured per day. However this takes mass production for granted which should at least be partly price stable. Over the last few years, however, the semiconductor market has suffered considerable price and demand fluctuations. A fall in prices of 20 to 25 per cent per year over a longer period for the same function is considered normal. The most evident fluctuations as well as the fall in prices can be shown in the case of memory chips. Whereas production of 64k chips in the USA has started, almost all one megabit memories will be produced in Far-Eastern countries. Evidently the US companies have given up the development of this field of production. The competition for generally usable mass ICs is regarded as enormous. But on the other hand, a lot of semiconductor manufacturers survive with the help of special products manufactured under a monopoly or with less competition and more stable prices.

Under these circumstances, a newly established silicon foundry will probably not start with the mass production of ICs for economic reasons. An advantage would be to develop an electronic system with standard components and semicustom ICs from the varieties offered on the market. The start of an indigenous silicon manufacture should only be made if the demand for locally made chips warrants it.

While ignoring these initial difficulties for an indigenous silicon production, the situation from the point of view of the developer has improved recently. The prices for standard compcnents as well as for silicon chips developed by the customer have steadily decreased, whereas the achievable complexity has steadily increased. The developers' possibilities are no longer restricted by a foreign production of components, unless political conditions forbid access to the same semiconductor manufacturers.

3.2 Gate arrays

Both of the semicustom methods, the gate array and standard cell design, are not far from the design methods with standard components, as explained in Chapter 2. As to computer simulation, they only differ by the various names of the components in the library and by the values of the propagation delay time. The functions are also not always identical in each technology.

A breadboard or a printed circuit board can be developed in hardware and by simulation, a gate array only by simulation. The breadboard can later be improved; for each redesign of a gate array the manufacturer needs the same time and the same expenditure as for the first design. Therefore, an essential difference between a gate array and a bre: er price of the prototype development. With gate arrays the c) times higher, but the device is much smaller and can be manufactured more cheaply later on.

In this chapt r the digital CMOS gate array is discussed, as well as the fast ECL and analog transistor arrays. Each of the three arrays are manufactured out of prefabricated silicon wafers, the so-called masters, for which the manufacturer has made all process steps, with the exception of the metallization of the top. The transistors are thus fixed into a position. By designing metal lines the customer connects the transistors with each other to the desired functions. The metal lines are 2 um, i.e., very small and therefore it cannot be mounted directly on the silicon wafer. The customer needs a design tool to work on a scale perhaps 200 times larger. This enlarged picture or layout has to be reduced to the original scale. This is done by the manufacturer using machines with light or electron beam exposure systems to produce the masks corresponding to the dimension of the wafer.

This mask will then be projected on the silicon wafer, as in phototechnics. After several stages of development the desired metal lines are generated on the wafer surface (Figure I).

According to the breadboard nearly every function can be manufactured by different routing of the transistors of the gate array. There is an advantage in price of the gate array as opposed to the full custom IC (section 3.4). The reason for this is that the gate array masters can be made by mass production at a low price and can then be stored. Individual wafers are processed on demand and at the request of the customer. For the metal surface only one mask is required which can be manufactured and transferred to the master within a few days. A disadvantage of this process is that often not all of the available transistors can be used resulting in a poor exploitation of the silicon surface compared to adapted full custom circuits. This increases the price of the chip, but this only plays an important role if the number of pieces is very high. The costs for prototype development to be paid to the manufacturer for a gate array are only about 10 to 20 per cent of the costs for a full custom design, the development and production time often being reduced to one third.

The design of a gate array starts with the simulation. The customer obtains a library with 50-100 elements from the manufacturer which corresponds to the basic functions of the standard components. Each element is characterized by delay time which describes how much time the outputs need to respond to changes at the inputs, furthermore by a numerical value for each input, called the "load" factor, and another value for the output, called the "driving" factor. If in the logic diagram an output is connected to one or more inputs, then in the simulation programme the load factors will be summarized for all the inputs concerned. By multiplying this sum by the driving factor of the output, the propagation delay time of such a connection between the elements can be obtained. The logic simulator correctly takes all the thereby calculated propagation delay times into account. The designer has now to decide whether the time behaviour of the circuit still shows the expected result. The manufacturer often specifies typical fluctuations of the propagation delay times. The design must work within these limits, that is it must meet the "worst case" conditions.

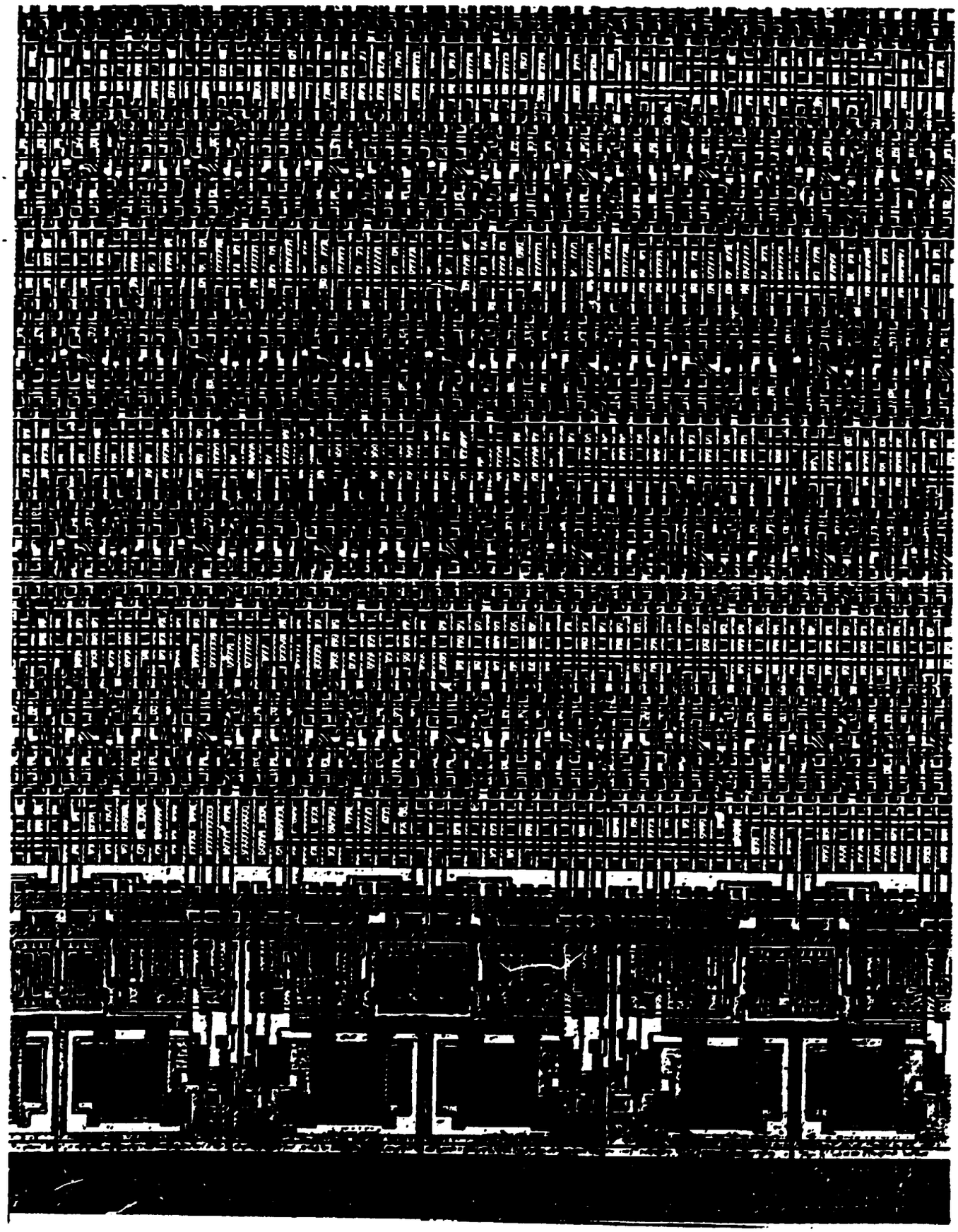

Figure I: Part of a CMOS gate array

This simulation, with exact propagation delay times, is called timing simulation. The many runs require about one month for 800-1,000 gates on a computer with about 1 MIPS (million instructions per second) (e.g. VAX 11/750 made by Digital Equipment). This can linearly be continued for a higher number of gates if the circuit is modular. For 6,000 gates a development and simulation time of half a year must be expected. The result of the simulation is a list which contains the used library elements and the connection of its inputs and outputs, the so-called "node list".

The manufacturer can make the metal layer(s) by using only the node list, but in order to test it afterwards he will still need the "pattern block" where all input and output signals as functions of time are to be found. A special test machine should be controlled by it. The input signals are applied to the chip under test and the resulting output values are compared against those desired. A reliable manufacturer also uses this patter block for his own control simulation of the custom design. He thereby compares the timing behaviour before and after the layout if realistic values for the delays caused by wiring capacitances are known.

The layout or the geometric design of the connection lines can be done manually or automatically by computer programmes by the customer or manufacturer. An approximate rule is that 1,000 gates can be wired by hand in about one month, 2,000 gates in about three months. It is obsolete to route more than 2,000 gates manually. As automatic routing is beginning to become predominant due to the possible complexities of up to 20,000 gates, the design of a gate array mainly consists of a good "timing" simulation and a good pattern block to test all gates, if possible. Only switched gates can be tested. The calculation of used gates is made with the so-called fault simulation.

If the layout is automatically made by the manufacturer, as is usual nowadays, the design will be reduced to generating the node list and the test pattern block. This, however, is just as necessary as the development and testing of a printed circuit board. It is therefore correct to state that, as mentioned at the beginning, gate array and printed circuit board development is not nearly so different in the design process, but this does not mean that a printed circuit board design can be transferred to the gate array on a scale

of 1:1. Because of the different libraries and testability, the gate array circuit will normally be changed by 30 per cent against the printed circuit board with the same functions. Since the manufacturer can guarantee a 100 per cent performance of the node list and the test pattern block, it is usual to expect that perhaps 90 per cent of all gate array designs will work at the first try.

The hardware and software which is necessary for simulation and layout generation is listed in Chapter 5. The following paragraph is dedicated to the technological possibilities, costs and to the different manufacturers.

According to a US company (LSI-Logic), Fujitsu is the leader in the gate array market, followed by Motorola and LSI-Logic. Therefore the CMOS family of Fujitsu will be shown here as being typical of the present state-of-the-art. Figure II. shows the CMOS gate array families sorted according to minimal line width and complexity. The importance of the line width for speed is shown in Figure III. The necessity of also offering RAMs on the chip leads to the subdivision of Figure IV. Figure V shows the most complex offer by Fujitsu with a line width of 1.5 micron. 20,000, respectively 10,000 gates and 12k RAMs will be obtained on a chip of about 144mm^2. 220 pins are possible, the switching time being about one ns and the access values of the RAM about ns. Indigenous 16-bit microprocessors, including the registers, can be designed using this. The price for the prototype devlopment to be paid to Fujitsu is DM 33,000 for the VH array with 2,000 gates. The chip costs about DM 40 for a minimum order of 200 pieces. Thus the minimal prototype costs are DM 41,000. For an array with 4,000 gates and a 2k memory in VHCMOS the minimum costs increase to DM 60,000. The largest array of 20,000 gates reaches DM 250,000. The single packaged chip then costs DM 500. The last example demonstrates the progress of the technology, with an unbelievably large chip area of 144mm^2 and with a cost of DM 250,000 for prototyping, whereas to develop a full custom IC of this complexity costs several million DM. Three years ago only full custom was possible in this complexity range.

The arrays of the other three Japanese manufacturers NEC, Toshiba and OKI are in the same order of magnitude, both in complexity and in price. The leading HCMOS company in the USA, LSI-Logic, buys masters from Toshiba and

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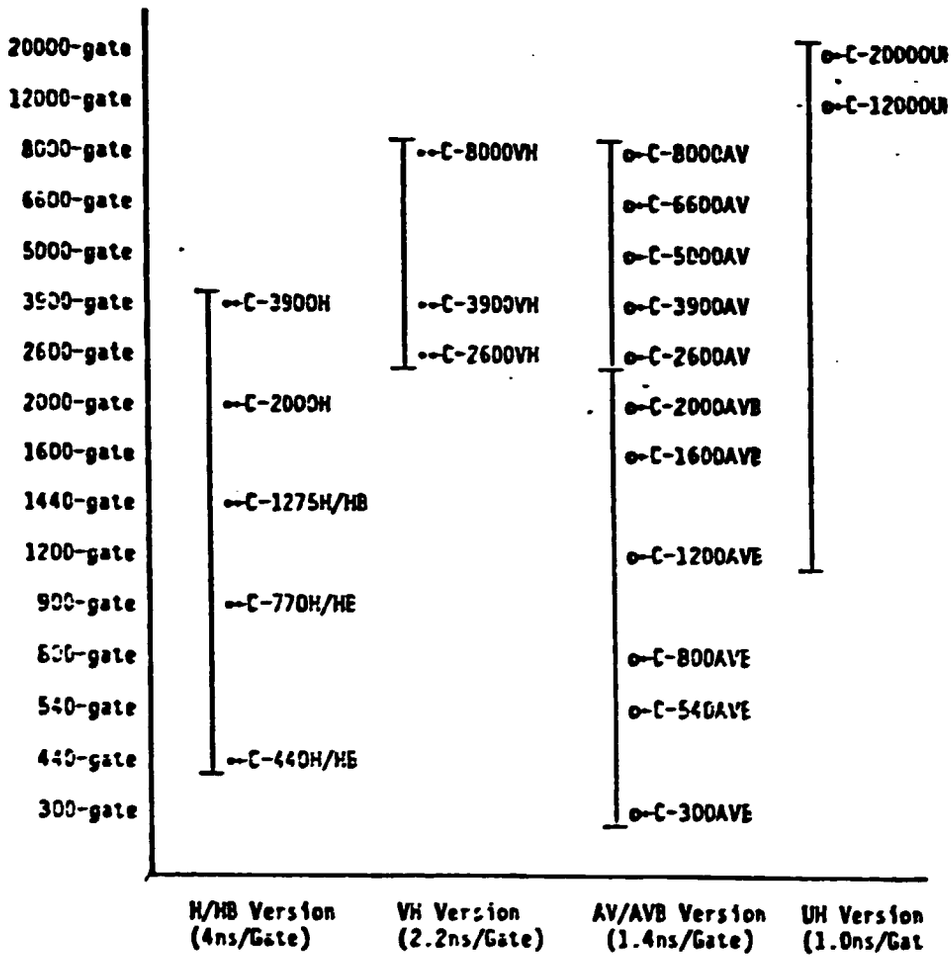

Figure II: Gate array family of FUJITSU

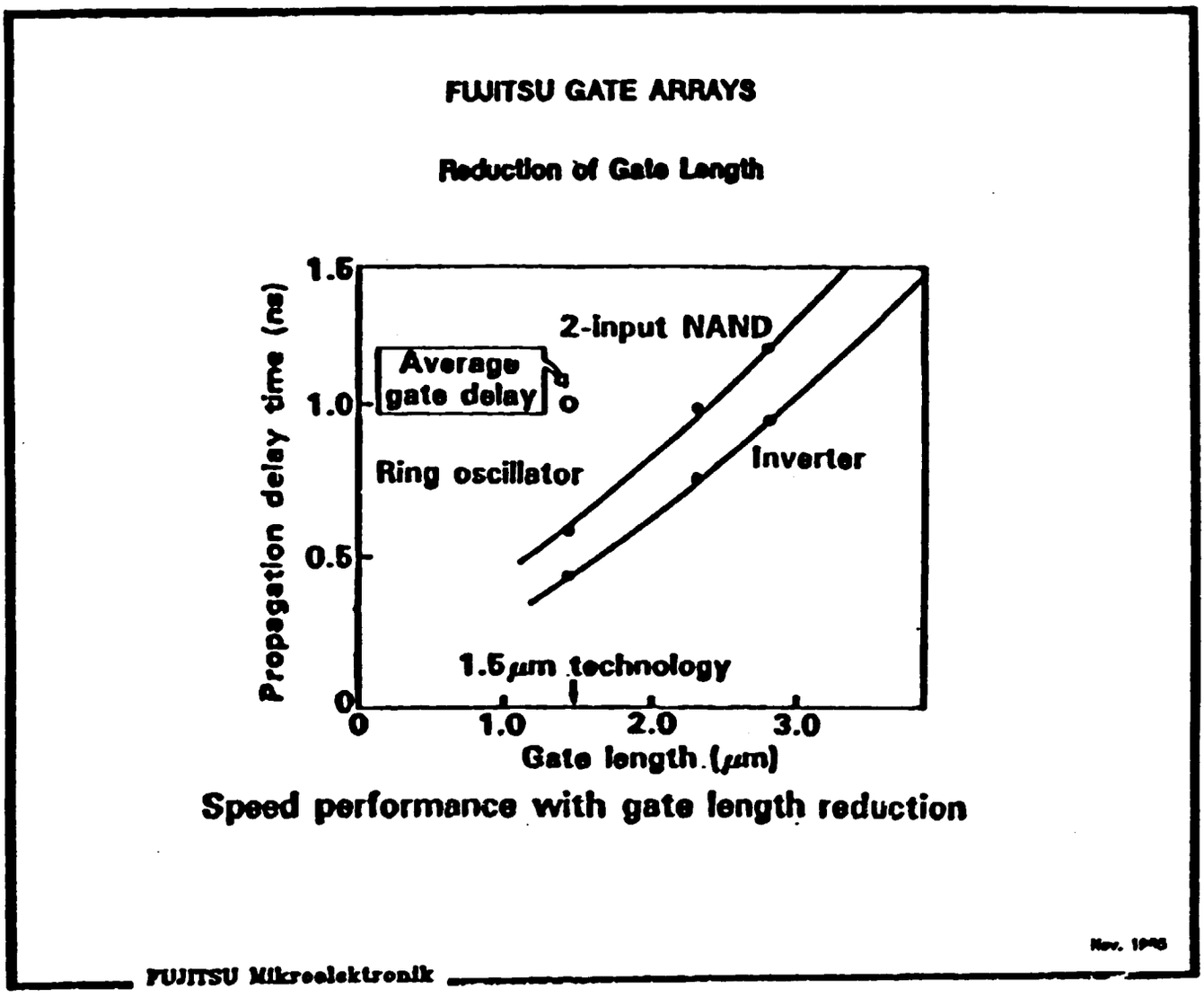

Figure III: Switching speed vs. line width

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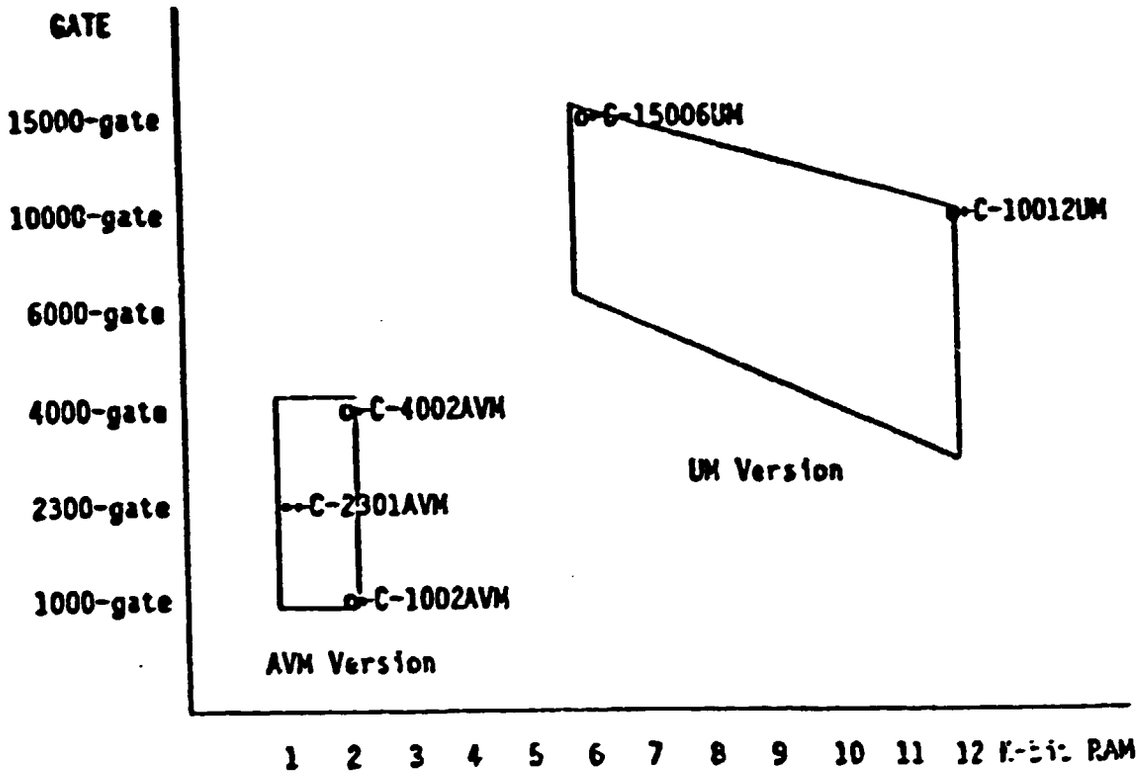

Figure IV: CMOS gate arrays with RAMs

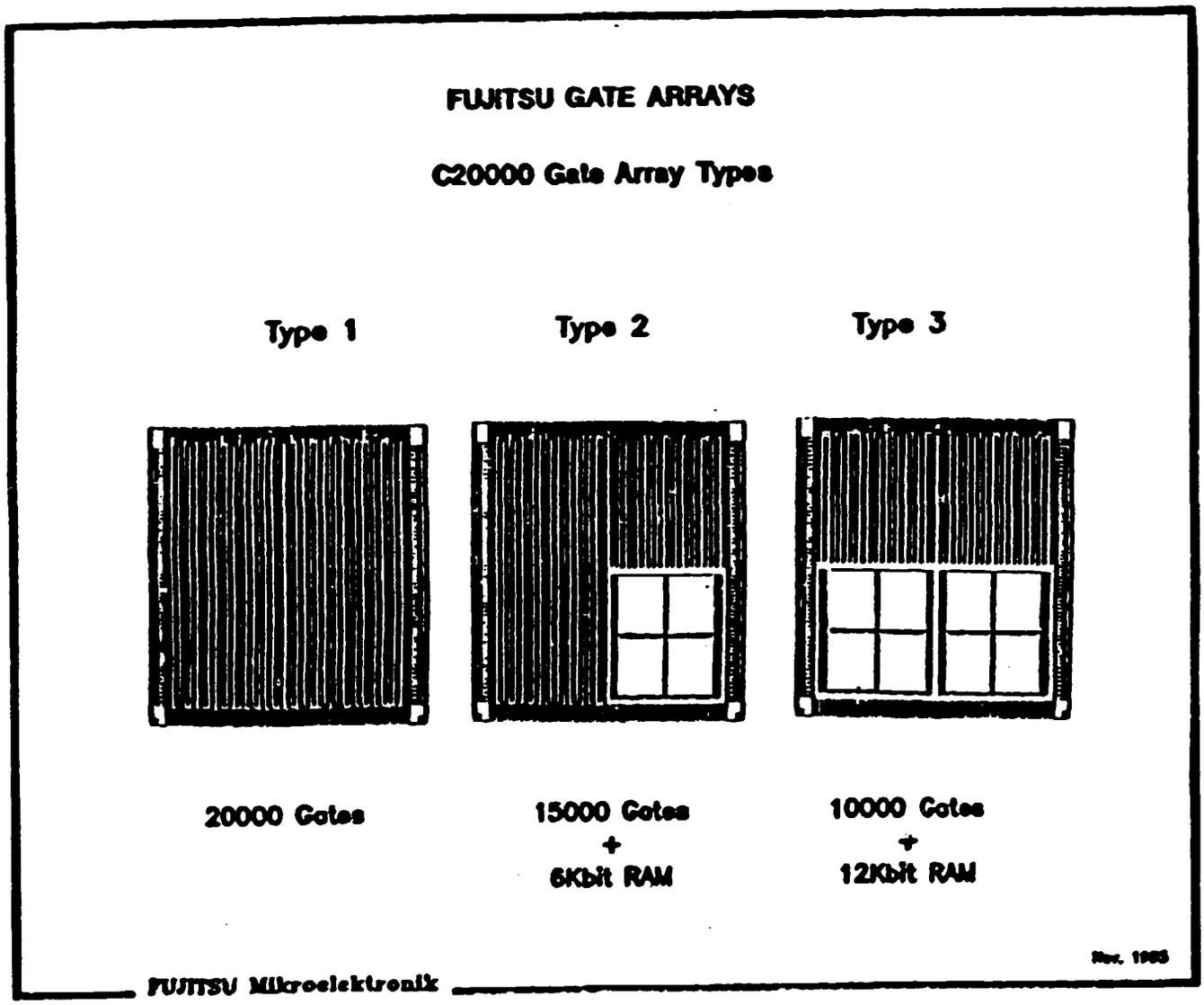

Figure V: Top complexity of today's gate arrays

only manufactures the two-layer metallization on its own. This demonstrates the superiority of the Japanese, not only in the field of memories but also in that of gate arrays.

Annex 2 lists about 20 manufacturers from Japan, USA and Europe without giving details. As most of these companies offer CMOS arrays of up to 6,000 gates and thereby cover more than 90 per cent of today's applications, discussions with all these companies are interesting. For example 1,000 gate arrays at present cost about DM 15,000 for the prototype design and DM 15 for the packed ICs, if 1,000 pieces are ordered.

There is heavy competition on the market. For the CAD tools in Chapter 4 it transpires that the customer should not confine himself to one manufacturer alone. The design software should be suitable for many manufacturers in order to achieve the best prices.

Apart from the CMOS arrays which dominate the market, only the field of ECL (Emitter Coupled Logic) will be discussed due to its present and future importance. From the semiconductor companies mentioned in the Annex, especially US companies such as Motorola and Fairchild should be mentioned, but Siemens and Thomson are also comparable in quality. The competition in this market is lower than that for CMOS. Therefore entry prices are considerably higher - about DM 100,000. The typical delay time lies between 0.25 and 0.5 ns. Systems and/or ICs can be developed up to a clock rate of 400 Mhz. Circuits of this sort are used for the transmission lines with glass fibre cables as well as for fast computers.

The ECL arrays reach complexities of about 4,000 gates with design rules of 1-2 um. Layout will normally be done automatically with interactive preplacement and corrections. ECL arrays are perhaps less suitable as a first project, as the set-up of the corresponding printed circuit board will pose considerable problems which can only be solved with the help of "hybrid" techniques. Due to high-frequency effects the methods of thick film and thin film technology must be applied.

Despite its smaller share of the market, an interesting technology which could also apply to trial projects in developing countries are the linear, bipolar transistor arrays. These are offered in complexities of up to 1,000

components of which the transistor share is 25 per cent. The rest are passive components such as resistors and capacitors. Regarding manufacturers, European companies such as AEG-Telefunken, Ferranti and Thomson should be mentioned. The entrance prices are between DM 20,000 to 30,000 and the price per packaged chip is DM 30 to 40 for the first 1,000 pieces. This technology is especially interesting for analog control circuits, as it can be used in the area of radio and television. For the development of indigenous devices the work with linear bipolar arrays would create good starting conditions. Also the change to design techniques of full custom ICs is possible without problem. Contrary to the digital CMOS design, however, more know-how will be required.

3.3 Standard cell design

Standard cell designs have to be processed by the customer in the same way as corresponding gate arrays, only the library of basic components can be different. Delay times may vary a little.

Standard cell technique is the best automatic design method. Each connection of function blocks which is described in the form of a node list can be transferred per computer onto a layout. The function blocks thereby vary from individual transistors to complete microprocessors and can contain digital as well as analog properties. The only condition is, that the cells can be manufactured in one technology line. The typical geometry is shown in Figure VI. The function blocks are designed geometrically as cells of the same height. The signal in- and outputs are at the top and bottom of the cell. The power lines, however, go from left to right through the cells so that its routing can be obtained by simple abutment of the cells. Function blocks of another height are also possible but then the layout algorithm will not work so effectively. The user can preplace different cells interactively. This is especially useful for big cells.

Due to the geometric limitations of the standard cells, the automatic layout programme has to solve a rather simple problem. First, it has to place the function in the different rows (placement) and then it must route them using the channels between the rows. As the width of the channels is not fixed as in a gate array, an automatic solution can always be obtained. Standard cells have hardly any restrictions. All functions which are possible within

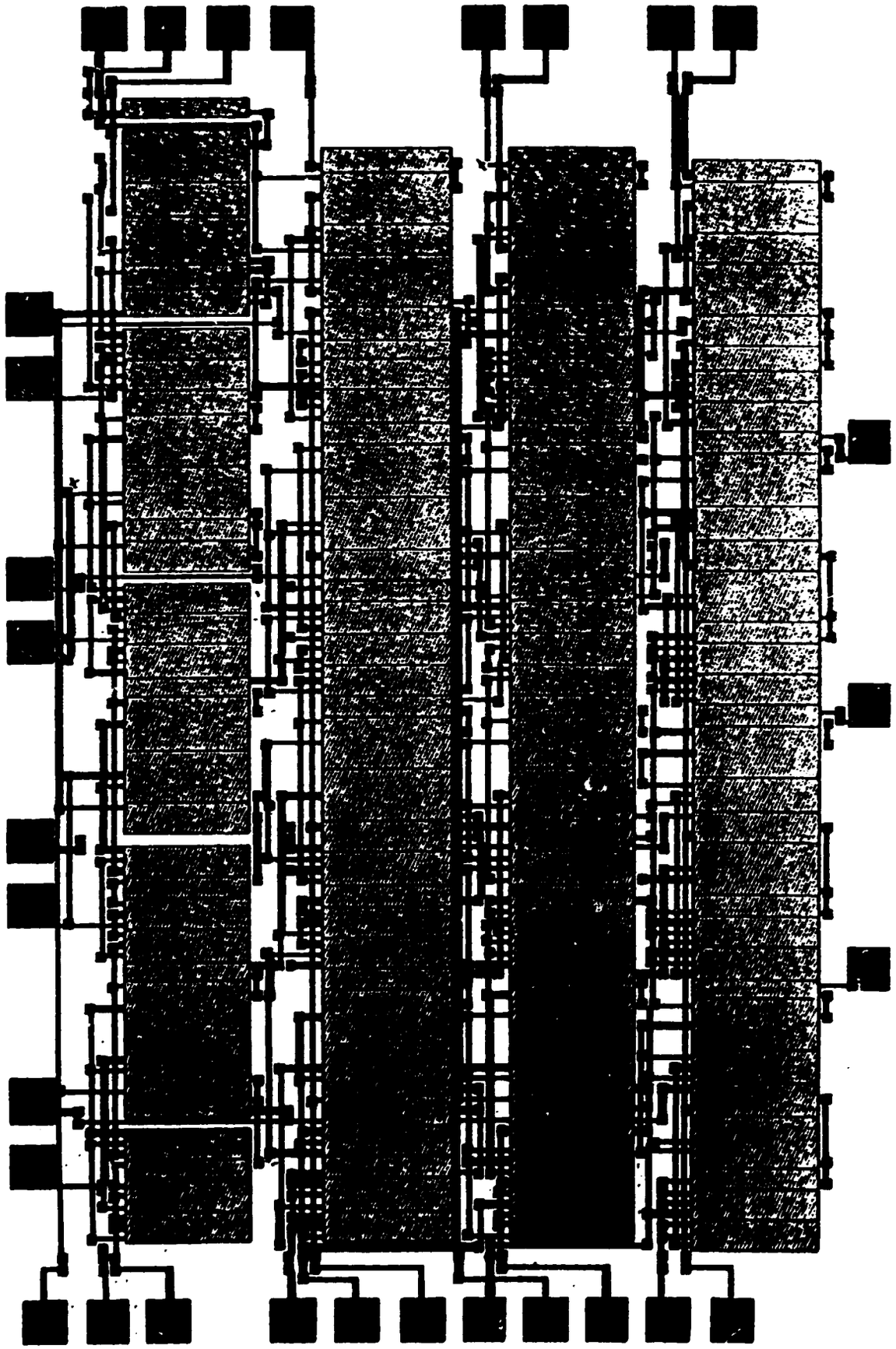

Figure VI: Standard cell design

the chosen technology can be used and therefore the standard cell process is the most flexible automatic one; analog as well as digital circuits and also the combination of both, are possible. By a better adaptation to the customer's needs compared to the gate array, the chip area will in general be smaller. The reduction in size can be as much as 65 per cent. Production costs of the single chip are therefore lower by this factor.

Greater flexibility has been achieved with the disadvantage that prefabrication, as for the gate array master, is no longer possible. All process steps have to be done as in the full custom design. The design only differs from that of the full custom method in the automatic placement because the transistors are placed and routed automatically instead of by a manual procedure. Because of 9 to 12 masks for the complete technology process, the production is much more expensive and needs much more time than the one or three masks of the gate array (three masks are necessary for the two-layer metallization). This explains the different use of the various design methods corresponding to their costs, as mentioned at the beginning of Chapter 3. Lower chip prices are contrary to higher entry costs. Prototyping with standard cell layout starts from DM 100 to 150,000. A peculiarity is that the big Japanese CMOS manufacturers have nearly identical libraries for gate arrays and standard cell design. The customer can thereby make his own choice as to which choice is the most favourable for him. A part of about one third of the market for custom ICs has been forecast for the standard cell method for 1990.

3.4 Full custom design

Full custom design is the classic technique which allows the manual transfer of an electric circuit into the optimal geometry. Figure VII shows such an nMOS design. Even if all standard components were designed in the laboratories of the large semiconductor manufacturers (this also applies to the masters of gate arrays and the libraries of gate arrays and standard cells), this design method would become less and less important to the customer. Only 30 per cent is expected for the market share in 1991 compared to 78 per cent in 1982. Apart from the high entry cost of DM 150 to 250,000, the long development time is above all a handicap for its application. Despite the greatest possible assistance by CAD programmes, the risk of errors in the

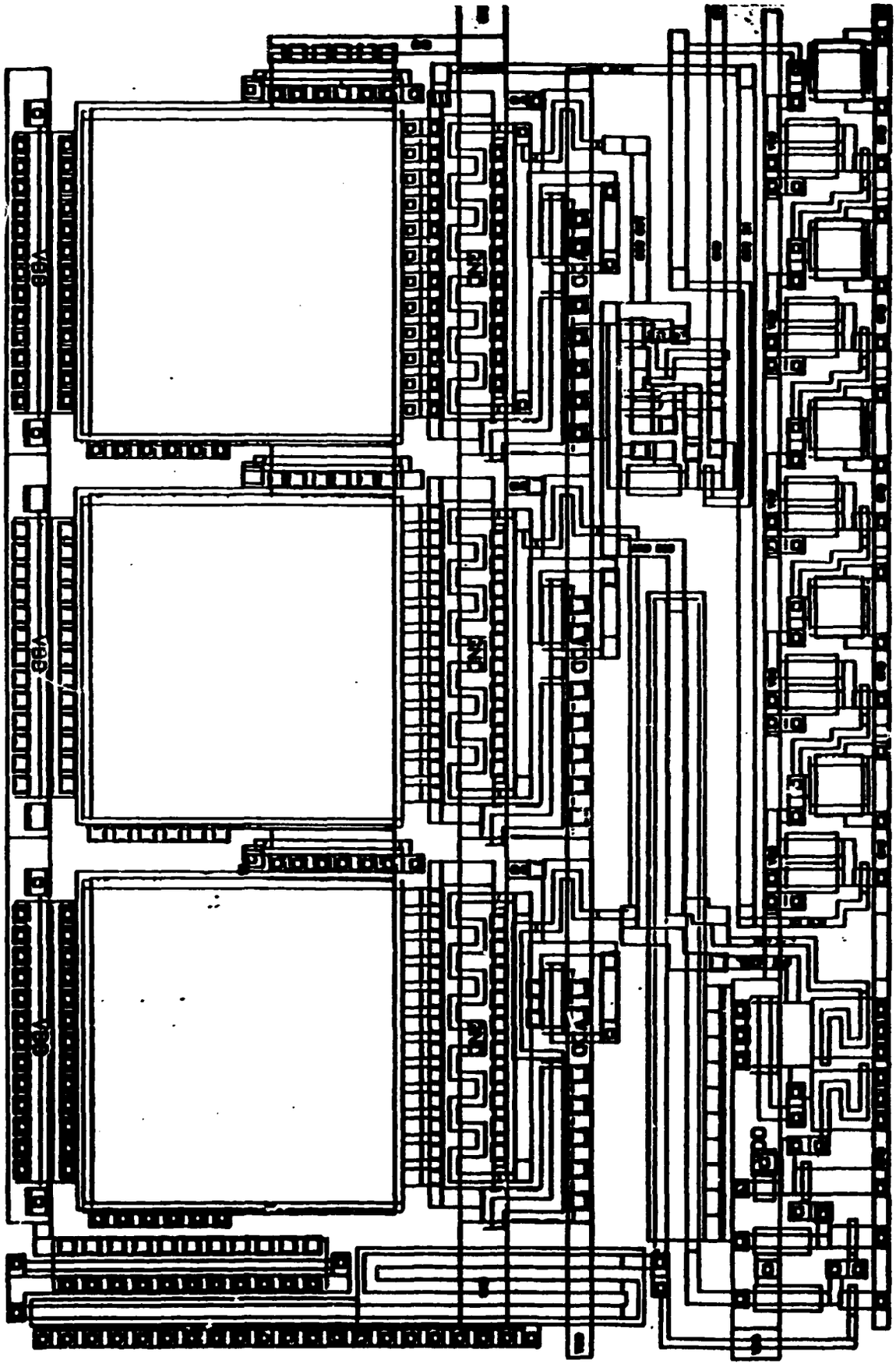

Figure VII: Full custom n-MOS layout

layout for manual design is so high that several "redesigns" (new technology runs with improved designs) often have to be made. This risk is higher with the inexperience of the designers. For a smaller company this is an incalculable risk when starting a product with the help of a full custom circuit. This method is therefore not recommended for initial projects.

Despite the foregoing, all necessary equipment and programmes are listed in Chapter 4, taking into account that this is the only possible way to support the present semiconductor factories in Arab countries. But in order to be successful, the complexity should initially not be too high. The training of designers for bipolar lines can also be carried out due to the linear arrays described in section 3.2.

The error analysis of a fabricated chip poses a special problem due to the necessary equipment and know-how of the employees. Some tools are listed in the Annex to this paper. It can be stated that efforts and knowledge must be greater the more the circuit layout has to be done manually.

This critical view of full custom design is valid, especially in the starting phase of a microelectronics laboratory, but a semiconductor factory cannot manage without these design methods or experienced designers. The normal user should choose his electronic system from among the other possibilities available.

4. CAD OF INTEGRATED CIRCUITS

User-designed silicon in 1982 represented only 5 per cent of the IC sales; however, a share of 17 per cent is forecast for these circuits for 1991. This demonstrates on the one hand the importance of the trade with standard components, and on the other hand the increase of the custom IC market. In 1984, gate arrays had returns of US$510 millions, standard cell ICs US$90 millions and full custom ICs US$775 millions. According to the number of designs, the gate array technique is the most important one, with about 4,000 designs world-wide in 1984. So CAD tools are mainly developed in this field.

4.1 Interfaces between customer and manufacturer

In the layout and manufacture of a chip seven main steps can be found:

- system architecture
- circuit design
- layout
- mask fabrication
- chip fabrication
- test
- packaging

The customer is always responsible for system architecture. The circuit design and layout can also be made by the customer and he can take responsibility for the testing of fabricated chips. Corresponding to this, there are three possible interfaces for the manufacturer on the system-, the circuit- and the layout levels. The other steps, i.e. mask fabrication, chip fabrication, packaging and standard function tests, are the tasks of the silicon foundry.

The design of an IC begins with the discussion of the different technical possibilities which are available according to Chapter 3. Alone or in discussion with a manufacturing company or with a design centre, will the desired technology be laid down, i.e., the partition of functions in one or more ICs, the use of additional PALs or standard ICs etc. The result is a block diagram of the individual functions and its proposed implementation. The performance of the whole system can be judged when compared to the costs involved. For the ICs to be implemented, exact interfaces have to be defined.

At this point, a number of companies stop their own activities in IC design. They hand this task to a design centre or directly to the manufacturer. The offer of such centres, e.g. in the Federal Republic of Germany, is high (about 70 companies), so that each centre will only make three to six designs per year on an average, thereby depressing prices. Without the need of investing in their own CAD tools, many companies can obtain their own ICs. The design of a 1,000 gate array costs about DM 40,000 when under the complete responsibiitiy of the design centre.

For the foundry and design centre concept discussed in this paper the interface on a system basis can only be the first step in training people at the design centre of a manufacturer when implementing the first project.

In the second interface at the gate or transistor level, the circuit is transferred after simulation. This interface is the most frequently used, the most standardized and the best documented one at present. It will, even in future, remain the most important one. It leaves system know-how to the customer and the technology to the manufacturer. The customer requires the electrical data-base from the manufacturer in order to be able to simulate the desired functions. This information is contained in the component library in which a number of logic functions, including their time behaviour is described. For the simplest case, the information can be found in a design manual. For some programmes and a few workstations machine-readable data-bases can also be obtained on tape or a floppy disc.

The customer can now design the circuit on the gate- or transistor level, according to the library of the manufacturer. Then he enters the circuit diagram on the computer. Today this will often be graphically made with the help of a "schematic entry" programme. In the following logic simulation the input signals will be specified and the circuit will be undergone to an exact timing analysis. The protection of the function against the "worst case" conditions is also a part of the simulation.

If logic simulation has been successfully finished, the node list is made in a format specificd by the manufacturer. Another file is created which contains the "pattern block" for later testing. Between 10 to 14 weeks after delivery of the two files the customer obtains the fabricated and tested chips and can install them in his system.

For gate arrays and standard cell designs this interface has been so successful that in future probably no other possibility will be offered. The gate array prices mentioned in Chapter 3 refer to this interface.

At the third interface the circuit is converted onto the layout. The customer requires from the manufacturer, additionally to the electric specifications interface, detailed documents about the geometric characteristics of the technology. As to gate arrays, the structure of the

master and the function library have to be available. For standard cell design a library which only contains the contacts and outlines of the elements is sufficient, instead of the complete geometry. In addition to this, design rules for the (metal-) levels edited by the user must be published. These rules can also be a part of the layout-generating programmes. Contrary to the second interface, the third one requires considerably more know-how by the user. The volume of software which is necessary is increased by a factor of three.

For the full custom design which is only possible at this level the customer needs the complete design rules from the manufacturer. Designs can only be successfully implemented if the customer has enough experience and good software packages. Furthermore, direct contact with the technicians of the manufacturing company is necessary.

The fabricated layout will be surrendered to the manufacturer in the form of a magnetic tape with the geometric structures in a common data format. This physical design will be at the customer's own risk. As opposed to the second interface, there is no manufacturer's warranty for the functioning of the fabricated chip. The manufacturer's warranty alone is sufficient reason not to aim at one's own layout. Another disadvantage of the individual layout also consists in taking over the essential test tasks by the customer after chip fabrication. Despite this, it should be pointed out that some of the design centres must reach the know-how stage of layout generation.

4.2 CAD equipment and programmes

According to both interfaces presented in section 4.1 on circuit- and layout level, the necessary software and hardware, starting with the minimal system, will be discussed at this point. The first interface on the system level does not require any equipment for the customer.

In principle, there exist three ways to CAD access:

- the development in the design centre of the manufacturer, there being a guest;
- the access to terminals which are connected with the host computer; and
- the design on one's own machines with one's own software.

A variant to the last way is the software and hardware which can be leased from several manufacturers. Whereas for a start, the first way can be discussed, in the long term only the third one is acceptable. The second way should, however, not be excluded because of its interconnection between the design centres.

The most important software package for the second interface is the logic simulator. On the basis of a standard hardware, VAX 11/750, a lot of simulators will be offered. The most familiar today is HILO of GenRad which costs about US$50,000. However, also with the help of cheaper packages such as DISIM (AEG, US$20,000), all modern gate arrays and standard cells can be successfully designed. The VAX 11/750 will soon be replaced by the cheaper and more efficient VAX station II which is offered at a price of about US$50,000, a graphic terminal included. With a programme for graphic circuit input, the hardware and software together will cost about US$100,000. Silvar-Lisco and Pheonix Data are two well-known hardware-independent software companies, but also the "workstation" manufacturers, mentioned in section 4.3, plan to offer their software for the Micro-VAX. On such a station four designs can be made at the same time.

If design centres have no access to VAX computers, the Micro-VAX is probably the best solution at present as regards the price/performance relationship. This does not at all exclude additional PCs in the same centre. Available VAX computers should, if possible, have access to Tektronix graphic terminals of the 4109 or 4115 serial in order to be able to use the standard software. The output of the node list and the pattern block is written on a magnetic tape or a floppy disc. The corresponding output programmes can be partly obtained from the different manufacturers, but they can also be written by the customer in about one month's manpower.

For the interface at the layout level additional programmes for automatic or interactive layout generation have to be installed. The programmes for the design rule check, for the electrical rule check and for the connectivity analysis should be added if the layout is done manually. The first programme looks for violation of the geometric rules, the second extracts the circuit out of the layout and the third makes a comparison with the originally simulated circuit.

Phoenix Data System and NCA offer all necessary programmes for about US$100,000 for which the Tektronix 4115 is the preferred graphic terminal, costing about US$40,000. For the Micro VAX II a graphic terminal is announced for the second quarter of 1986. Thereby, the purchase of the expensive Tektronix 4115 will become superfluous.

The programmes for automatic layout generation belong to another group. They can be obtained for gate arrays, for standard cell designs and as a silicon compiler for solutions which are similar to full custom ones. Prices begin at US$100,000 and go up to several hundreds of thousands of US dollars. The usual design centre does not have these programmes as the automatic layout can best be made by the manufacturer. The design centre of the silicon foundry has to be equipped with this software.

A very cheap option is layout generation by hand at the desk. This is, however, only successful for gate arrays. This process is very suitable for training employees. It is also done at German universities. The minimal software which is supported by the VAX/Tektronix hardware can be obtained free of charge. This software should also be available within one year for the IBM personal computer. The software includes analog simulation, a graphic editor and a programme for circuit extraction. At present, the data base is an AMI CMOS gate array.

CAD equipment on layout level varies therefore from US$10,000 (personal computer and manual layout) up to US$1 million for a professional centre with several stations. One centre at least should be equipped with all tools. For the majority of the centres, though, the interface on a circuit level is much more profitable.

4.3 The workstation concept

The workstation manufacturers are a special group of companies who offer CAD. The three companies Daisy, Mentor and Valid dominate the world market by some 90 per cent. They offer software and hardware for the interface on circuit and layout levels because they are turnkey systems. The price for a circuit level is estimated at US$80,000. A complete offer, layout included, costs about US$200,000.

All large semicustom manufacturers have installed their data bases on the stations of the three companies mentioned. When buying a workstation the customer is immediately able to develop a gate array or a standard cell chip. The change from one manufacturer to another can easily be made without changing the software. Disadvantages of these solutions are that:

- in general, the station offers only one working place;
- several stations are rather expensive;
- own CAD developments cannot be implemented and thereby the
- design centre is dependent on the workstation manufacturer.

There cannot be any doubt that a selection of all necessary software tools at one station would be the best solution. On the basis of personal computers, a whole system could cost only US$20,000 in the near future. As to the circuit level this price seems to be possible even today.

All workstation manufacturers work intensively on PCB software whereby all necessary software tools will be available at a single station instead of on systems for PCB layout (Chapter 2). Daisy has announced a package to be available in the near future.

5. SILICON FOUNDRY FOR SEMICUSTOM DESIGN

After the explanations in section 3.1.2 a silicon foundry for standard ICs has to fight against enormous start-up difficulties. It is essential that such a factory represents the present state of engineering, as only under these conditions can electronic systems be developed competitively.

An elegant way out of these difficulties could be semicustom manufacture. The factory buys the masters for gate arrays from one of the leading companies and only makes the wiring and/or the processing of the metal levels by itself. LSI-Logic of the USA obtains its array masters from Toshiba of Japan and is very successful in doing this. Investment costs for such a system are about US$2 million for chip fabrication and US$1.5 million for mask fabrication. Further, US$2 million should be added to the other eight to ten process steps, and, above all, the problem is to obtain sufficient know-how for the additional ten steps.

6. RECOMMENDATIONS

The following method may be recommended in order to install design centres for microelectronics, with or without connections to a silicon foundry.

The first task of the design centre is the development of electronic systems. The centre therefore needs equipment:

	US Dollars
- for prototype development with standard components	10,000 - 50,000
- for the development of printed circuit boards	10,000 - 15,000
- for the development of semicustom ICs	35,000 - 230,000
- furthermore, it needs test equipment for PCBs and ICs	30,000 - 60,000

Chip fabrication in an Arab country is not initially necessary in order to succeed, as an indigenous manufacture will not become economical before several centres are working successfully. At least one centre has to be equipped with layout- and/or full custom possibilities. Due to the considerably higher costs and the better skills and experience of the employees, not all centres should be equipped with chip fabrication facilities.

For the first project a digital CMOS system is suggested. An example for this is a bilingual word processing system at a cost of about US$1,000. Such a system includes standard components as well as modern gate arrays with a complexity of 1,000 to 2,000 gates. For the manufacture a PCB and a test factory should be available independently of the design centre. The final assembly can be made in TV factories or by the same method used in TV factories.

Regarding personnel in the design centres, it is recommended bringing together local specialists who have finished their studies in Europe or in the USA and work in the corresponding development departments in industrial countries. Some of these engineers have been enthusiastic in their support for the founding of a microelectronics industry in their native countries, including both hardware and software.

Initially, the best solution is to apply to companies in Japan or Europe to produce semicustom ICs. Japanese technology represents the peak of progress.

References

1. The TTL Data Book for Design Engineers Vol. 1, Texas Instruments ISBN 3-88078-037-4 Seventh Edition

2. The TTL Data Book for Design Engineers Vol. 2, Texas Instruments ISBN 3-88078-042-0 Seventh Edition

3. Schottky TTL Data Book, First Edition, Motorola Semiconductors

4. TTL Data Book, National Semiconductor

5. FAST Data Book, Fairchild Camera and Instruments Corporation

6. FAST-Schaltungen (Circuits) 1983, Valvo Unternehmensbereich Bauelemente der Philips GmbH, 2000 Hamburg 1, FRG

7. ECL Data Book, Fairchild, Mountain View, California 94042, USA

8. MECL Data Book 1982/83, Motorola Semiconductors

9. MECL System Design Handbook, Fourth Edition, Motorola Semiconductors

10. High-Speed CMOS Data Book, Integrated Device Technology Inc., Santa Clara, California 95054, USA

11. CMOS Data Book, Toshiba, Japan

12. LSI Data Book, Sixth Edition, Monolithic Memories Inc., Santa Clara California 95954-1592, USA

13. Programmable Array Logic, Advanced Micro Devices Inc., Sunnyvale California 94088, USA

ANNEX I

Digital Laboratory

			DM
1.	Standard components, clock frequency limit 30 MHz		
1.1	Component stock 80 types in TTL-LS or HCMOS 50 pieces	6,000	
1.2	Wire-wrap-equipment for wrap-wire AWG 30 pistol and tools (Standard Pneumatic)	1,200	
	Wire, different colours	180	
1.3	Sockets 14, 16 and 20 Pins: 2000 pieces (Augat, Germany)	5,000	
1.4	Wrap cards, 10 pieces (Bicc-Vero, Germany)	600	
1.5	Measuring equipment: Voltage/current supply, 5 pieces (Colant)	1,400	
	Oscilloscope (Tektronix, Iwatsu, Philips, etc.) 60 MHz	3,000	
	Multimeter	500	
	Subtotal		17,880
2.	Standard components, clock frequency limit 85 MHz		
2.1	Component stock, made up of 80 types TTL-S or FAST, 50 pieces (DM 8,000) 40 types TTL-LS or HCMOS, 50 pieces (DM 3,000)	11,000	
2.2 and 2.4	as for 1.1 and 1.4	7,000	
2.5	as for 1.5 but Oscilloscope (Tektronix, Iwatsu, Philips etc.) 100 MHz (DM 5,400)	7,000	
	Subtotal		25,400

Extension of Digital Laboratory

3.	Event counter (Tektronix, Philips, HP, Wavetek)	7,000	
3.1	Logic analyzer, either	50,000	
	KLA 48, Kontron (DM 43,000) K200, Gould (DM 70,000) Colt, Dolch (DM 48,000) HP1614, HP (DM 45,000)		
3.2	Oscilloscope (Tektronix, HP) 300 MHz	18,000	
	Subtotal		75,000
4.	Development of PAL's		
4.1	Stock, 10 types, medium complexity 25 pieces	4,000	
4.2	PAL programmer, medium performance, maximum 24 pin		
	2 L 30 Scantec	8,000	
	IBM-PC XT	6,800	
	PALASM (Software)		
4.3	PAL programmer, improved performance, for all available PAL's		
	DATA I/O	26,000	
	PP2 Scantec	20,000	
	Cupl (Software)	3,500	
	Subtotal		68,300

Microprocessor Laboratory

5.	Typ Z80		
5.1	Stock, CPU and Periphery	1,000	
5.1.1	Software development system	8,000	
	CP/M-Computer based on Z80 8 Bit-Extension	9,000	
5.2	Typ MC 68000, Motorola 16-Bit processor		

5.2.1	Stock CPU and Periphery		2,500	
5.2.2	Wrap sockets		1,000	
5.2.3	Software development system Unix-computer SUN, CONVERGENT, PCS, SPECS	DM 25,000	55,000	
	Subtotal			76,500
6.	Summary Electronic laboratory for prototyping of PCBs including 16-Bit Microprocessors Items 2., 3.2, 4.2, 5.2			263,080

ANNEX II

Manufacturers of measuring equipment

1. Tektronix, Inc., P.O.Box 1700, Beaverton, OR 97075, USA, Tel.: (800) 547-1512

2. Hewlett Packard, European Headquarters, 150 Rue du Nant d'Avril, CH-1217 Meyrin 2-Geneva, Switzerland, Tel.: (022) 83-81-11

3. Kontron Messtechnik GmbH, Breslauer Str. 2, 8057 Eching/Munich, Federal Republic of Germany, Tel.: (089) 31901-311

4. Keithly Instruments GmbH, Heiglhofstr. 5, 8000 Munich 70, Federal Republic of Germany, Tel.: (089) 7144065

5. John Fluke Mfg. Co., Inc. P.O.Box C9090, Everett, WA 98206, USA, Tel.: (206) 356-5500

6. Iwatsu Electric Co., Ltd. Overseas Operation Dept., 2-1-3, Nihonbashi, Chuo-Ku, Tokyo 103, Japan, Tel.: 03-272-0461

7. Gould Inc. Design and Test Systems Div., 4600 Old Ironsides Dr., Santa Clara, CA 95050-1279, USA, Tel.: (408) 988-6800

8. Data I/O Europe, Vondestraat 50-52, 1054 GE Amsterdam, The Netherlands, Tel.: (020) 186855

9. Philips, 5600 MD Eindhoven, The Netherlands, Tel.: (040) 78-23-70

10. Scantec GmbH, Landshuter Allee 49, 8000 Munch 19, Federal Republic of Germany, Tel.: (089) 134093

ANNEX III

Major semi-custom manufacturers

Japan:	-	FUJITSU
	-	TOSHIBA
	-	NEC
	-	OKI
USA:	-	LSI LOGIC
	-	MOTOROLA
	-	TEXAS INSTRUMENTS
	-	FAIRCHILD
	-	AMI
	-	AMD
	-	SILICONIX
Europe:	-	FERRANTI
	-	VALVO / PHILIPS
	-	THOMSON (MOSTEC)
	-	SGS-ATES
	-	MATRA HARRIS
	-	PLESSY
	-	SIEMENS

ANNEX IV

CAD, Soft- and Hardware
(incomplete)

		US Dollars
1.	**Workstations: Integrated systems for nearly all CAE-tasks**	
1.1	Daisy PCB-, gate array-, standard-cell and full custom design, data-bases of many manufacturers	230,000
1.2	Mentor PCB still under development, all 3 custom methods	200,000
1.3	Valid as 1.2	180,000
2.	**Workstation for single tasks**	
2.1	PCB-Layout:	
2.1.1	Calay VO	100,000
2.1.2	Racal	300,000
2.2	Logic simulation for PCBs and semicustom ICs:	
2.2.1	Daisy (IBM AT)	35,000
2.2.2	Valid (IBM AT)	34,000
2.2.3	Valvo Philips (IBM AT) (only hardware, software free as part of the gate array contract)	20,000

3. **Standard software packages**

The standard hardware of today is a VAX 11/750 from Digital Equipment and a Tektronix Color Graphic Terminal, Serial 4107, 4109 or 4115 etc. The price for such a configuration reaches US$250,000. The new DEC-System Microvax II will be offered in 1986 for US$50,000 including colour terminal with nearly the same performance. It can be expected that this station will become the new CAD-standard.

3.1 Integrated system:

3.1.1	Phoenix Data System logic simulation for semi-custom layout full custom layout including all steps of layout checks and schematic entry	100,000	200,000

3.1.2	Silvar Lisco Different simulation packages, automatic layout tools for semi-custom design and schematic entry	50,000	200,000
3.1.3	NCA Corporation All full custom tools, especially all layout checks and schematic entry	100,000	200,000
3.1.4	The workstation manufacturers VALID and Daisy are intending to offer their software packages also for the Microvax in he near future.		
3.2	Single software packages:		
3.2.1	Logic simulation HILO of GENRAD Corp. DISIM of AEG		40,000 25,000
3.2.2	Different software packages are available free of charge from universities in the field of simulation of analog circuits (SPICE etc.), simulation at the register level (RTS1A etc.), layout editing (KIC etc.), design rule check etc. Ready access to the group of VAX users and their software packages would be an advantage for the open VAX-configuration.		

ANNEX V

Equipment for a CMOS-Line
(without equipment for making photomasks)

	Thousands of DM
Photolithography	
Wafertrac	200
Maskaligner	300
Maskcleaner	100
Asher	60
Clean Benches	200
Implementation/Diffusion	
Diffusion furnace 2 x 4 stack	500
Implanter (medium current)	3,000
Rapid Annealer	200
Low Pressure Chemical Vapor Deposition	
LPCVD Poly-Silicon	200
LPCVD Si_3N_4	200
LTO (Low Temp. Oxide)	250
Plasma-Deposition	
Si_3N_4	300
Metallization	
Sputter-Deposition Al, Si, Cu	300
Clean Room Equipment	
Clean benches with cleaning and wet etching stations	
Inprocess Test, Inspection	
Electrical Test	200
Microscope	50
Thickness, steps	100
Optical (Ellipsometer)	100
Linewith	100
REM	1,000
Packaging	
Dicing saw	100
Chipbonder	50
Wirebonder	50

ANNEX VI

Equipment for testing ICs

	DM
Full custom design:	
- Wafer prober (Süss, Fed. Rep. of Germany)	77,000
- Semiconductor analyzer (HP), including plotter	60,000
- LCR meter (HP)	30,000
- Logic analyzer (Tektronix), including pattern generator	50,000
- Oscilloscope (Tektronix)	6,000
- Curve tracer (Tektronix)	25,000
- Multimeter, etc.	6,000
	254,000
Semi-custom design (digital circuits):	
- Logic analyzer	50,000
- Oscilloscope	6,000
- Multimeter etc.	6,000
	62,000