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A REVIEW OF THE STATE-OF-THE-ART OF GaAs RESEARCH*

prepared by

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ABBREVIATIONS

AlGaAs	*aluminium gallium arsenide*
BFL	*buffered FET logic*
CAD	*computer aided design*
CCFL	*capacitor coupled FET logic*
CMOS	*complementary symmetry metal-oxide-semiconductor*
D-MESFETs	*depletion mode MESFETs*
DAC	*digital to analogue converter*
DARPA	*Defense Advanced Projects Agency*
DBS	*direct satellite broadcast*
DCFL	*direct coupled fet logic*
E-MESFETs	*enhancement mode MESFETs*
EBL	*electron beam lithography*
ECL	*emitter coupled logic*
EW	*electronic warfare*
FET	*field effect transistor*
GaAs	*Gallium Arsenide*
HBT	*heterojunction bipolar transistor*
HEMT	*high electron mobility transistor*
IC	*integrated circuit*
JFET	*junction gate FET*
L-Band	*1.1 GHz to 1.7 GHz*
LED	*light emitting diode*
LSI	*large scale integration*
MBE	*molecular beam epitaxy*
MESFET	*metal semiconductor field effect transistor (Schottky gate contact)*
MMIC	*Microwave Monolithic Integrated Circuit*
MODFET	*modulation doped field effect transistor*
MSI	*medium scale integration*
NMOS	*n-channel metal-oxide-semiconductor*
PIN	*p-type - intrinsic - n-type diode structure*
RAM	*random access memory*
SAG	*self-aligned gate*
SCL	*source-coupled logic*
SDFL	*Schottky diode FET logic*
Si	*silicon*
SPDT	*single pole double throw (switch)*
SRAM	*static RAM*
TEGFET	*two-dimensional electron gas field effect transistor*
VLSI	*very large scale integration*
VHSIC	*very high speed integrated circuit*
X-Band	*8.2 GHz to 12.5 GHz*

CONTENTS

SUMMARY

This review deals with a variety of aspects of GaAs research, spanning both digital and analogue applications. The relative merits of GaAs as a material for high speed semiconductor devices are presented. The prospects of gallium arsenide as a competitor to silicon for digital applications are investigated. The recent upsurge in heterostructure research is highlighted with reference to high electron mobility transistors (HEMTs) and heterojunction bipolar devices. The performance of these new devices is compared with that of the well established enhancement and depletion mode field effect transistors (MESFETs) used in present GaAs IC technology.

The present performance of GaAs integrated circuits is discussed in detail and related to the expanding market for this type of technology. The current state of GaAs IC research is described for both digital and analogue devices. State of the art results are reported and likely areas of improvement indicated. The important area of testing, packaging and reliability, crucial to the success of all commercial technologies, is addressed. Recent advances in material growth, device design and fabrication are outlined. The requirements for sub-micron geometries, necessary for further improvements in speed and performance, are outlined with particular reference to crystal growth, molecular beam epitaxy and electron beam lithography techniques. Developments in the areas of computer aided design and the appearance of industrial IC foundry services are reported. Areas of significant collaboration between industry, research institutes and universities throughout the world are highlighted.

The rapidly expanding area of integrated optics is also discussed, with reference to the likely impact on the fibre-optic communications systems market. Finally, the future prospects for GaAs technology are outlined. The review concludes with the suggestion that gallium arsenide technology will be utilized in conjunction with silicon technology rather than as a substitute for it in most systems.

INTRODUCTION

Recent advances in gallium arsenide technology have led to a dramatic increase in interest in using gallium arsenide (GaAs) integrated circuits in a wide range of applications. Initial interest centred around analogue applications, and the early 1980's saw the birth of a new generation of GaAs monolithic microwave integrated circuits (MMICs). Current trends however, suggest that the development of high speed digital IC's will dominate GaAs technology.

Gallium arsenide has several properties which lead to superior high frequency/speed performance when compared with silicon. Gallium arsenide has a higher low field electron mobility than silicon, which allows electrons to reach a peak velocity in excess of twice that of electrons in silicon. Furthermore, in very small devices (sub-micron) the phenomenon of 'velocity overshoot' allows even higher velocities to be obtained (upto five times those achieved in silicon devices). Another advantage of GaAs over Si is that devices fabricated using n-type material have the property that sub-micron epitaxial layers grown on semi-insulating GaAs, exhibit mobilities approaching the bulk value. This contrasts with silicon where thin layers grown on insulators exhibit substancially lower mobilities than the bulk value. It is this feature of n-type GaAs which gives GaAs transistors lower parasitic resistances and higher gains than similar silicon devices.

Digital integrated circuits fabricated in GaAs offer advantages in speed, power dissipation, operating temperature range and radiation hardness when compared with silicon. GaAs digital integrated circuits have the high speed capability required for very high-speed computers, high data rate communication systems, and high-speed wide-bandwidth measurement systems. Space and military applications take advantage of a radiation hardness which extends beyond 10 megaRADs for GaAs ICs. Silicon MOS circuits generally fail around 10 kRADs - the best silicon circuits withstand 1 MRad. GaAs IC's have been operated over the temperature range -200 to 300 degrees Centigrade, and consequently circuits have been developed to take advantage of this temperature range for use in combustion engines and other hostile environments.

Gallium arsenide discrete analogue devices first appeared with the introduction of the transferred electron oscillator (Gunn diode) in the early 1970's. This two terminal device which is capable of generating power at microwave frequencies was rapidly incorporated into microwave sub-systems and is still used extensively in both commercial and military applications. Interest in using GaAs spread with the widespread introduction of the GaAs MESFET (metal semiconductor field effect transistor) which is used in a wide variety of microwave applications upto 40 GHz. The demand for integrated sub-systems led to the development of analogue GaAs

MMICs, for applications such as direct broadcast satellite (DBS), receiver front-ends and phased-array radars. The first commercial GaAs analogue IC was introduced by the Harris Corporation in February 1984. Upto the present time the drive to develop analogue MMICs has not matched the effort put in to the rapidly expanding digital field. This can be partly attributed to the well funded research and development programs dedicated to digital GaAs research (such as the DARPA program in the USA).

The speed advantage of GaAs over silicon has led to the rapid development of GaAs digital circuits. Considerable effort in the United States, Europe and Japan has already resulted in the development of nanosecond access time 16 kbit GaAs RAMs. Research in the USA and Europe has been aimed largely at military applications and commercial communication systems, whereas strong investment by Japanese companies has been directed towards the rapid development of fifth generation computers.

The recent development of heterostructure transistors (HEMT, MODFET or TEGFET, and the HBT), which promise operating frequencies upto 100GHz has already been exploited with the development of very high speed digital IC's capable of operating well in excess of 10 Gigabits per second. The very high demands placed on fabrication technology by these devices (some of which require layer thicknesses of less than 100A and contact widths of less than 0.2um), has in turn led to increased efforts in developing l ter crystal growth, molecular beam epitaxy (MBE), dry etching techniques and high performance electron beam lithography.

Another expanding area of application for GaAs and related compounds lies in the field of optoelectronics. Solid-state sources and detectors are key components in fiber-optic communication systems. Research into developing integrated electro-optic sub-systems has already begun.

Performance of GaAs Integrated Circuits.

Although GaAs has substantial advantages in terms of power dissipation, speed, operating temperature and radiation hardness, there are other factors which must be considered when comparing the relative merits of silicon and gallium arsenide. In particular the complexity, reliability, availablity and cost are important factors in determining the best choice of technology. Recent developments in distributed parallel processing using VLSI silicon technology have tended to offset the immediate speed advantages gained from GaAs in a number of computing applications. However, there are many applications where parallel processing is not applicable. Specifically, bit stream processing, which incorporates error detection and data correlation, and data acquisition and sampling systems for wideband signal processors are not suited to parallel processing. Future systems will inevitably exploit the best attributes of each technology, and GaAs and Si sub-systems will be incorporated into areas which make the optimum use of their capabilities.

The relative performance of GaAs and Si technologies are shown in Figures 1 to 3. The speed of silicon CMOS, NMOS, TTL and ECL families is compared with the faster GaAs MESFET, HEMT and HBT logic technologies in Figure 1. It is clear that present GaAs HBT technology is ten times faster than the fastest silicon ECL logic and nearly fifty times faster than CMOS. Even the well established GaAs depletion-mode MESFET is three times faster than ECL, which in view of the relatively simple fabrication technology of MESFET logic makes it an attractive alternative for high speed integrated circuits. The speed-power product shown in Figure 2 for various technologies again demonstrates the superior performance of GaAs. GaAs MESFETs are shown to have a speed-power product six times better than CMOS – the nearest silicon competitor. Newer GaAs/AlGaAs technologies offer even better characteristics, with speed-power products ten times lower than CMOS.

At the present time, the relative maturity of silicon technology allows much greater levels of integration to be achieved than is possible in GaAs. Figure 3 shows the past, present and predicted trends in IC complexity. CMOS digital circuits with over 100,000 gates are already available, whereas GaAs technologies only extend to tens of thousands of gates at the present time. Hence, although the level of IC complexity is increasing rapidly for GaAs and GaAs/AlGaAs technologies, system designers still do not have the high-density, high-level functions available from silicon VLSI/VHSIC technology.

The Markets for GaAs ICs

The market for digital and analogue GaAs ICs is developing rapidly. A recently released report (Electronic Trend Publications) forecasts an increase in demand from the current $60m worth of business to $1.6 billion by the year 1990. Gallium arsenide ICs are being developed for a wide variety of applications, ranging from specialised very high speed digital signal processors for military applications, to high-volume consumer requirements such as direct-broadcast satellite receivers (DBS) and fibre-optic communication links. At the present time military applications represent 76% of the overall market. It is predicted that this figure will drop to 30% by the end of the decade with a corresponding increase in the DBS and communications market to 35%.

Upto the present time the microwave communications market has been dominated by discrete component technology (in particular GaAs MESFETs have an important role as low noise amplifiers). Small-scale GaAs integrated circuits are currently being introduced and pre-scaler (frequency divider) circuits are already available. Medium-scale integrated circuits such as data-multiplexers, demultiplexers, variable-dividers and pattern generators are at pre-production stages. These MSI circuits have an existing market and are economically viable because of the reasonable yields possible.

The GaAs IC industry has upto now been driven by military requirements, where high speed digital and high frequency, light weight analogue circuits are required in high technology defense systems. Signal processing and phased-array radar applications require GaAs technology to achieve the specifications required by the military. Research in the USA has led to the production of 16kbit RAMs and 10000 gate arrays.

The demand for higher speed logic and memory for computers has stretched silicon technology to the limit and although current research into new types of silicon devices promises to extend the speed capabilities of existing technology, GaAs ICs have already been produced which provide the necessary improvements. Silicon central processor units are being developed with over 5 million gates. Since the CPU cycle time is limited by the propagation delay between components, it is necessary to pack the components as closely as possible in addition to maximising their speed of oparation. The consequent increase in packing density and size of component leads to a problem in disposing of the heat generated within the CPU. Again GaAs has the advantage over silicon that it has lower power dissipation as well as faster switching speeds. Impressive developments in GaAs digital IC technology have been reported by both Japan and the United States. The Japanese have already presented results for 4kbyte RAMs fabricated using HEMT technology for ultra-high speed operation.

There is considerable speculation that GaAs ICs will follow the path of silicon integrated circuits towards high-volume, low cost production. However, many applications for GaAs ICs are relatively specialized and hence it would be expected that most GaAs IC designs would not be required in very large volumes. It may be that the market for fast GaAs logic and memory ICs will justify large scale production (but not on the scale of silicon), but it is unlikely that a wide range of analogue MMICs will be required in large production quantities (with the possible exception of DBS circuits). As a consequence of the requirement for limited supplies of specific types of GaAs ICs, custom research, design and development will be necessary for many systems applications.

GaAs IC RESEARCH

Research on gallium arsenide integrated circuits has been largely concentrated in the United States and Japan, although there has been substancial activity in European countries. The USA and European countries have recently concentrated research on digital integrated circuits. The US government has decided through the Defense Advanced Projects Agency (DARPA) to set up GaAs foundries with $45 million from the government and a further $22 million being drawn from private industry. Companies such as Rockwell and Honeywell are key members of the group involved in this concept. The ESPRIT program in Europe has provided support in some areas for GaAs IC research. In Japan, the Ministry of International Trade and Industry has been responsible for stimulating GaAs IC research and development. Japan's main interest, in contrast to other Western countries lies in a

largely non-military area, developing commercial fifth-generation computer technology. Japan's research is again dominated by digital requirements and impressive results are already being reported at conferences.

Research on analogue ICs appears to be lagging behind the better funded digital area. The absence of strong government support has generally led to research being motivated by private venture funding for commercial aims (DBS etc) or hopeful military contracts (phased-array).

Research on Analogue Integrated Circuits

A large number of companies in the United States have research programs for analogue GaAs ICs (MMICs). Companies such as Avantek in the USA have developed broadband MMIC feedback amplifiers capable of operating from 0.1 to 12 GHz. Rockwell International have developed a fully monolithic 20GHz transmit module for the NASA Lewis Research Center, which has a 5-bit phase control and exhibits a gain of 16dB from 17.7 to 20GHz. In the United Kingdom, companies such as Plessey and GEC have led the way with research on analogue ICs, and others such as STC and Thorn are investing strongly in this area. Effort has largely been devoted to developing small-scale integration analogue circuits such as amplifiers, mixers and phase shifters. Thomson CSF of France initiated research into monolithic amplifiers and have developed improved design aids for analogue circuits [1]. NEC in Japan have recently reported research on an X-Band voltage controlled oscillator [2], which represents the increasing interest in wideband monolithic sources.

The demand for GaAs IC technology and availability of design and fabrication facilities has created a number of options for the system designers. Companies with established GaAs research, design and fabrication facilities clearly will opt for in-house production. Many companies have aquired design expertise but lack the fabrication facilities and expertise. In this situation in-house design and the use of external 'foundry' fabrication is an option. Systems manufacturers may choose to contract-out the whole process with merchant designers and separate foundry fabrication. Finally, for applications requiring limited quantities of specific designs, custom design and fabrication facilities are offered by some companies. The relatively recent upsurge in the number of companies offering 'foundry' facilities is evidence of GaAs IC technology reaching a useful state of maturity. The function of 'GaAs Foundry Operations and Standardization of GaAs ICs and packaging was recently discussed at the 1985 GaAs IC Symposium.

Analogue ICs are currently being developed across the full microwave frequency spectrum of 1 GHz to 30 GHz. Broadband EW sub-systems, particularly phased-arrays, represent a major area of interest. The other principal research area is concerned with the commercial application of DBS.

The distributed amplifier is a circuit which has received a great deal of interest from Western researchers. Hughes have successfully developed a seven section 2 to 30 GHz amplifier, which exhibits a gain of 6 +/- 0.3dB across the band. A packaged amplifier design was recently described by Jones et al of Tektronix [4].

Feedback amplifiers have been produced at lower microwave frequencies, such as the single supply 1–3 GHz design by Motorola [5] and the 0.8–1.8 GHz low noise DBS design of Plessey [6]. Monolithic switches have been the subject of considerable research effort by many laboratories. Plessey have described an L-Band SPDT switch [6]. Bedard et al of Adams-Russell Co. have reported a high performance L-Band GaAs SPDT switch with an insertion loss of 0.8dB and an isolation of 35dB at 1.5 GHz [7]. Raytheon have developed several fast GaAs FET switch designs to cover the 0–20GHz regime, for broadband EW applications [8]. GEC (Hirst) have investigated GaAs surface orientated PIN diodes for monolithic switching applications, using both conventional and new shallow trench fabrication techniques [9]. A high gain X-Band limiting receiver amplifier has been recently developed by TI in the USA [10].

The DBS area has stimulated several major research projects. NEC have reported a fully integrated 12 GHz low noise converter, consisting of a low noise amplifier, image-reject filter, dual-gate FET mixer and buffer amplifier integrated onto a single chip [11]. Avantek have also described a low-cost 4 GHz low noise amplifier for television receiver only (TVRO) applications [12].

Millimeter-wave ICs are an important developing research area and several papers addressed this subject at the recent IEEE GaAs IC symposium. B. Spielman of the Naval Research Laboratories gave an invited paper on monolithic millimeter-wave integrated circuits at this symposium. A 115 GHz monolithic GaAs FET oscillator, developed by Tserng and Kim of Texas Instruments, demonstrates the impressive high frequency capabilities of this technology [13].

Research on Digital Integrated Circuits

Gallium arsenide has a substantial speed-power advantage over silicon technology. This was demonstrated clearly at the 1984 GaAs IC Symposium, where a group from the LEP laboratories (France) compared the performance of a complex 40 gate circuit fabricated in silicon NMOS and GaAs BFL logic [14]. It was reported that the GaAs circuit (a 3 bit feed-back adder) was three times faster at the same power levels and consumed one-tenth the power when operated at the same switching rates.

Intensive research on digital ICs has led to a dramatic increase in the integration levels possible. As a result of this research effort, 16 kbit random access memories (RAMs) have recently been reported. transistors. In particular, a very high density 16 kbit static RAM, with over 100,000 transistors, has been described by NTT, which uses self-aligned gate technology in conjunction with a two inch wafer process [15]. This RAM, which used direct coupled FET logic, has an access time of 4ns and dissipates 2.5 watts. A creditable 99% yield is claimed, based on functional 4k blocks. NTT have also developed a 2 ns access time 1 kbit RAM using 0.95 micron gate length enhancement mode transistors. A fast 2.6ns access time 4 kbit RAM, dissipating 1.8 watts, has been reported by the Toshiba Research and Development Center [16]. The Toshiba circuit uses both depletion and enhancement logic, and is fabricated using buried gate technology. Rockwell have put the

emphasis on low power dissipation with the development of a 2.8ns access time 1k bit static RAM, developing only 110 mW [17]. They achieve low operating powers using a depletion mode process with high resistance Cermet load resistors in each cell. Rockwell are developing a 4k GaAs static RAM, which dissipates 1 microwatt/bit in standby and has an access time of 10ns. Using a 3 inch wafer process, they have produced 15 completely functional 256 bit RAMs on a single wafer. The Cermet resistor process was again used to minimise power dissipation. Rockwell report read and write access times of 1 and 2 ns respectively for the 256 bit RAMs.

Material and process refinements have gradually made direct coupled FET logic (DCFL), which uses normally-off enhancement mode MESFETs (E-MESFETs), the most promising approach in GaAs for future LSI and VLSI circuits. This technology has been used to fabricate 3000 gate 16 x 16 bit parallel multipliers and fast static 16k RAMS (SRAMs) with 5ns access times and dissipation levels as low as 2 watts. Small-scale integration and MSI level circuits, such as multiplexers and prescalers, have been designed using other GaAs FET technologies such as buffered FET logic (BFL), Schottky diode FET logic (SDFL), capacitor-coupled FET logic (CCFL) and source-coupled logic (SCL), which utilize normally-on depletion mode MESFETs (D-MESFETs). Enhancement-mode MESFETs used in DCFL have many advantages over depletion mode devices. E-MESFETs allow single power supply operation (D-MESFETs require both positive and negative supplies), simpler logic gates, lower supply voltages, low power dissipation and consequently higher integration densities (necessary for LSI/VLSI). The major drawback of E-MESFETs is that they require a relatively complex and expensive process technology, to achieve the extremely thin, lightly doped channel region. The thin active layers are extremely surface-sensitive, highly resistive and can be difficult to control. A final restriction with E-MESFETs is that they are limited to a small logic voltage swing of around 0.5V before strong forward gate conduction occurs. LSI design philosophy requires the difference between the voltages representing logical 1 and 0 states to be twenty times the standard deviation of the threshold voltage, which means that the E-MESFET threshold voltage must be uniform to within 25 millivolts . This clearly puts stringent demands on the wafer quality and processing control. However, improvements in fabrication technology and material growth have made E-MESFET and DCFL technology viable for LSI applications. Rocchi of LEP reported at the 9th European Specialist Workshop on Active Microwave Semiconductor Devices, that for fast, low power LSI applications, 0.6 micron gate length DCFL circuits were three times faster than 0.6 micron gate length silicon NMOS and consumed ten times less power at the maximum speed of the NMOS circuit. Rocchi also claims that these results also apply as an approximate comparison for silicon ECL and CMOS circuits for continuously operated systems [18].

A number of laboratories have been investigating direct coupled FET logic. AT & T Laboratories have developed frequency dividers and multiplex-demultiplex IC set, with 12:1 multiplex capabilities operating at 1.3 GHz [19]. Flahive et al report gate delays of around 30pS, with speed-power products of the order of 4.3fJ for these circuits. Direct coupled FET logic (DCFL) has also been investigated by OKI Electronic Industry Co., who have been using enhancement mode designs in

conjunction with MOCVD epitaxial techniques, to develop a 11.7ns, 8 x 8 multiplier, dissipating 103 mW [20]. GaAs JFET technology for DCFL large scale integrated circuits was described by Wada et al of the Sony Corporation at the 1985 GaAs IC Symposium [21]. Sony, McDonnell Douglas and Toshiba have been pioneering research into GaAs JFET technology for ICs, as an alternative to the popular self-aligned gate (SAG) approach. Sony and McDonnell Douglas place the gate beneath the surface by p-type ion implantation. Toshiba have developed a reactive gate technique, where reaction between a platinum gate and the GaAs surface is used to produce a 'virtual' recessed gate.

Digital circuits incorporating heterostructure devices are being investigated in a number of laboratories. Heterojunction bipolar transistors (HBTs) and high electron mobility transistors (HEMTs also known as TEGFETs or MODFETs), fabricated from GaAs and AlGaAs using MBE technology, are being used to produce very high speed ICs. Fujitsu reported a 2 ns access time for a cooled (77 K) 4 kbit static RAM, based on 1.5 micron gate length HEMTs [22]. They expect to achieve sub-nanosecond access times from a 1 micron gate length RAM currently being investigated. Kobayashi et al of Fujitsu have reported a fully operated 1 kb HEMT static RAM at the 1985 IEEE GaAs IC Symposium [23]. A high speed 4x4 bit parallel multiplier using selectively doped heterostructure transistors was described by Schlier et al of AT & T Bell Laboratories at the same symposium [24]. Pei et al of AT & T described a 10 GHz frequency divider at the 1984 GaAs IC Symposium which used 0.4 micron gate length, selectively doped, HEMTs [25]. This ultra-fast circuit achieved gate delay times of down to 11ps/gate, with a speed-power product of 15fJ/gate. HBTs have been successfully incorporated in an 8.5 GHz frequency divider by Rockwell, who used emitters 1.6 microns wide [26].

High speed digital to analogue converters (DAC) are the subject of research by the Hughes Research Laboratories. A 6 bit DAC has already been reported by this laboratory, achieving 700 ps settling times [27]. A particular effort is being made in this area to improve the processing technology to achieve higher DAC speeds. Hsieh et al of Hewlett Packard recently described their latest results for a 12-bit GaAs digital to analogue converter at the 1985 GaAs IC Symposium [28].

A wide range of other GaAs digital circuits have been reported for logic applications. These include multipliers such as the Rockwell 8 x 8 multiplier exhibiting a 5.2 ns multiply time, the Fujitsu 16 x 16 bit multiplier with 10.5 ns multiply time, and adders such as the NEC 32 bit adder with a 7.6ns add time. A large number of small scale integration ICs have also been demonstrated (combinations of gates, shift registers, counters etc.). Furutsuka et al of NEC have described a GaAs IC 12x12 bit expandable parallel multiplier using LSI sidewall-assisted closely spaced electrode technology [29]. This circuit was designed using depletion mode FETs in BFL and SCFL logic gates, because of their high load drivability and large noise margin. The circuit was shown to perform within a 4ns critical path delay.

A new era in macro cell array design, allowing customisation of ICs without incurring the development costs of full custom design, has dawned with the

appearance of a commercially available 3 GHz array, announced in October 1985 by Harris Microwave Semiconductors. The macro cell array which uses MSI technology, has 48 NAND gates, 8 NOR gates, 88 inverters, 8 master/slave D flip flops and several other functions, and is claimed to be twice as fast as other GaAs arrays presently available on the market. The array is aimed at both the satellite communications market and military applications, where high operating speeds, low cost and rapid delivery are important. Rockwell International are also developing a group of mask programmable GaAs circuit elements, for use in high speed, high performance communication systems. The Rockwell system will be based on buffered FET logic, which was chosen after an analysis of the speed/power/size trade-off of the different GaAs logic technologies.

Higher operational speeds can be obtained from GaAs digital circuits by operating them at low temperatures. Texas Instruments have demonstrated that a speed improvement of 50% can be achieved by operating the ICs at 77K rather than at 300K. The improved speed of operation leads to an increase in power dissipation of around 50%. Research has shown that GaAs devices with highly doped active layers are more suitable for low temperature operation.

NASA in conjunction with the University of Virginia have been investigating the feasibility of digital transmission systems based on monolithic GaAs technology. They aim to develop satellite channel modems with a two billion bit-per-second data rate using a 20 GHz carrier. The system must have a low weight, high efficiency, high r.f. power and low cost specification.

Testing, Packaging and Reliability

Methods of testing and packaging very high speed/high frequency circuits are major concerns in order to ensure optimum reliability and performance of the IC. Low frequency parametric testing of integrated circuits which have process-monitor test circuits included on them is routinely used as a primary test for GaAs ICs. In contrast, high speed/high frequency testing is considerably harder to implement. Gigabit automated testers are not commercially available and considerable effort is currently being devoted to developing both analogue and digital automated test facilities. An invited review describing the 'Testing of GaAs Digital ICs' was recently presented by T. Gheewala of Sperry Semiconductor Operations, at the 1985 IEEE GaAs IC Symposium in Monterey [30]. Plessey have addressed the problem of automatic testing of analogue GaAs ICs, and in a paper by Buck and Eddison they describe an ATE system for on-wafer testing of GaAs MMICs [31]. This system is claimed to measure chips at the rate of one chip every two minutes for a two inch wafer process, when optimised.

Packaging for GaAs ICs represents another area of concern. Difficulties encountered with degradation in circuit performance due to packaging parasitics (package capacitances and lead inductances) has led to the development of new packaging technologies. In particular efforts are being made to minimise die bonding capacitances and allow wideband operation. Gigabit logic have developed 36 pin packages for GaAs ICs [32]. They have used two main approaches - a design based

on four-layer ceramic technology which has been used with clock frequencies upto 2.5 GHz, and a new silicon subcarrier concept which utilizes co-planar transmission lines and includes bypass capacitors and terminating resistors for GaAs ICs. This latter approach allows clock rates of up to 4GHz to be used. Harris Semiconductors have developed a high packing density "Waferline" package, in which chips are mounted in hollows in the package. Magnavox have introduced a low cost package which is claimed to be suitable at 5GHz. Smith et al of TriQuint Semiconductor Inc. recently presented a paper on 'New Approaches to Packaging for High Speed GaAs Integrated Circuit Application' which outlined the company's latest methods of packaging [33].

There is still very little information available on the reliability of GaAs ICs. The diversity of GaAs and GaAs/AlGaAs technologies presently being considered for IC fabrication has meant that reliablility research effort has been relatively uncoordinated. The electromigration properties of interconnecting tracks on GaAs surfaces has received some detailed consideration. Kretschmer and Hartnagel recently presented a paper relating the surface quality of GaAs to material migration, using an XPS analysis technique [34]. They investigated five surface conditions based on various etching and cleaning processes commonly used in IC fabrication. They concluded that it is necessary to provide as far as possible native-oxide free surfaces between closely-spaced neighbouring conductors, and that it it is desirable to use a suitable surface treatment to achieve a high reliability. The reliability of HEMTs (MODFETs) and ICs which incorporate HEMTs has been investigated by Christou et al, who have conducted accelerated stress tests for circuits operated in the range 150 to 210 degrees centigrade [35]. They identified the failure mode to be diffusion controlled degradation of the two-dimensional electron gas layer. This manifested itself as a degradation in the transconductance. It was also found that a high incidence of alpha radiation induced burnout in the HEMTs, which may be due to parasitic conductance in the AlGaAs layer and in the inverted heterojunction inteface.

Materials, Design and Fabrication of GaAs Integrated Circuits

GaAs integrated circuit technology has matured to the point at which companies in the United States, Japan and Europe achieve consistent yields on small production runs of MSI GaAs ICs. This reflects advances in the quality of material, improvements in fabrication technology and the development of sound design principles. The recent upsurge in GaAs IC 'foundaries' and the rapid drive towards GaAs LSI and VLSI technologies demonstrates the significant advances being made in these areas.

The quality of semiconductor material is fundamentally related to the performance of the final IC. For example, the uniformity of threshold voltage for enhancement mode devices is directly related to the number and distribution of dislocations and other defects in the substrate. A review by G.T.Brown of RSRE, at the 9th European Specialist Workshop on Active Microwave Semiconductor Devices, considered the effect of GaAs substrate quality on IC applications [36]. The paper reviewed the current understanding on the distribution of dislocations in semi-

insulating substrates and how they modify the distribution of point defects. Efforts to reduce or homogenise dislocation densities and the accompanying effects were also discussed. Crystal and wafer suppliers Sumitomo have addressed the problem of reducing the effects of dislocations. A GaAs–InAs mixed crystal process has been developed to produce dislocation–free crystals for IC substrates [37]. Lee et al of the Hughes Research Laboratories have similarly found that a small fraction of indium alloyed with the GaAs suppresses dislocations, resulting in greater uniformity of threshold voltage [38]. The presence of 'Non–Uniformity in In–doped/alloyed, semi–insulating GaAs' has been researched by F.Hyuga et al of the NTT Corporation [39].

High quality semi–insulating GaAs substrates are essential for GaAs IC production where direct ion implantation is used to produce the required doping structure. Ion implantation is usually used in IC fabrication as it has the advantages of good reproducibility, high uniformity, high yield and low cost. The yield and subsequent success of the fabrication process depends on obtaining high quality substrates with few defects. As the quality of semi–insulating substrates steadily improves, greater attention is being paid to optimising ion–implantation processes. The subject of arameter Control in Ion–Implanted GaAs Integrated Circuits' was discussed by K.R.Elliott (Rockwell International Corporation) at the 1985 GaAs IC Symposium [40].

The Massachusetts Institute of Science and Technology have been investigating the dependence of device performance on crystal growth and material parameters. MIT have been considering the Bridgman and liquid phase electro–epitaxy methods of crystal growth. They have found that stoichiometry is a fundamental factor affecting the structural and electronic properties of melt grown GaAs. This work has shown that deviations from stoichiometry govern dislocation density, concentration of point defects, related deep levels and the amphoteric behaviour of impurities. Sato et al of the Optoelectronics Joint Research Laboratory in Japan have investigated the effects of melt composition on the electrical uniformity of silicon implanted, undoped semi–insulating GaAs crystals [41]. This work considers the effect of melt composition on the carrier profiles produced by implantation. The results indicate that for a slightly arsenic–rich composition, it is possible to obtain very high uniformity in the peak value of the profile and smaller deviation in the range of the implant. It appears that it is also possible to make the impurity profiles sharper.

Rockwell International have recently reported improvements in the liquid enscaptulated Czochralski crystal growth technique, which has led to significant improvements in the quality and quantity of semi–insulating GaAs substrates produced using this technique. In particular, they claim to have achieved better control of wafer diameter and reduction in the incidence of twinning (which leads to changes in crystallographic orientation away from the required <100> orientation). Rockwell claim that wafers produced using this technique are suitable for LSI fabrication.

Heterostructure devices (HEMTs and HBTs) require molecular beam epitaxy (MBE) techniques to produce the very thin layers assocaited with these devices. D.Miller of Rockwell presented an invited paper at the 1984 GaAs IC Symposium on the subject of 'MBE materials considerations for HEMT Circuits' [42]. This paper described the optimization of the epitaxial structure to achieve high performance devices. It also stressed the importance of wafer uniformity and discussed the problems of wafer to wafer reproducibility. At present, the lack of production MBE equipment limits the development of pre-production prototypes, but the introduction of multi-chamber MBE systems will overcome this problem. HEMT technology also has several other production problems associated with it. Enhancement HEMT technology, like E-MESFETs, requires a very high degree of wafer uniformity because of problems of high channel resistance, threshold voltage uniformity and layer thickness control. The high degree of layer thickness control afforded by MBE minimises some of these problems, but sensitivity of the channel thickness to other process steps such as high temperature annealling and plasma etching can cause threshold voltage variations. Shibatomi et al of Fujitsu recently reported on improvements in MBE and associated HEMT technologies and predict high performance, high yield HEMT LSI circuits [43]. They expect to be able to achieve sub-nanosecond access times for 4kb static RAMs with one micron gate technology and two micron design rules. Heterjunction bipolar transistors (HBTs), fabricated from thin layers of GaAs and AlGaAs, have the threshold immunity characteristic of all bipolar technologies and have demonstrated switching times of less than 10ps, and may provide an alternative to HEMTs for ultra-high speed logic applications. However, at the present time HBT IC circuits have only been extended to relatively small groups of gates. The fabrication technology of HBTs is more complex than for HEMTs, and requires both ion implantation and MBE technology.

The drive towards very small device geometries for very high speed, high density integrated circuits has meant that electron beam lithography (EBL) techniques are increasingly used in place of established photolithographic methods. Production requirements and the increasing size of chips has led to the development of EBL machines with increasing write-areas. EBL techniques are essential for future sub-micron gate length technology - FETs with gate lengths of 0.2 microns have already been fabricated. The viability of creating 0.1 micron gate lengths will shortly have to be addressed if further speed improvements are required in the future.

Design rules for GaAs ICs are becoming established and many companies now offer foundry facilities. Advanced computer aided design techniques (CAD) are being developed, which are capable of accounting for the special characteristics of GaAs, which make the design rules differ from silicon. This work is particularly important for small-scale devices.

In the area of design and characterisation there has been significant collaboration between industry and research institutions such as universities. Examples of centres offering these services to the GaAs IC industry are to be found at Leeds University (Microwave Solid State Group), Sheffield University, Glasgow University,

Nottingham University, Cambridge and UWIST in the United Kingdom. In the United States, Universities at Illinois, Cornell, North Carolina State and Massachusetts Institute of Technology have extensive research programs aimed at improving the technology and developing accurate computer models for characterising small geometry GaAs devices. Japan has a number of universities which are investigating high speed GaAs devices. In particular, the Universities of Tohoku and Hokkaido have recently reported results on optimised design considerations for MESFETs [44] and high speed devices [45]. Cornell University have recently described a research project on the optimum design of MBE low noise monolithic amplifiers, carried out in collaboration with COMSAT Laboratories [46]. Sophisticated computer modelling techniques have been developed at Leeds University [47] and North Carolina State University, supported by UK and US electronics industry. Both groups have used two-dimensional finite-difference numerical models to examine the operational (dc and large-signal ac) characteristics of short gate length (sub-micron) GaAs MESFETs for MMIC and GaAs VLSI applications. The numerical models have being used to develop improved analytical models suitable for use in IC computer aided design applications. The two-dimensional simulations are also being used to study the effects of variations in device geometry and material parameters.

Integrated Optics

GaAs technology offers the possibility of producing completely integrated opto-electronic systems. Monolithic integration of light emitting sources and detectors with associated GaAs driver and receiver electronics will allow low cost, compact, reliable sub-systems to be produced for use with fibre optic communication systems. Honeywell have been investigating integration schemes to overcome difficulties associated with combining the fabrication requirements for opto-electronic components with electronic components. They have developed a technique for fabricating the AlGaAs light emitting diodes (LEDs) and GaAs detector diodes in recessed well structures on semi-insulating substrates. The electronic interface circuit is then fabricated using ion-implantated MESFETs on the surrounding semi-insulating surface. Fujitsu have developed a monolithic laser and driver circuit, capable of gigabit-rate modulation, with a 400ps turn-on time [48]. The circuit which consists of an AlGaAs/GaAs GRIN-SCH laser and a GaAs MESFET driver circuit on a semi-insulating GaAs substrate, exhibited excellent cw operating characteristics with a threshold current of 15mA and a quantum efficiency of 50%

Future fibre-optic systems will utilise GaAs IC technology to achieve 2 Gbit per second non-return-to-zero data rates, which will far outpace present 45 Mbit/second systems. It will be possible to improve the receiver performance of fiber-optic systems by using GaAs IC comparators to achieve better noise margins and sharper pulse edges. General Electric and the Harris Microwave Semiconductor Inc. are already developing high speed Manchester decoders are already GaAs IC technology [49], which can be used to simplify encoding and decoding of signals with improved accuracy for optical systems. General Electric and TriQuint Semiconductors Inc. have also been conducting research into the development of GaAS IC decoders for gigabit rate communication links [50].

Integrated opto-electronics research in Europe has been further stimulated by funding provided by the Research and Development in Advanced Communication-Technologies for Europe (RACE) program. Projects are being supported in both industrial and university laboratories.

The Future for GaAs Integrated Circuits

Gallium arsenide IC technology is developing rapidly, with semiconductor companies investing increasingly in this area. However, GaAs digital technology may still have some way to go before it is widely accepted by the electronics manufacturing industry. A recent presentation by R.W.Keyes of IBM, Yorktown Heights, USA, at the European Solid State Circuits Conference (ESSCIRC), indicated that whilst IBM are investigating GaAs technology, they do not regard it as a substitute for silicon high speed logic at this time [51]. At present no major breakthroughs are being reported for silicon technology, and although designers continue to make smaller and smaller geometries and higher packing densities, dramatic speed improvements for silicon ICs are unlikely.

Current research confirms that GaAs logic gates with gate delays of the order of tens of picoseconds, tens of micro-watts power dissipation and very wide operating temperatures are a reality, and that improvements in performance of one or two orders of magnitude are possible for digital computers and communications systems. As the technological aspects of GaAs ICs are resolved the implementation of GaAs IC technology will remain a market driven issue which will depend on the requirements for faster high performance systems. It is likely that GaAs IC sub-systems will find applications where their speed, power, temperature and radiation hardness can be utilized in conjunction with existing silicon technology, rather than as a complete substitute for it.

The projected rapid growth in the GaAs IC communications market for satellite receivers, fiber optic links, mobile telephones and data aquisition/processing will put even greater emphasis on the immediate need to resolve manufacturing difficulties. Improved packaging and testing techniques must be developed and the long term reliability of GaAs ICs assessed.

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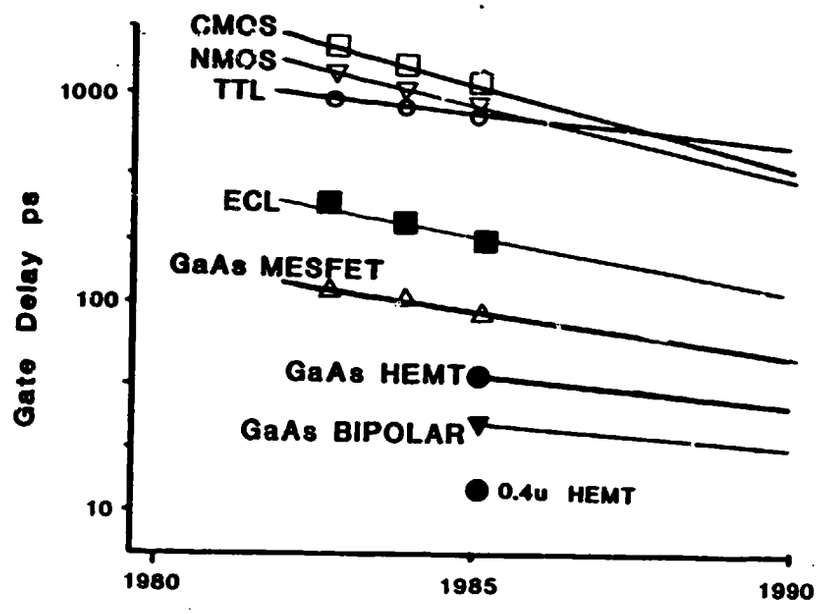
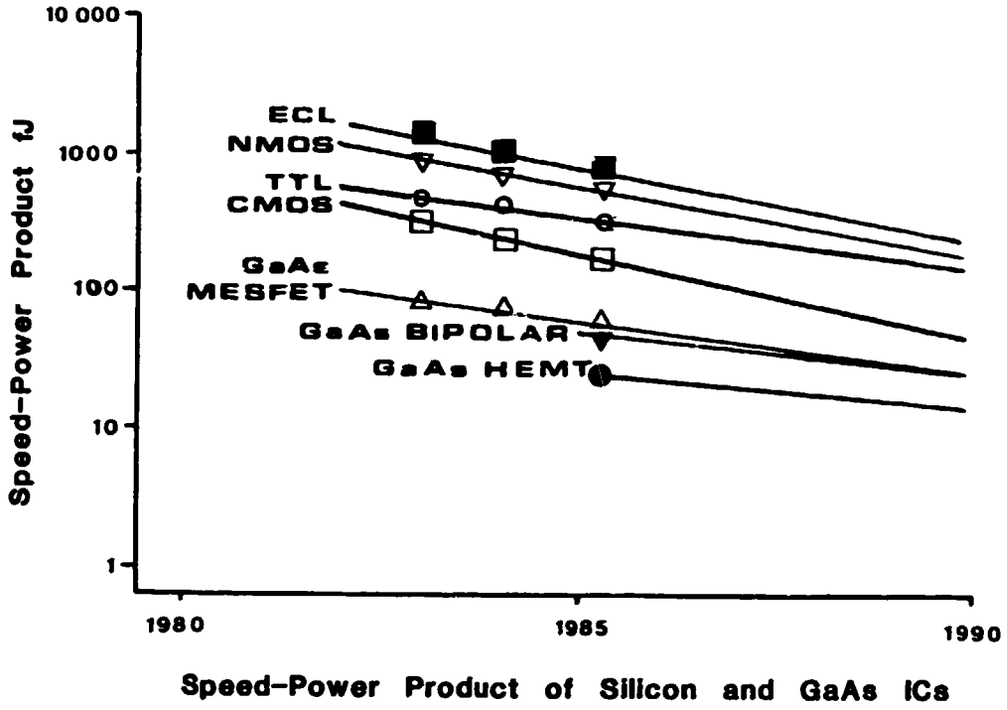


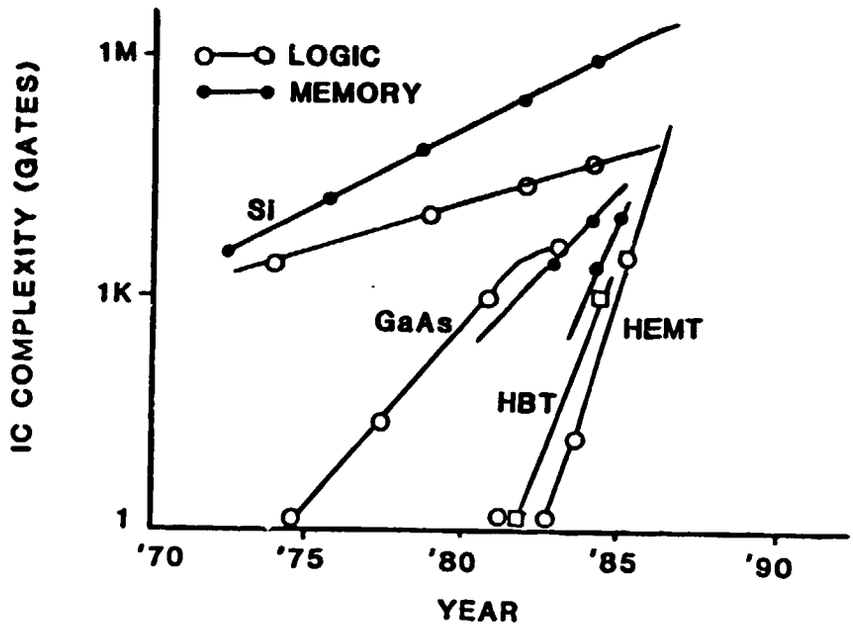
Speed comparison of silicon and GaAs devices

Fig.1



Speed-Power Product of Silicon and GaAs ICs

Fig. 2



IC Complexity of Silicon and GaAs

Fig. 3