OCCASION

This publication has been made available to the public on the occasion of the 50th anniversary of the United Nations Industrial Development Organisation.

DISCLAIMER

FAIR USE POLICY

CONTACT

Please contact publications@unido.org for further information concerning UNIDO publications.

For more information about UNIDO, please visit us at www.unido.org

UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION
Vienna International Centre, P.O. Box 300, 1400 Vienna, Austria
Tel: (+43-1) 26026-0 · www.unido.org · unido@unido.org

RESTRICTED

15191

DP/ID/SER.A/669
17 January 1986
ENGLISH

SEMICONDUCTOR DEVICES AND ELECTRONIC SUB-SYSTEMS FOR TRANSPORTATION

DP/IND/84/015

INDIA

Technical Report: Power Transmitter Devices for Transportation Equipment*

Prepared for the Government of India
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations Development Programme

Based on the work of H.B. Assalit
Expert in Power Semiconductor Devices

United Nations Industrial Development Organization
Vienna

* This document has been reproduced without formal editing.

V.86-50589

TABLE OF CONTENTS

ABSTRACT

This report summarizes the activities of the Consultant regarding the development of High Power Transistor Devices.

The project involvement includes several lectures on power devices, their characteristics, design and evaluation, assistance in improving present device designs and evaluation, and various discussions on power device related matters such as passivation, diffusion alloying, etc.

The present and future power semiconductor facilities were also evaluated.

Some recommendations have been included as part of the conclusion of this report.

1. INTRODUCTION

This consultancy assignment was established within the framework of the UNDP Project "Semiconductor Devices Electronic Sub-Systems for Transportation" (IND/84/015). Its purpose was to provide assistance to the Institute in research and development of power transistors for power control in electric drives for transportation.

Previous Consultants, namely Dr. P. Rai-Choudhury, from Westinghouse Electric Corporation, Pittsburgh, USA, and Prof. D.J. Roulston from the University of Waterloo, Ontario, Canada, had been already involved with this project. Dr.Rai-Choudhury had been involved in design, process and material related matters; while Dr. Roulston brought his contribution to the computer modelling aspect of transistor design.

The mission of the consultant was to provide assistance in improving the design available, contribute to its evaluation, and assist the staff members in their research wherever necessary.

The consultant arrived in New Delhi on November 7, 1985. After various meetings at CEERI Center and UNDP, the Consultant went to CEERI, Pilani where he arrived the same day.

The assignment at CEERI started on Nov. 7, 1985 for a period exceeding one month (Nov. 7 to Dec. 10, 1985).

2. PROJECT INVOLVEMENT

After discussion with Dr. G.N. Acharya, Institute Director, Dr. Amarjit Singh, National Chief Project Coordinator, UNDP Project and Dr. W.S. Khokle, Deputy Director, a work program was established. This program included the following:

- A series of lectures on power devices, their characteristics, design and fabrication,
- Assistance in improvement of present high power transistor design, assistance in process definition for power device fabrication, and assistance in testing and evaluation,
- Evaluation of power semiconductor processing facilities,
- Any further assistance as required by the members of the Institute.

2.1. Lectures

The lecture programme is given below:

Lecture - 1 - Review of present day
Power Semiconductor Devices,

Lecture - 2 - Thyristor Devices-Characteristics and Design,

Lecture - 3 - ASCR/RCT/GATT/GTO

Lecture - 4 - Thyristor Device Fabrication

Lecture - 5 - Lifetime Control in Thyristor Devices

Lecture - 6 - Power Transistors-Characteristics and Design

Lecture - 7 - Thyristor Testing & Evaluation

Lecture - 8 - Plasma Spreading in Thyristor Devices.

Besides these lectures, a series of meetings were held with some members of the Solid State Group to discuss subjects related to device processing and testing.

2.2. Assistance in Improvement of Present Transistor Design

Work on the development of a high power transistor device has been pursued at CEERI since July 1984. At present a particular transistor design with a current rating of 100A, and a voltage rating of 500 volts has been developed, and is being evaluated.

The Power Group is composed of scientists who have made good progress in developing this device, and the members of the team should be commended for their achievement.

There are however a few areas of concern at the moment. These are:

- Blocking capability and associated processing,
- Emitter contacting through patterned molybdenum shim,
- Molybdenum versus Tungsten,
- Switching speed and switching speed improvement,
- By-pass diode recovery speed,
- Packaging and associated process.

2.2.1. Blocking Capability

It was formerly demonstrated that the junction blocking capability satisfies the junction design and that good voltage can be achieved on diffused wafers.

The fact that the voltage capability deteriorates after further processing seems to indicate that one (or all) of the following processes is causing the deteriorations:

- Surface contouring for field control
- Final etch
- Passivation
- Alloying.

Surface contouring effects are being investigated by using smaller size particles for sand blasting (27 μ instead of 50 μ). It was also suggested to use 12 u size particles.

Final etch, which will eventually be done on a "Spin Etch" machine (not available yet), is now done in a static set up using a CP4 etching solution (5 x HNO_3 +3HF +3Ch_3COOH).

The etching operation takes about 5 minutes, there is a running DI water rinse at the end of the etching cycle. However, during the cycle, etching is done in steps with intermediate rinses in "Static" DI water contained in a beaker.

It was suggested to investigate the use of faster etch solution with only one etching step followed by a running DI water rinse (the etching solution is CPX-4 mix with 8 PTS nitric acid + 5PTS hydrofluoric + 4 parts acetic acid + 4 parts phosphoric acid).

Also suggested was the use of a caustic etch technique using potassium hydroxide solution at 95°C for 5 minutes followed by a 5 min. rinse in running DI water.

Note that in the first case, protection should be provided for the substrate and the cathode aluminum contact, in the second case, protection should be provided for the aluminum contact only.

The present passivation involves the use of a silicon elastomer (SSE from the Transene Co. USA). It is a satisfactory passivant for laboratory use, but other passivants would be more satisfactory for larger production quantities than those presently being processed.

RTV 11, by the General Electric Co., has been extensively used in high power device passivation and is a very reliable product. Other elastomers and resins have also shown satisfactory performance. Polyimide is a rather new material from DuPont-De-Nemours USA, or Rhone-Poulenc France, etc. which offers also great potential for junction passivation.

Alloying could effectively produce a deterioration of the blocking capability by creating stresses on the silicon.This possibility should be investigated.

2.2.2. Emitter Contacting

With the presently used planar technology, the emitter area has to be contacted through the use of a properly shaped molybdenum shim (see figure 1.).

Although the "Machining" by chemical etching of this shim is not a serious problem at the moment, it is felt however that, after reduction of the dimensions involved in the emitter design as it is being planned (350 µm finger width instead of 559 µm), "Machining" of the shim will become more difficult. Also as the device area increases a good alignement of the shim with respect to the emitter fingers presents more difficulty.

The solution to this matter could reside in the use of "Mesa Technology" (fig. 2b) instead of the present "Planar Technology" (fig 2 a).

With a mesa configuration, there is no need to use a patterned shim, and the emitter islands can be directly contacted by the "Strain Buffer" which is normally used as an intermediate member between the device and the package pole piece,

This technique requires perfect control of the etching operation used to produce the Mesa. The Power Group scientists should be able to develop this process.

2.2.3. Molybdenum versus Tungsten

The present device design involves the use of a molybdenum substrate to which the device is alloyed, or brazed, by means of a lead-silver- antimony preform. Although molybdenum is a proven material for power device substrate mounting, it offers the disadvantage of being attacked by the etching solutions normally used to perform the final etch operation on the silicon surface at the device periphery.

Since masking is not a convenient solution, one has to use a special machine (spin etch machine) to avoid the attack of the substrate by the silicon etch solution. This machine spins the device while the etching solution is distributed by jet on the silicon surface. If the rotational speed is sufficient, the etch can be kept away from the molybdenum substrate.

Tungsten is not attacked by the silicon etches, and therefore the use of such material simplifies the final etch process (Note also that tungsten matches the silicon better than molybdenum as far as thermal expansion is concerned).

It would be worthwhile to investigate the use of tungsten as an alternate material for device mounting (Note: This material should be "pressed and sintered")

2.2.4. Switching Speed

Although it was not possible to measure exactly the switching speed (turn-on and turn-off) of the few devices available, some measurements were made to evaluate the storage time.

It appears that the present device will have a rather long storage time at turn-off; too long to be compatible with high frequency operations of the kind found in PWM inverters circuits. Measurements of the lifetime in the collector region of the device have also indicated a high value for this parameter (8 to 12 μsec.)

There are three possible solutions to improve the switching speed of these devices.

The lifetime can be reduced in the collector region. This is a practical solution, above all if "Electron Irradiation" is available as a means of controlling the lifetime.

Since some characteristics are marginal, one may find out that the devices with lower lifetime are not capable of meeting some specifications such as gain and saturation voltage.

Providing a speed-up diode as shown of figure 3 is also a solution. The diode gives access to the main base of the device and allows to speed up the device saturation. On high power devices, the integration of this diode

is a difficult task, and the next solution could be preferred.

The third solution is simply obtained by an extra connection to the main base of the device as shown of figure 4. As above, this connection can be used to speed up the desaturation of the device. Note that if one wants to use only one electrode for turn-on and turn-off, then one can externally connect a speed-up diode between the two base connections(This would simplify the base circuitry). This solution is however difficult to implement mechanically.

At this stage of the project development, the first solution should be the preferred one. Due to the presence of heavy n^+ layers on both side of the device, gold doping for lifetime control might not be a satisfactory process. Electron irradiation should be the preferred method for controlling the lifetime in this application.

2.2.5. By-Pass Diode

The integrated by-pass diode (see fig 3&4) must be a fast recovery type diode. With the lifetime values measured in the collector of the transistor (8 to 12 µsec). This diode, which shares its own base with the collector of the transistor, will not achieve the required recovery speed.

Here again, lifetime control has to be provided to reduce the lifetime to levels compatible with the high speed performance required for this diode.

The lifetime required here may be too low to permit proper operation of the compagnion transistor. If this is the case, then the diode will have to be removed from the transistor chip, and provided as a discrete component connected across the transistor device.

2.2.6. Packaging

The present packaging parts have been provided by Westinghouse. These parts are available in limited quantities. It should be the task of CEERI to investigate other sources for their package parts.

The two main ceramic package suppliers in USA are: Latronics based on Pennsylvania, and Interceram based in New York.

Drawings and other pertinent information should be sent to these companies to obtain price and delivery information. The tooling cost should also be provided.

Assembly of the devices in their packages should be done by cold welding. A cold weld, press should be made available to CEERI.

3. EVALUATION OF POWER SEMICONDUCTOR FACILITIES

CEERI is now in the process of installing the power semiconductor

facilities required for processing high power devices.

Facilities of this kind can be generally divided into the following areas:

- Incoming Inspection
- Fabrication
- Process Control
- Assembly
- Surface Field Control
- Packaging
- Testing and Evaluation
- Supporting Facilities.

3.1 Incoming Inspection

The incoming inspection area should include all quality control operations performed on the materials when received from the material suppliers.

There are mainly three types of materials to be evaluated:

- Silicon
- Substrate
- Package Parts

Incoming inspection on the silicon material is generally limited to a verification of the resistivity, a control of the thickness of the wafer, and a control of the wafer diameter. The thickness of the epi-layer of epitaxial wafers could also be verified on a sample basis.

Incoming inspection on the other parts is mainly a visual inspection to detect the gross finish faults, and dimension verification.

The tools for incoming inspection are available at CEERI. Material specifications and inspection instructions should be established as part of the general engineering process instructions.

3.2. Fabrication

The fabrication area ("Fab" area) should include all equipment and essential accessories required for

- p-type Diffusion
- n-type Diffusion
- Oxidation
- Photomasking
- Metallization
- Chemical Treatment

3.2.1. p-type Diffusion

Diffusion furnace, quartzware and laminar flow station are already available. The evacuation system for closed tube diffusion has been ordered. The equipment available is being installed and should by operational in the

near future.

3.2.2. n-type Diffusion

Diffusion furnace, $POCl_3$ source system, quartzwave, and laminar flow station are available and under installation.

3.2.3. Photomasking

Spinner, first mask aligner, bake ovens, laminar flow station are available. A developer is available, but is not in use. There should be a fume hood installed with the spinner for evacuation of photo-resist fumes. A second mask aligner is required in this area. (A Kasper 2001 would be satisfactory.). Note that the photo masking area is rather limited, and all equipment described above cannot fit in the present available space.

3.2.4. Metallization

An evaporator and laminar flow station are available and in operating conditions.

3.2.5. Chemical Treatment

US cleaner, fume hood are available. There is a need for teflon, and polypropylene accessories. The fume hood is not working properly.

3.3. Process Control

All equipment required for process control such as spreading resistance apparatus, four point probes, thermo-electric probe etc. are available at CEERI. Note that the spreading resistance measuring equipment is out of order because of computer failure.

There is a need here for providing specific process control instructions.

3.4. Assembly/Alloying

With the arrival of a new vacuum furnace, the alloying area should be well equiped for this process. Alloying fixtures should be designed. A laminar flow station should be made available.

The selected, room might not be large enough to accommodate all equipment involved.

3.5. Surface Field Control

Bevelling/contouring machine, bake oven, and fume hood are available. A spin etch machine has been ordered. There is a need in this area for a passivation machine (which could be "Home-Made") and a laminar flow station.

3.6. Packaging

A laminar flow station, an old used wire bonder and an old used resistance welding machine, are available in this area.

The old wire bonder should be replaced by a new one with a capacity for 20 mils wire size (Orthodyne, for example), and the welding machine should be replaced by a cold weld press capable of welding the Ni plated copper

packages being used for the power transistor.

3.7 Testing and Evaluation

Transistor testing involves the measurement of the following parameters:

- a) Blocking voltages and leakages
- b) Current Gain
- c) Saturation Voltage
- d) Sustaining Voltage
- e) Safe Operating Area (Forward and Reverse)
- f) Switching Times
- g) Switching Losses
- h) Overload SOA
- i) Thermal Impedance

Items a, b and c can be measured at CEERI with the help of the available Tektronix Curve Tracer. Item f is on order from the LEM Company, Switzerland. The other items require some circuit design and construction, or require to be ordered. Safe operating area tester, and thermal impedance tester are commercially available.

Testing and evaluation are important tasks in a device development, and all evaluation equipment listed above should be made available.

3.8. Supporting Facilities

DI Water supply should be available in sufficient quantities to allow ample use of this element.

The present supply of DI Water should be updated to better quality. ($\geq$16 MΩcm).

Eventually the system should be upgraded to larger capacity.

4. CONCLUSION AND RECOMMENDATIONS

The following conclusions involves:

- Characterization
- Design and Process
- Facilities
- Trends
- Special Equipment

4.1. Characterization

Generally speaking, there should be more characterisation done on the present transistor design. The feasibility has been demonstrated, but further testing and evaluation are required to totally assess the capabilities of the design. There is a need for equipment in this area, but while waiting for equipment it would be worthwhile to build simple test circuits that could

be used for preliminary evaluation

As a first step towards characterisation, detailed specifications should be provided with all test conditions.

4.2. Design and Process

The present design appears to be satisfactory. The horizontal design could however benefit from the use of radial fingers in place of circular segmented fingers.

A mesa technology could offer some advantages when compared to the present planar technology.

There should be some investigation made regarding the use of tungsten instead of molybdenum as substrate material. An investigation should be started to evaluate the use of aluminum as the metal to be used for collector contacting to the substrate (this item was not dealt with in the bulk of this report, but it would be an important item in device processing).

Control of the lifetime should be provided to improve the switching speed of the device. Depending upon its recovery speed, the by-pass diode might have to be separated from the transistor.

Final etch and passivation techniques could be modified to accommodate the present day requirements. It is felt also that it would be beneficial to the overall performance of the project, if the processed quantities were at pilot production scale (25 or 50 devices per batch). This would allow better feedback concerning process control and repeatability, and could ensure a better technology transfer.

4.3. Facilities

As a whole the present and future facilities appear to be satisfactory. There is a need for more space in some areas (photo masking, alloying). A mask aligner, a cold weld press with its dies, and a wire bonder would be required to complete the facilities.The quality of the DI water and its distribution require improvement.

4.4 Trends

With the requirements described in Appendix I, there wil be a need for GTO type devices for the high voltage components (1500V, 1850V). Power transistors are not available with this type of voltage ratings and the development of such devices would require much effort without much change of success.

The low voltage rated device (400V) has a rather high current rating for a transistor device (660A) which could also be difficult to achieve; the combination of two transistors in parallel is of course a possibility, but the GTO could also be in this case a satisfactory solution device.

Except if equipment size is a limitation (as it could be in the case

of small battery operated vehicles), all three applications described in Appendix-I could use GTO devices.

Considering however the progress made in the present transistor design development, it would be wise to complete this project before working on the development of a GTO device.

There has been also some discussions about "Transistor Power Modules" as an alternate to replace" press-pack transistors". These rather new components are now much used in Japan and US industries, and should eventually become a major component in the Indian Power Conversion Industry.

Perhaps some studies should be started to determine the necessary requirements to develop such devices.

4.5. Special Equipment

Although the control of lifetime by gold doping has been a common practice for many years, it is recognized as being a difficult technique to handle, and it may lead often to production losses, or low yields.

High energy particle irradiation, now in use for more than 10 years, has been offering much better control and reproducibility than gold doping.

Although some trade-offs have to be sacrificed, irradiation appears to be the proper tool for lifetime control in power devices.

A satisfactory equipment would be a linear electron accelerator with energy level up to 12 MeV.

This machine could be also utilised for other operations such as medical product sterilization, food sterilization, resin hardening etc.

The possibility of making such machine available in India should be investigated.

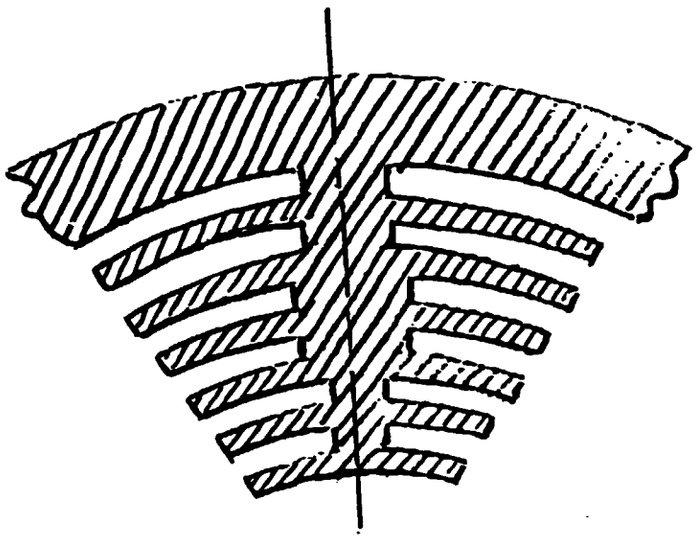

Fig 1. Emitter Contacting Shim - Approximate Shape
(≈ 1/6 th of the total area)

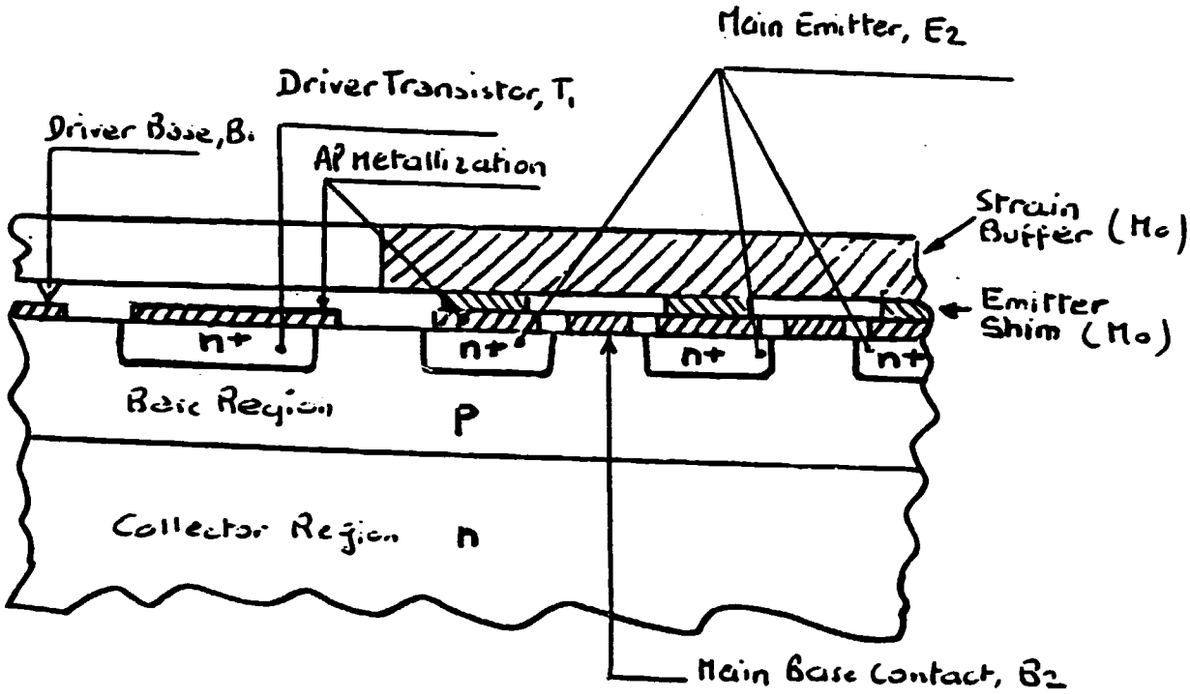

Fig 2a - Planar Technology

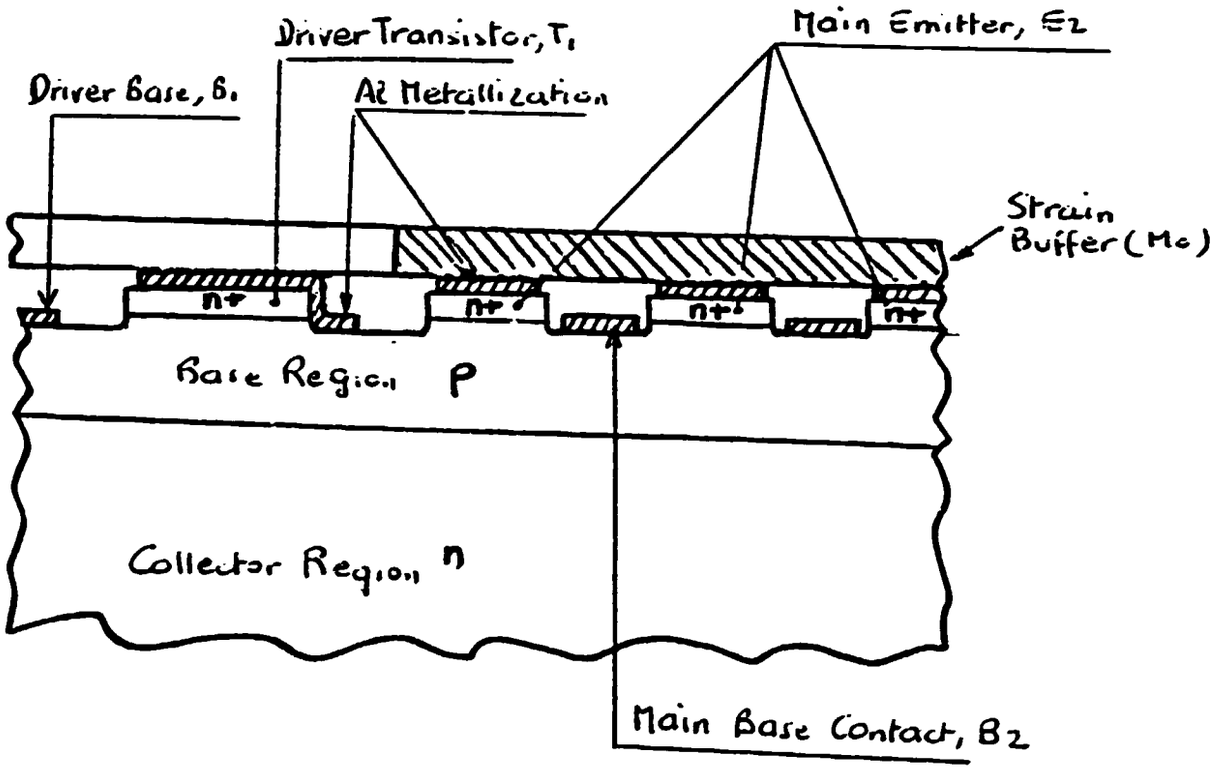

Fig 2b- Mesa Technology

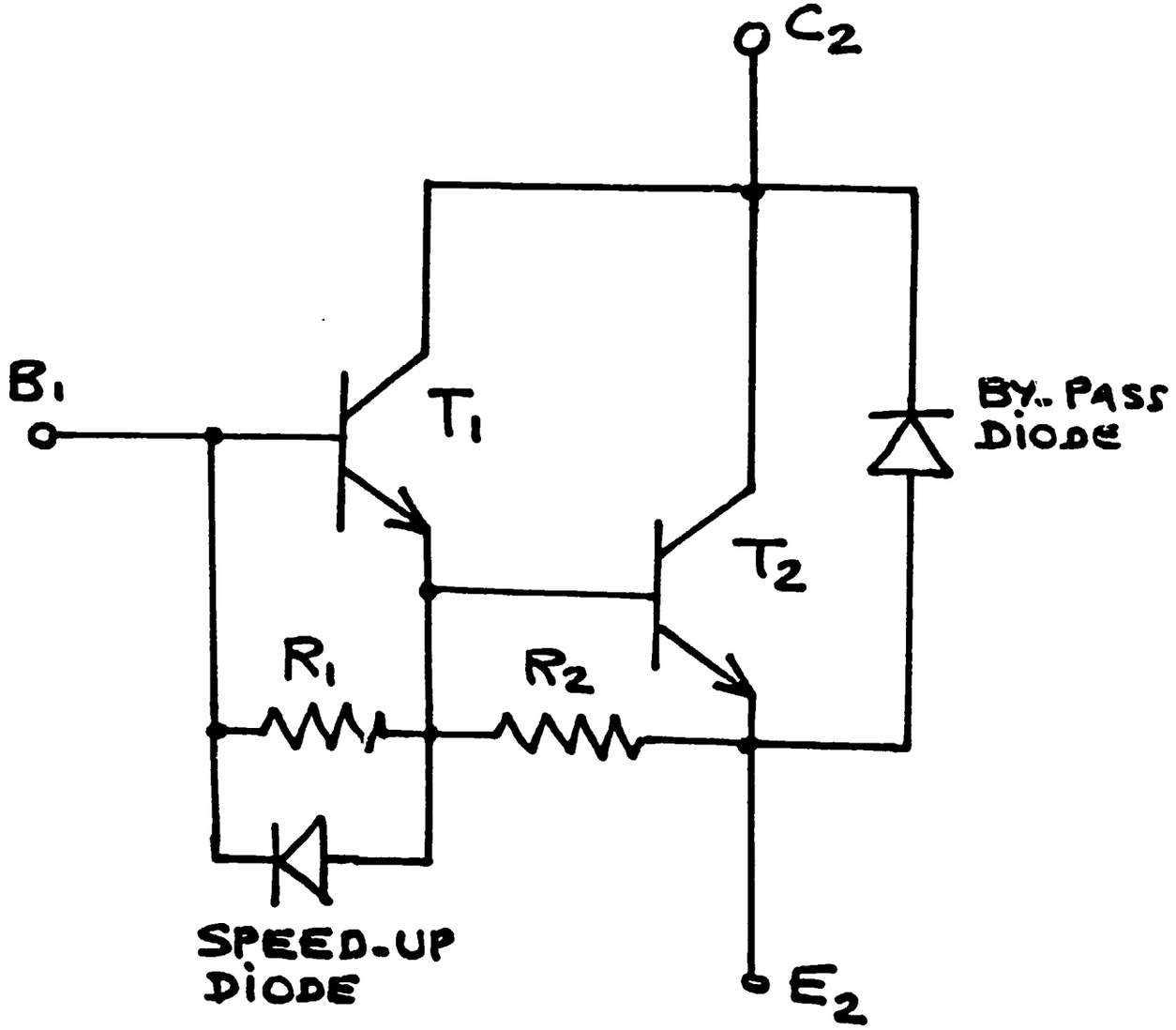

Fig. 3. - Speed-up Diode Connection.

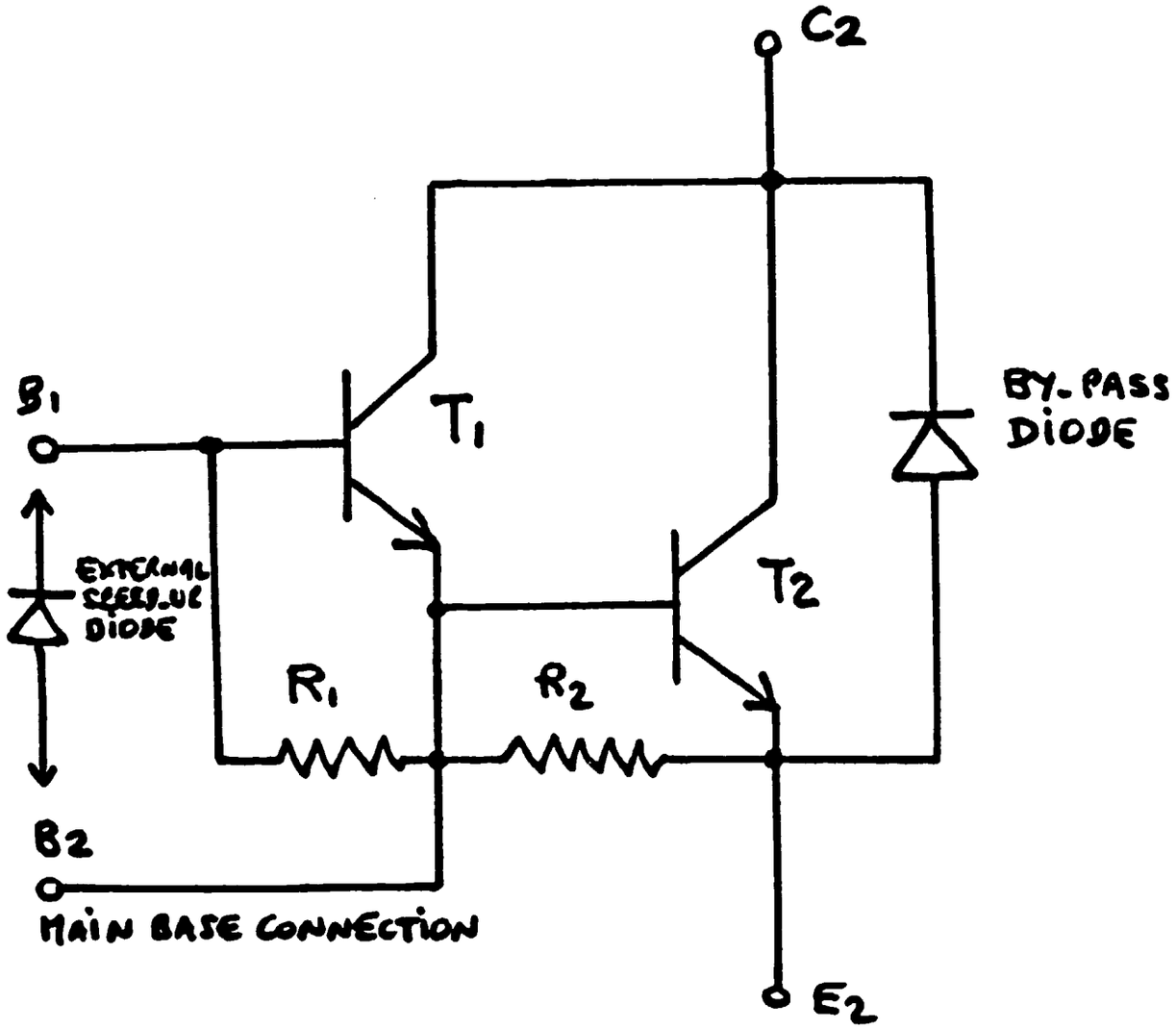

Fig. 4 - Additional main base connection.

POWER SEMICONDUCTOR DEVICE REQUIREMENTS FOR ELECTRIC VEHICLES

	Battery Vehiles upto 100 HP (Edc = 150 volts)	Trolley Buses Upto 100 HP Edc	Trolley Buses Upto 250 HP Edc
		600V	750 volts
Voltage Ratings	400	1500	1850
Continuous duty current Ratings	660 Amps. OR 330A ..Two Nos.	180 To 200 amps	250 Amps
Preferred Turnoff Times for PWM AC Drives	20 Microseconds		
On State Drop at Imax	Preferably less than 1.6 volts	Less than 2 volts	less than 2.5 volts