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INDIA

India.

Technical Report: Power Semiconductor Devices for Transportation Equipment (Part II)*

Prepared for the Government of India
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ABSTRACT

The present mission consisted of giving lectures, participating in discussions, initiating experiments, and a visit to potential user of the technology. A lecture was given on the theory and recent developments on gate turn-off thyristors (GTO). In view of the many application advantages, the development of this device in India should be considered. Discussions were held on various process steps needing further development. These include open tube Aluminium and gallium diffusion, epitaxial growth of high resistivity silicon, bevelling and junction passiviation, alloying, and testing of the 100 A darlington transistor. The progress to date on the process development is satisfactory and on schedule.

A number of improvements of the existing facilities were identified. Need for a mask aligner is quite urgent and appropriate equipment has been identified.

Visit to BHEL consisted of a seminar on GTO and discussion on a number of production problems. Detailed discussion was held on the status of 100 A darlington project and the facilities needed for its implementation in BHEL.

1. Introduction

The project is aimed at developing semiconductor devices and electronic sub-system for transportation. This includes four major tasks, which are power devices, hybrid circuits, monolithic integrated circuits, and inverters for the electronic subsystem. Prior to this mission the author visited CEERI twice under the present project. Significant progress has been made during this period. In the short span of about a year and a half, the power device group at CEERI has built up working capability from small mm size devices to relatively larger devices of several cm in diameters. The present mission was concentrated primarily on the issues related to process development and materials problems for the power device development.

The three tasks on which investigation has started are:

Task 1 : Design of 100 A Darlington Transistor
(Nov. 1984 - June 1986)

Task 2 : Fabrication of 100 A Darlington Transistor
(Feb. 1985 - Sept. 1986)

Task 3 : Process capability for Large (2 inch) Device
(Nov. 1984 - May 1986)

2. Design of 100 A Darlington Transistor

The design of the 100 A darlington has been modified to decrease the emitter width from 500 /um to 350 /um . This will improve the switching behaviour and thermal stability of the device. The mask layout for the new design is being fabricated. The epitaxial layer thickness has been changed to 90 /um as part of the design optimization.

3. Fabrication of 100 A Darlington Transistor

Processing of 100 A darlington transistors has been discussed and the following problem areas identified:

1. Low surface concentration of Ga diffused wafers at 970°C diffusion temperature.
2. Minority carrier lifetime improvement and control.
3. High reverse leakage current in bevelled collector - base junction.
4. Jigging for fusion testing.

In order to adjust the working point after base diffusion without having to etch the wafer a lower temperature gallium diffusion was attempted. Forty wafers have been diffused with gallium at 970°C. These wafers have surface concentration of 9×10^{17} cm^{-3} , which is considered too low. In order to salvage these wafers a boron reinforcement diffusion has been carried out using ten of these wafers. The diffusion cycle has been chosen to achieve the required base charge for the present design. These wafers are being prepared for the phosphorus emitter diffusion. Unfortunately, due to breakdown of the spreading resistance equipment the dopant profiles cannot be measured at CEERI. Selected samples will be taken to Westinghouse for profile measurement and results transmitted to CEERI within a few weeks.

Minority carrier lifetime enhancement during processing has been discussed. Precleaning of wafers and furnace tube using HCl gas before diffusion and oxidation has been suggested. At present the process is sufficiently under control to yield good carrier lifetime for the present transistor. However, further improvement in carrier lifetime for higher voltage devices is desirable.

Diffused wafers have been alloyed to molybdenum discs using two lead-silver-antimony preforms, each 2 mm thick. Prior to use, alloy preforms and lapped moly discs have been annealed in hydrogen at 800°C. Alloying has been done at 850°C and involves, slow (10°C/min) heating and cooling and a soak time of 3 mins. The present equipment has several limitations and results in reproducibility problems. Delivery of a new vacuum furnace is expected in the near future. This furnace should provide satisfactory process control for the alloying operation. In the meantime, four wafers are being alloyed in the present furnace for analysis of bond integrity and voids. These wafers will be examined at Westinghouse using ultrasonic void detector.

Ten fusions have been fabricated up to alloying and are ready for bevelling. The bevelling and passivation operation will be completed as soon as the process is optimized. Experiments with bevelling have been carried out with previously processed fusions. Bevelling using the air abrasive system with 50 /um aluminium particles produces surface damage. Inadequate etching of this damaged layer due to the unavailability of the spin etcher has resulted in to leaky junctions. Experiments are being conducted using 10 /um alumina particles, air pressure, speed of rotation, bevel angle, powder flow etc.

The high reverse leakage problem is suspected to be due to inadequate removal of the surface damage and is expected to be solved as soon as the bevelling process is optimized.

Four fusions have been completed by perforating the alloying and passivation steps at Westinghouse, and are ready to be tested. A new fixture has been designed and fabricated for testing the device. It is undergoing some modifications and should be available for device testing in the immediate future. In order to package these fusions cold welding facilities are normally used. Due to a lack of such facilities resistance welding will be attempted as soon as equipment is modified and tested.

4. Process capability for large (2 inch) Devices

Process capability of large diameter (2 inch) devices is near completion. Open tube diffusion, sintering furnace, sealed tube diffusion, all these facilities are being installed. With the additional equipment, such as, vacuum alloying furnace, spin etcher, varian tube sealing system etc. which is expected to be delivered in the near future, large device processing capability should be adequate within the next six months. There are some items needing attention, however, that will be discussed under 'Materials, Devices and Equipment'.

5. Materials, Devices and Equipment

A number of items in the materials category need some attention. CEERI has been unable to obtain any quotation for the epitaxial silicon wafers from Wacker Chemitronic. Attempts will be made to persuade Wacker to supply CEERI with wafers. Since we have a significant data base on their material it is not advisable at this time to change supplier. Also the quotation on moly discs, 1.5 mm thick, 33 and 40 mm diameter, will be expedited from USA. These moly discs are needed for the fusion fabrication. Also packaging specifications for 33 mm and 40 mm devices will be discussed with the vendor and quotations obtained. All the above materials items will be expedited by the author on his return to the U.S.A.

Two types of darlington transistors and two types of GTOs have been identified for purchase to provide the power electronics group with experience in using these new devices for inverter applications. Characterization and analysis of these devices will also be very valuable for the power device group in designing future devices.

Regarding facilities requirement, a suitable mask aligner is needed for the power device group that can handle large diameter wafers, is able to align both front and back of wafer and is efficient to operate. Such an aligner has been identified and information given to CEERI. The power device facilities area also needs a super Q system to raise the quality of the D.I. water to 18 mega ohms. Epitaxial silicon reactor has not been operational for quite some time for lack of rectangular quartz reactor tube with appropriate end caps. It is an important item that needs to be purchased. Other accessories for the epitaxial system that are needed are an improved RF coil, a laminar flow bunch, and substrate silicon wafers.

6. Lectures and Discussions

A lecture was given on the theory, design and fabrication of GTO. Some of the points covered in the talk were current status, turn-off processes, design considerations, device geometry, working point optimization, device fabrication and recommendation. This device has the advantages of both thyristor and transistor. Unlike thyristor, GTO does not require commuting circuits and therefore has lower losses. The manufacture of the device is however, complicated because of fine geometry and requires seven or more masks. The details of the process are available at CEERI.

A talk was given on the trend of power devices and comparisons made between transistors, thyristors GTO and other emerging devices. Some of the major points are summarized below.

Transistors are levelling off at 1200V, 200-300A. At 400 V/300 A darlington is a preferred device (GTO has higher V_F). Darlingtons are used for electric vehicles and in aircraft power. FET's will switch faster but not needed for low frequency operation. Trends for transistor development are for higher voltage (1600 - 2000V), higher frequency, integration, modules and stacks. In comparison with transistors, power MOSFET's have major application at 120 V/60-100A. At higher voltages ($\sim$ 1000 V) only low current (4-6A) devices are available.

Thyristor development is levelling off at 4-6 kV. Trend is towards larger size ($\sim$ 5" devices). Fast switching thyristors are being replaced by GTO's. Thyristor development is being carried out in the areas of light triggering, self protection and high current (i.e. large area).

Gate turn-off thyristor (GTO) is a rapidly developing device. Fabrication of this device requires fine geometry control and clean room processing. One of the primary reasons for the take off of this "old device" is the availability of superior lithography and VLSI related process developments that have taken place. The trend for the GTO development is towards higher voltage (4.5 KV - 8 KV), higher frequency (2 kHZ - 5 kHZ, 10 kHZ), reverse conducting, integration, module, light triggering and snubberless devices. Current increase has been levelling off at about 2500 - 2700 A. In comparison, static induction thyristor (SIT) looks like GTO and the only advantage over GTO is its high dv/dt capability. A typical SIT has a turn off current of about 600 A, 300 A (RMS) and has high forward drop. The device is normally on, and V_{AVAL} is reverse bias sensitive.

It is recommended that the GTO would be the next important device after darlington (for low voltage applications only) that should be developed in India.

A number of discussions were held on current problems and their solutions, in particular, detailed discussions were held on open tube diffusion of gallium and aluminium, surface passivation and epitaxial growth of high resistivity silicon.

It is often difficult to control the working point and the surface concentration during gallium diffusion by the sealed tube method. Open tube gallium diffusion that allows control of surface concentration over a fairly wide range has been developed elsewhere. It is recommended that CEERI workers investigate the possibility of developing the process capability for open tube gallium. Sealed tube aluminium diffusion often results in the degradation of carrier lifetime in silicon. An open tube diffusion technique that uses hydrogen as a carrier gas and Al_2O_3 di-s as the aluminium source gives relatively high minority carrier lifetime.

At the present development of this process in CEERI is not recommended in view of other items of higher priority.

Surface passivation is very important for reliable operation and stability of power devices, and the critical issues of the passivation process were discussed. The role of primary passivation layer to reduce interface states and the secondary passivation layer to protect the surface against mechanical damage were discussed. Other active and passive roles of the dielectric layers were also outlined. Thermal oxide is generally not used for passivation of high power devices, because of drift effects and high fixed charge density. Details of a number of important organic passivation materials (elastomers, polymers and copolymers) were discussed. Some passivation material was brought from the United States for use at CEERI. Surface preparation prior to application of the polymer material and the polymer itself are significant factors in determining initial device properties, and device stability.

Availability of high resistivity thick epitaxial silicon is very important in the fabrication of darlington transistors. For this an in-house capability, particularly for India, is important. In order to obtain high resistivity, thick epitaxial layer one must have an ultraclean dedicated system that will produce about 100 ohm-cm (n-type) material which can then be doped down to 50 ohm-cm or so. The substrate must have a built-in gettering capability such as back damage, enhanced, or intrinsic gettering. Substrate surface must be very carefully prepared to avoid growth spikes. High temperature hydrogen firing, as well as, HCl etching prior to epitaxial growth should be attempted; hydrogen firing might be preferred. These above issues have been discussed in detail with the CVD group.

7. Task Summary

The design of the 100 A darlington transistor has been further improved through computer modelling that includes narrower finger width and high emitter efficiency. New mask sets are being fabricated in CEERI.

A number of processing steps need further optimization. These are sealed tube gallium diffusion, bevelling and passivation. All these problems are being investigated actively. Several devices have been fabricated up to the passivation step, and expected to be completed soon. Four devices from a previous process have been successfully fabricated, and attempts are being made to package and test them.

For the fabrication of large area wafers, a number of equipment items, such as, diffusion and sintering furnaces, bevelling machine, and laser sutter equipment for silicon to device dimension are being installed. Remaining equipment for spin etching, alloying, tube sealing, press for testing and dynamic tests are expected early in 1986.

8. BHEL Visit

Visited BHEL, Bangalore, a production organization for interaction on power device development work. Discussions were held with Dr. E.S. Ramamurthy and his group. A seminar was given on GTO, a rapidly emerging power device. The technology was reviewed including design and fabrication of the device. BHEL expressed keen interest in the device because of its many applications advantages. A detailed discussion was held to assist them in solving some of the processing problems, in particular, device stability in reverse blocking and lifetime control.

The status of the darlington transistor development activity was described and various process steps were explained. Possibilities of packaging these devices in PHEL were explored.

9. Conclusions and Recommendations

Work on the design and processing of the 100 A darlington transistor is on schedule. Significant progress has been made on the process development. Work to date has resulted in a number of completed fusions awaiting testing. Process development for bevelling and passivation is needed. Work is somewhat handicapped due to the unavailability of the spin etcher. Lack of adequate D.I. water supply and wafer handling materials limit the batch size to five or six wafers, which is insufficient for process optimization. Procurement and installation of the remaining equipment are proceeding without any unexpected delay.

The following recommendations are being made to strengthen the capability of the group for timely completion of the project:

1. Super Q System is required to raise the quality of the D.I. Water.

2. Mask Aligner is needed to handle Large Diameter Wafers with provisions for Back Side Alignment.

3. Selected accessories for the epitaxial system are to be purchased in order to get it operational.