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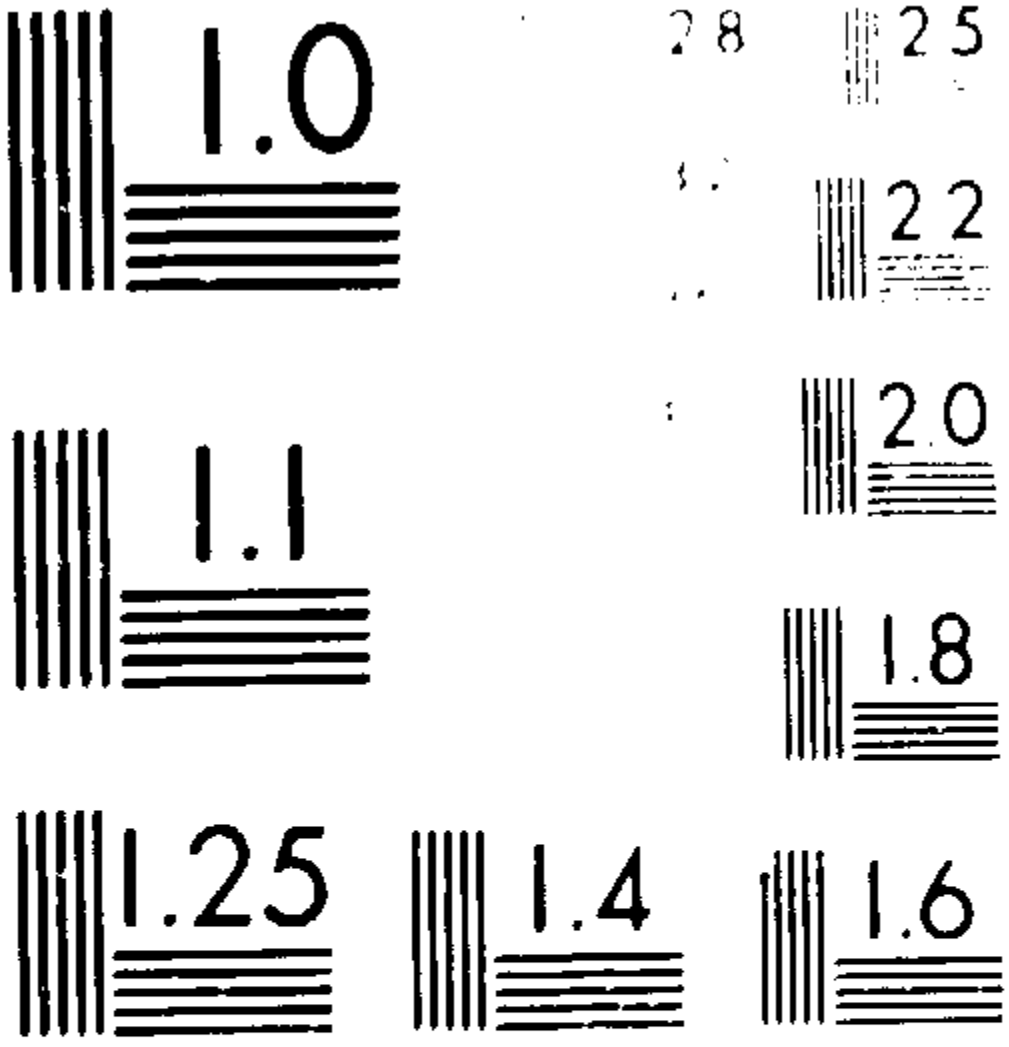
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5 November 1982
English

India.

IMPROVEMENT OF TESTING AND EVALUATION FACILITIES - NATIONAL TEST HOUSE, CALCUTTA

DP/IND/75/040

INDIA

Technical report: Improvement of environmental and reliability test facilities at the National Test House, Calcutta *

Prepared for the Government of India
by the United Nations Industrial Development Organization
acting as executing agency for the United Nations Development Programme

Based on the work of Geoff Bone,
expert in environmental testing of electronic components

United Nations Industrial Development Organization
Vienna

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Explanatory notes

During the period of the mission the value of the Indian Rupee in terms of U.S. dollars was as follows (UN Operational Exchange Rate)

February	1982	8.85	Rupees per dollar
March	1982	9.15	Rupees per dollar
July	1982	9.21	Rupees per dollar

Information was not available for rates of exchange earlier in the project but it was assumed to be about 8.0 Rupees per dollar.

In this report NTH is used as the common abreviation for the National Test House, Calcutta.

Abstract

Title of Project - Improvement of environmental and reliability test facilities at the National Test House, Calcutta.

Project number - DP/IND/75/040

The purpose of the project was to improve the environmental test laboratory and to set up a failure analysis laboratory in the field of electronic components. The length of the mission was six months.

In the initial period the requirements were determined and recommendations made to NTH regarding the failure analysis laboratory which have been accepted, and are being acted upon. Some preliminary training was given. Best use could not be made of the UNIDO expert due to lack of suitable equipment at NTH.

Recommendations were made with a view to improving the overall effectiveness of NTH.

Assistance was given with preparations for the introduction of Phase II in October 1982, and recommendations made.

Introduction

The Government of India realised in 1973 that there was a need to strengthen and improve the testing and evaluation facilities at NTH Calcutta in respect to the quality and reliability of electronic components with a view to helping the expanding electronic component industry within India.

Some previous work of a fairly simple nature had been done in this field by NTH.

In 1973 as a result of a circular from UNDP/UNIDO, the Government of India requested aid for a wide range of specialities which were the responsibility of the NTH Calcutta, a part of the Ministry of Supply and Rehabilitation. The Project Document for Phase I was submitted 13th September 1976, it was approved by the Resident Representative UNDP 28th September 1976. It's scheduled starting date was January 1977 and the duration was to be two years. The project is still proceeding and is not expected to be completed before December 1982. The mission being reported on began in February 1982 and lasted for six months. The Govt. co-operating agency was the Ministry of Supply and Rehabilitation.

The original UNDP contribution was $ 301,500. In February 1982 $ 473,478 had been spent with another $ 103,000 allocated. The delay in implementing the project and the subsequent cost escalation of equipment was the main cause of the increased cost.

The contribution of the Govt. of India originally amounted to Rs.1,227,700 ($ 153,500), all of which was in the form of personnel, buildings, and equipment.

The original project document objectives for the mission were to provide facilities for vibration measurement and analysis for electronic components, and other environmental testing systems for the environmental laboratory at NTH. As well as providing equipment UNDP were to provide the services of a foreign expert in this field for a mission period of eighteen months from July 1977, and to provide training abroad in this field for one NTH officer for a period of six months from November 1977. Due to poor co-ordination between UNDP and NTH little progress was made in the implementation of the project. The six months training period was changed to a two months foreign orientation tour for the Project Co-ordinator which took place in March, April and May 1979 (See Annex I). As a consequence of this tour the Project Coordinator suggested at the Tripartite Review Meeting, May 1980, that the expert's specialisation should include the failure analysis of electronic components. This was agreed, the expert's job description was revised, and the duration of the mission reduced to six months. The revised objective of the mission was to strengthen the capabilities of NTH in evaluation of electronic components by organizing and setting up a failure analysis laboratory in the field of electronics at NTH, Calcutta. This has only been partially achieved due to the lack of suitable equipment which limited training to mainly theoretical considerations. However recommendations were made regarding space, equipment and staff for the failure analysis laboratory. The mission objective of organising and setting up the Failure Analysis laboratory was one of five separate specialities chosen by NTH for strengthening

and improvement in the overall project. (Phase I). It was expected that the improved facilities and equipment would enable NTH to develop the necessary expertise which in turn would assist industry to achieve an improvement in quality and reliability. This would in the long term help promote exports and reduce imports in those fields.

In October 1982 Phase II, Project DP/IND/82/007/A/01/37, UNDP Input $1,500,000 is scheduled to begin for a duration of three years. Concern by UNIDO and UNDP that the mistakes and lack of progress evident in Phase I should not be repeated in Phase II resulted in request that time should be spent to ensure NTH's preparedness and fitness to undertake the new Phase. It was thought by all concerned that this work should receive priority. A total of six weeks has therefore been spent in organising this aspect.

An informal workshop course which comprised nine sessions was run at NTH for suitable staff. This was not as successful as hoped due to lack of suitable equipment which meant the practical content was low. Considerable interest was however generated in a small group which augers well for the future.

In this mission all the work was done by UNIDO.

Details of International staff are shown in Annex II and Senior counterpart staff in Annex III.

Recommendations

1. If the NTH is to regain any of its former esteem the cleanliness of the buildings and its facilities must be improved, and when improved, maintained.

Action NTH.

2. It has been accepted that poor co-ordination between UNDP and NTH was responsible for the lack of progress of Phase I. This is only partially true, a share of the responsibility must rest with the poor internal communications which exist at NTH. The management of NTH must rectify this, it will take time, it will cost money, it is necessary. It should be remembered that they are running a scientific organisation with over seven hundred employees. The Govt. of India must provide them with good modern office and communication facilities which are the tools of management.

Action by NTH and Govt. of India.

3. At present there is no central system to ensure that test equipment is calibrated at the appropriate intervals. In an organisation like NTH the aims of which are to act as a calibration and test house of national stature there must be a central organisation responsible for this within NTH with full audit authority.

Action NTH.

4. The incidence of breakdown and non-availability of test equipment is too high. The causes of this which may include poor storage conditions, misuse, effect of power cuts, or lack of maintenance must be determined and action taken. The rectification of faulty equipment takes too long and ways must be devised to speed it up.

Action NTH.

5. NTH must make more effort to contact industry and to inform potential customers of the facilities available if good use is to be made of them. In short they must sell themselves, they must not sit back and wait for work to come to them. One senior officer should be given responsibility for this. Some thought must be given to good modern presentations which would inspire confidence in the client.

Action NTH.

6. Co-operation between NTH and the UNIDO expert has in general been good, however there have been occasions when information has only been available after repeated requests. For future experts to achieve their objectives there must be a greater willingness at all levels to impart information.

Action NTH.

7. UNDP to retain title to the equipment supplied to NTH.

Action NTH.

Recommendations for Phase II

1. NTH must adopt a more systematic and professional approach to the management of the Project. There must be close control over all documentation with any changes or variants authorised only by the Project Co-ordinator. There must be good internal communications so that there is a clear and completely unambiguous outline of the duties and responsibilities of NTH staff concerned with this Project.

Action NTH.

2. There must be close and effective co-ordination between UNDP and NTH for the successful execution of Phase II. There will be times when NTH will want guidance and advice. As well as visits by UNDP to NTH Calcutta, it also calls for visits by NTH to UNDP Delhi. At present the Project Co-ordinator is not authorised to travel by air. It will be essential for effective co-ordination of this Project that the time and tedium involved in rail travel be reduced by the use of air travel. In Phase II the most critical job is that of the Project Co-ordinator, he must get full support if the Project is to succeed.

Action UNDP, NTH & Govt. of India

3. With the current frequency of power cuts in Calcutta and the intermittent use of standby generators, it is essential for the wellbeing of electronic equipment, both existing and to be procured, that no damage is caused to the equipment. It will not be good enough for professional engineers just to sit around and talk about it, some practical work must be done, and an investigation started to measure voltage variations and transients. It must take into account periods when other existing test equipment such as high voltage testers are being used.

Action NTH.

4. The UNIDO fellowships abroad are an important part of Phase II, they are equally as important as the supply of equipment. It is to be hoped that the result will be not just a gain in experience but that the fellows will benefit by the "culture difference" and that on their return NTH will benefit. It is recommended that during the selection of candidates that some emphasis is given to their personal qualities so that the most receptive and observant are chosen to benefit from the experience. On their return their comments and observations should be put into action.

Action NTH.

I. ENVIRONMENTAL AND RELIABILITY LABORATORY

A. Objectives

To assist in improving existing environmental and reliability testing facilities and to extend its scope to meet the growing needs of industry and science.

B. Activities

Most of the equipment is old and with the exception of the UNDP input, is incapable of meeting the demands imposed by modern specifications.

The equipment requirements more determined and suppliers were with difficulty contacted.

The UNDP input to this laboratory was equipment for vibration testing of electronic components and equipments, the cost was $ 25,000. Details are shown in Annex IV. The Government of India input comprised a bump test machine, three environmental test chambers for heat, humidity and dust, and a cold test chamber. These were items from the existing set up and is the equipment referred to above. The value was $ 11,000. A new climatic chamber has been ordered by NTH through the Government of India Plan at an approximate cost of $ 38,000, delivery is expected early 1983.

C. Findings

It is considered that there is sufficient space available in the present laboratory to house new equipment provided the old equipments are removed. The existing area is not air-conditioned or temperature controlled, this will be necessary otherwise the ambient temperatures will be too high for efficient operation of new equipment. It was found that NTH staff were working independently to upgrade the laboratory equipment, and one item, the climatic test chamber was ordered without any reference to the UNIDO expert. While NTH staff are perfectly free to do this it does indicate a lack of co-operation on their part. It would appear that the objectives will be achieved by NTH albeit slowly without any further need of UNIDO/UNDP assistance.

II. FAILURE ANALYSIS LABORATORY

A. Objectives

To assist and advise on setting up of the failure analysis laboratory in NTH.

B. Activities

An initial report was prepared and issued as Annex I to the Preliminary Report of this mission dated 26th March, 1982. It contained recommendations for space, equipment and staff. (Annex VI). Equipment

suppliers were contacted, replies and quotations were received from some and recommendations of suitable equipment made to NTH.

A suitable area is being converted into a failure analysis laboratory in accordance with the recommendations in the report.

There has been no material input by UNDP for this laboratory. The Government of India have provided space and facilities and intend to provide equipment and staff. The equipments will be procured in 1982-83 through the Government of India plan.

C. Achievements

The objectives for this section of the mission have been achieved i.e. assistance and advice has been given, accepted, and put into operation. It will however be the end of 1983 before the laboratory is fully operational due to the delay in getting equipments, it should however be capable of fairly simple investigations by early 1983.

D. Utilization

It is thought that for electronic components it will take time for the work load to build up, at present the work load cannot be estimated. The main item of equipment in the failure analysis laboratory would be the scanning electron microscope (s.e.m.) complete with energy dispersive X - Ray attachment for chemical analysis. This would also be regarded as a central item for materials investigation covering the whole field of NTH's work, and its utilization would be quite high once its capabilities become widely known.

III. STAFF AND TRAINING

A. Objectives

To make recommendations on staff and staff training and train counterpart personnel.

B. Activities

Recommendations on selection of staff were made in Annex I of the Preliminary Report of this mission dated 26th March 1982. A workshop on failure analysis of electronic components was held in April 1982. It comprised nine sessions each of two hours duration. A copy of the syllabus and course notes are included as Annex V to this report.

Due to the lack of equipment and the unavailability through breakdown of existing equipment, it was not possible to do much practical work and the "workshop" therefore was mainly of a theoretical nature.

The workshop started with ten members, at the end the numbers were down to six, all of whom had attended most of the sessions.

C. Achievements

A few people who had no prior knowledge or experience of failure analysis of electronic components were initiated into this field. In some cases considerable interest was generated.

D. Utilization

There is a danger that if the laboratory is not completed quickly that the interest will fade.

IV. TECHNICAL SEMINARS

A. Objectives

To conduct technical seminars for specialists in reliability engineering and "failure analysis" of electronic components.

B. Activities

This was partially covered by the workshop course mentioned in Chapter III.

A half-day seminar on "Reliability Testing and Failure Analysis with particular reference to electronic components" was held in Calcutta in July 1982. It was convened jointly by NTH and the All India Radio and Electronics Association (Eastern Zone). The programme is shown in Annex VII. Approximately thirty people attended, half of whom were from outside NTH.

C. Findings

The amount of interest shown at the seminar although not excessive was encouraging. The use of colour slides was well received, and these together with practical demonstrations should form an essential part of any future seminar.

V. CO-ORDINATION WITH OTHER PROJECTS

A. Objectives

To co-ordinate activities at this project with those of other existing projects in this field in the country.

B. Activities

Comments were made in the Preliminary Report of this mission dated 26th March 1982. Little contact was made with other organisations as these are in the Defence field which makes for difficult communications apart from the inherent difficulties which apply to normal communication in India.

PHASE II

A. Objectives

To advise and assist in the organisation and planning to ensure its eventual smooth introduction and operation.

B. Introduction

In February 1982 Mr. V. Ivanov, UNIDO Vienna, requested the UNIDO Expert to help whenever possible with the preparation at NTH for Phase II. In May 1982 both Mr. A. Krasiakov and Mr. T.R. Maakan UNDP Delhi made a similar request in order to avoid the chaotic situation which marked Phase I.

Phase II is bigger than Phase I. The UNDP input is $1,500,000 of which $1,007,500 is for equipment while the training of Indian Nationals will account for $294,000. The training will consist of two study tours by the National Project Director (the Director General of NTH) and the National Project Co-ordinator (Associate Director of NTH) each of one and a half months duration, six study hours by senior scientists for one month each, and twenty one UNIDO Fellowships for working scientists each for six months. The training will take place in Europe and/or the USA. Phase II covers the Chemical, Physico - Mechanical, and Electrical/Electronic disciplines. The services of four UNIDO Experts for a period of six months each are required.

The scheduled date of commencement is October 1982 and its duration will be for three years.

C. Activities

The Project Document was examined and a realistic workplan was produced.

Frequent discussions were held with the National Project Director which covered all aspects of the management and organization of the project. Meetings have been held with Mr. M.J. Priestley, UNDP Resident Representative, Mr. T.R. Maakan, UNDP Programme Officer, the National Project Co-ordinator and the UNIDO Expert. A number of aspects of the organisation and management of the project were discussed.

To ensure delivery of equipment in a reasonable time scale and to minimise cost escalation some equipment (cost $ 302,000) was ordered in June 1982 through UNDP and it is expected that by the end of July 1982 another $ 200,000 of equipment will be ordered.

Several foreign consulates in Calcutta have been contacted as a source of information for suitable establishments for study tours and fellowships.

D. Findings

The discussions held with NTH were fruitful. They highlighted a number of weak areas which must receive attention. It is the considered opinion of the UNIDO expert that the time spent doing this has been well worthwhile, and as a result it is thought that NTH will now be able to organise and execute Phase II in a reasonable manner.

Annex I

Fellowships awarded

Awarded to Mr. B.P. Ghosh, Joint Director, NTH, in November 1977. Field of study was environmental and reliability testing of electronic components and equipments. This was done in the United Kingdom for two and a half months from March 1979 to May 1979.

Annex II

International Staff

UNIDO Expert - GEOFF BONE
British
Expert in failure analysis, environmental and reliability testing of electronic components.
UNIDO service 31st January 1982 to 30 July 1982.

Annex III

Senior counterpart staff

National Test House - Dr. S.R. DAS
Director-General
Applied Physics
Joined NTH as Director-General
in December 1979
was National Project Director for Phase I.

- MR. B.P. GHOSH
Joint/Associate Director
Applied Physics
Joined NTH 1962
Was National Project Co-ordinator
for Phase I.

Annex IV

Equipment provided by UNIDO/UNDP

The major item supplied in connection with the work of this mission was -

Sine wave vibration testing and measurement equipment, manufactured by Bruel and Kjaer, Denmark.

The approximate cost was $ 25,000. The order was placed by UNIDO September 1977 and delivered Calcutta June 1978.

Annex V

WORKSHOP ON FAILURE ANALYSIS OF ELECTRONIC COMPONENTS

SYLLABUS

Session I	April 1st 1982
	Introduction
	The application of failure analysis
	The basis of failure analysis. Materials
	Interaction between these materials
	The effect of above on electrical parameters
Session II	April 5th 1982
	Techniques of failure analysis
	Examples of failure modes and mechanisms
Session III	April 7th 1982
	Introduction to electronic components
Session IV	April 12th 1982
	Techniques of opening components.
Session V	April 14th 1982
	Electronic component families
Session VI	April 16th 1982
	Electronic component families (continued)
Session VII	April 26th 1982
	Simple electrical measurements
	"Reverse" engineering of integrated circuits

....(ii)

Annex V (contd.)

(ii)

Session VIII	April 28th 1982	"Reverse" engineering of integrated circuits (continued)
Session IX	April 30th 1982	Factors affecting component reliability.

Annex V (contd.)

WORKSHOP ON FAILURE ANALYSIS OF ELECTRONIC COMPONENTS

Introduction

The purpose of the initial part of the Workshop is to provide a gentle introduction to modern electronic components. The approach taken will be to describe them in terms of materials and their combinations rather than by their electronic functions. This is the best approach for a multi-disciplinary group as it provides a good materials background for the electronic specialists while supplying a gradual exposure to simple electronics for the non-electronics people. This workshop is not perfect nor complete, it is designed around facilities currently available in the National Test House, Calcutta. Later parts of the course will deal with the techniques of Failure Analysis starting with simple visual examination and basic electrical measurements then dealing with some of the more sophisticated techniques.

Over the last 30 years the Electronics Industry has seen an increase in the complexity of both components and equipment, an increase in packing density, and in more exacting requirements. All of these demands can be met but normally at the expense of decreased reliability. However there has been a parallel demand for increased reliability. On the whole all of these demands have been satisfied. This has been achieved by many simultaneous improvements in different fields, e.g. there have been better and cleaner manufacturing facilities, there has been an awareness of the importance of environmental test facilities (reflected in the sophistication of modern component specifications), the introduction of semi-conductor technology has resulted in lower voltage and temperature stress levels, and the replacement of analogue by digital systems are just some of the contributions which have helped. Above all however has been the availability of high quality and more reliable electronic components.

In the 1950's discrete electronic components were evaluated by subjecting the components to the applicable standards and by large scale life tests. Failures were often rejected without further investigation and there was a general feeling that some failures were inevitable. Indeed some Quality Assurance Groups went to great length to show statistically that there would be always be some failures and that this would have to be accepted.

In the 1960's the integrated circuit became available in quantity and it was soon apparent that the previous approach of large scale testing was not economically viable and a new approach was evolved. This resulted in the introduction of step-stress testing where a

smaller number of components were successively tested at increasing temperatures until failure occured. It was at this time that Failure Analysis as we know it today began. It was introduced on both economic and reliability grounds. Failure Analysis of defective components revealed the failure mode e.g. cracked semiconductor chips, metallisation defects, broken bonds etc. This approach was by necessity a post-mortem operation. The speed with which integrated circuits evolved from Small Scale Integration (SSI) to Medium Scale Integration (MSI) to Large Scale Integration (LSI) meant that a new approach had to be used. In failure analysis there was an evolution too, this was in response to a demand that it should be possible to forecast the possible causes of failure enabling their elimination. This was achieved by the failure mechanism approach, this uses a model which accounts for the chemical and physical changes that take place in the component resulting in failure.

At this stage it is useful to define some of the terms used in this field. Failure Analysis is the name given to the systematic investigation of an item to determine the particular failure mode (cracked semiconductor chip etc.). The means by which the failure mode occurs is the failure mechanism, this may be for example, thermal stress causing a cracked semiconductor chip). The overall name given to what is now a recognised discipline is Reliability Physics, and its aim is to provide a sound physical base for understanding the degradation processes that occur in electronic components and so cause poor reliability.

The application of failure analysis

The usefulness of the results of a failure analysis investigation will vary between component manufacturer and the component user. To a component manufacturer the determination of failure mechanisms in his products will enable him to,

1. devise more effective process controls and screening methods to improve both yield and performance;

2. Gain valuable background experience for the modification of existing products and the development of new ones;

3. calculate failure rates with confidence over a wide range of stress-time conditions;

4. predict the reliability of a component during the design stage.

When the determination of failure mechanisms is done by the component user, they will enable him to distinguish between,

1. components made defective by his own design faults;

2. components made defective by his own mishandling and assembly faults;

3. defective (or potentially defective) components being supplied to him by a component manufacturer.

He is thus able to determine the cause of failure and to allocate responsibility for it.

It should be noted that failure analysis investigations are often carried out on good components. Different manufacturers of an identical item (or items meeting identical specification) can be compared, this often reveals marked differences which could affect their long term reliability.

The 'Basics' of failure analysis

This consists of a knowledge of:

1. Materials and processes used in the manufacture of electronic components.

2. The interaction between these materials during manufacture, test, storage, and service.

3. The effect of the above on electrical parameters.

4. A knowledge of investigation techniques.

Materials

Examples of materials used in electronic components are -

Metals - used for electrical conduction or resistance;
- used for their thermal conduction properties;
- used for their mechanical/structural properties;

e.g. in the packaging of components.

Ceramics
- used for electrical insulation, especially at high temperatures,
- used for good thermal conduction,
- used for their dielectric properties, e.g. in capacitors,
- used in packaging.

Plastics
- used for electrical insulation,
- used for their dielectric properties, e.g. in capacitors,
- used in packaging.

Other
- Carbon, used for conduction in resistors and capacitors.
- Silicon for semiconductors,
- Silicon dioxide, used for electrical insulation and protection purposes,
- Paper, used in capacitors,
- Liquids, sulphuric acid is used in capacitors, some organic liquids used as impregnants for capacitors.

Interaction between these materials during:

Manufacture - the most common cause of interaction is the effect of heat. Some reactions such as diffusion between two dissimilar metals which will be extremely slow at room temperature will be accelerated at a higher temperature. Apart from chemical reaction there can be mechanical stress caused by differential expansion caused by heat.

The effect of pressure can be a problem. It is known that silicon is a brittle material, in semiconductor manufacture excessive pressure during the thermocompression bonding of gold wires to the silicon chip may cause cracks, these will be propagated by heat.

Test - applied voltage may trigger some electrolytic action, especially if there have been errors in the processing e.g. incomplete cleaning after chemical reactions. Often in these tests a much higher voltage than the normal rated voltage is used. This higher voltage may initiate dielectric breakdown which may cause subsequent failure of the component.

Annex V (contd.)

Storage - the effect depends upon the storage conditions. If moisture is present together with a change of temperature (e.g. heating during the day and cooling at night) this can cause moisture related problems of corrosion. If the components are not hermetically sealed moisture ingress is possible leading to failure when a subsequent voltage is applied.

Service - in service the component will experience variations in voltage, extremes of temperatures, humidity, vibration, shock, variations in air pressure. All of these may have some effect on the combinations of materials which comprise modern electronic components.

The effect of the above on electrical parameters:

The result of interaction between materials is to ultimately affect the way in which electricity is affected in the conductive and resistive modes. Excessive interaction will result in the failure of an electronic component and this will usually fall into the following categories:

Degradational failures, where a gradual change in electrical properties occurs with time, this may be either a positive or negative change. This may be due for example to the oxidative effect of heat causing changes in resistance through removal of a conductive material and due to an electro-chemical reaction removing tiny amounts of a resistive film. Degradational changes in semiconductors can be caused by the interaction of small quantities of surface contaminants which have an advance effect on such parameters as leakage current.

Catastrophic failures, these are usually indicated by either opencircuit or short circuit conditions. Some examples are, poor wetting of the chip attach alloy in power transistor chips which results in poor thermal conduction resulting in overheating of the chip and eventual electrical short circuiting. Electrical overstress can cause metallic electromigration leading to both short circuit and open circuit depending upon whether metal is deposited or removed. Other examples are the effect of heat on the reaction between gold bonds on aluminium bonding pads of semi-conductors. The resultant porous alloy known as 'plague' can result in the failure of the bond joints causing an open circuit condition.

It should be by now clear the contribution each disciplins can make to a failure analysis group drawing upon their own specialist knowledge. It cannot be emphasised enough that time and time again the good failure analyst has to go back to "basic" and ask very simple questions such as "what happens when I heat/cool it does it effect the expansion, dielectric properties, surface tension, viscosity" and so on. In failure analysis basic simple questions like these have to be continually asked, they are essential.

Techniques of Failure Analysis:

It is important that this investigation is carried out in a methodical manner with a logical sequence of events, with as much information as possible being extracted from each step, and destructive steps left to the last.

A typical approach to a semiconductor defect investigation is shown below - it is also with modifications applied to passive components.

a) Before anything is done as much information as possible should be gathered regarding the defect, its previous history, how long it has been in service, the way in which it was used, how was the defect detected.

b) The defective component should be visually examined, for obvious signs of damage poor workmanship, contamination. All markings such as date codes etc. should be recorded. A low power stereo-microscope up to x30 is ideal for this.

c) The component should be X-rayed at this point - this will in the case of gold bond wires, show loose bond wires, crossed bond wires and also voids in the gold-silicon alloying below the chip. Other defects may be indicated such as the presence of foreign matter.

d) A preliminary functional electrical measurement is carried out at this stage to confirm the fault. This may be done using both automatic test equipments or fairly simple ones such as a curve tracer. At this stage, it may be necessary to use both high and low temperature or other environmental conditions to simulate original equipment conditions and so reproduce the fault. Much useful information is obtained at this stage, e.g. is it a catastrophic or degradation fault, is it intermittent, temperature or shock dependent.

There are differing opinions regarding which should be done first, the X-ray or the functional test, with good arguments for either side.

e) The next stage is to check the semiconductor package for hermeticity, for both gross and fine leaks. The presence of a leak would indicate the presence of moisture in the package with adverse effects on the aluminium metallisation of the chip.

f) At this point if suitable equipment is available a PIND examination is done. This is Particle Impact Noise Detection and is a method for the detection of loose particles inside the package. The component is mounted on a shaker (1-15g, 14-60 Hz) and as the particle hits the case high frequency (100 kHz or higher) stress waves are generated and detected.

Also at this stage a Residual Gas Analysis may be done to establish the nature of the atmosphere in the package, and hence the type of any contaminant which may be present.

g) Opening the component, IC packaging falls into three main types, round metal cans, ceramic packages and plastic encapsulated devices. The metal and ceramic are to be found in military or professional quality components, and plastic for the commercial ones.

The round metal cans, e.g. TO-5 can be opened by holding the can in a small bench style lathe and cutting the metal with a hacksaw. The metal cover on metal-ceramic dual-in-line packages is conveniently removed by careful grinding using wet and dry paper.

Ceramic dual-in-line packages are opened either by careful grinding of the cover or by cracking the ceramic adhesive with a sharp edge, i.e. by a sudden shear shock.

Plastic packages provide the greatest challenge for the investigator. Many methods exist ranging from hot fuming nitric acid to various solvent blends. Thermal decomposition of the plastic may be used. However the temperature at which this happens is about 400°C therefore on silicon chips with gold bonds "plague" will be present. A possible method being investigated is that of Plasma Etching, which has the advantage of low temperature thus avoiding "plague". A thermal shock method has been used which has been quite successful.

h) After opening, the chip is visually examined, first with a low power stereo microscope up to x40 magnification for bond integrity, soundness of alloying between chip and package, and for the presence of obvious contamination.

Higher power examination is always done with a metallurgical microscope with illumination thro' the objective lens and normal to the chip surface. The chip is examined for such defects as cracks, metallisation faults and such signs of electrical stress as flash-across-shorts and open circuits in the metallisation.

At this point it may be appropriate to examine the device using a Scanning Electron Microscope. This has the advantage over the optical microscope of much higher magnification and also greatly increased depth of field (up to x300 better). When coupled with chemical analysis equipment such as an X-ray energy dispersive system, minute quantities of contaminants can be detected.

i) If precise micromanipulators are available it is possible to isolate particular parts of the chip for electrical measurement. These instruments are fitted with a metallurgical microscope which has special long working distance objectives.

j) At this stage it may be necessary to remove some of the different layers on the chip and to follow this up by etching of the surface. This will reveal the different n and p areas of each individual transistor on the chip. If all the stages of this work have been photographically recorded it makes the work of identification and understanding of the device much easier.

k) Finally, it may be necessary to section the device to show diffused regions or bond sections.

There are a number of specialised techniques available which can be used at the appropriate time. These include the use of Infra-Red to determine voids in the alloying between chip and case or crystal dislocations in the chip.

Liquid crystals have been used to indicate temperature variations across the chip.

The previous notes indicate the depth of investigation which may be necessary to obtain sufficient information to obtain the correct failure mechanism.

Annex V (contd.)

Examples of failure modes and mechanisms:

A number of examples covering different aspects of a range of electronic components will be discussed, including the following:

Power transistors, diodes, ceramic, polycarbonate and tantalum capacitors, and integrated circuits.

Introduction to Electronic Components:

At this stage we can regard electronic components as just combinations of materials which have a particular effect upon the flow of an electric current. Some will conduct it easily, others will resist it to a greater or lesser extent and some will show a tendency to store it. Combinations of materials have been designed which can switch it or amplify it. We can therefore at this stage define an electronic component simply as "a combination of materials in a suitable package which will give a desired electrical performance".

In order to avoid what could be a chaotic situation with different component manufacturers producing different products of varying size and performance, standards and specifications for components were agreed upon, usually by committees comprising representatives from both manufacturers and users. Such bodies are the Indian Standards Institute, the British Standards Institute, and the International Electrotechnical Commission. The purpose of such standards is to ensure interchangeability of components from different manufacturers and to provide an appropriate level of quality and performance. There are basically two levels or standards of performance, one is the ordinary or commercial standard, the other is a professional or military standard capable of withstanding the greater demands made by the more vigorous conditions of use. There is generally only one component specification to cover both levels of components, the professional and military types are subjected to more tests and a higher level of screening particularly environmental testing.

Annex V (contd.)

As stated above the purpose of specification is to ensure a uniform and "appropriate" level of quality and performance. Note the use of the word appropriate. Conformance with a specification does not guarantee a perfect product, it only promises a good probability of "fitness for use". These last three words form the best and simplest definition of quality, and is a little simpler than "the totality of features which bear on a product's ability to satisfy the requirement" which is the official European definition. Some people often confuse quality with reliability. The definition of quality makes no reference to the performance of the item with time. When we talk about an item being reliable it implies fitness for use over a period of time. The BS 4778 definition of reliability is "the ability of an item to perform a required function under stated conditions for a stated period of time." During the course of its life an electronic component will encounter a variety of environmental conditions, e.g. heat, cold, humidity, low air pressure, vibration, shock, as well as the normal handling involved in equipment manufacture such as solder heat and cleaning solvents. The main protection against such hazards is good basic design of the component, careful choice of suitable materials, and by the correct choice of packaging.

Recent years have seen an increase both in the severity and number of environmental tests which are included in the electronic component specifications. This reflects the wider use of electronic equipment for outside purposes. The normal approach is to have a general environmental test specification covering the whole range of different environments with different degrees of severity for each test appropriate to the different levels e.g. commercial or military. For situation where highly reliable components are required e.g. in space application, a number of additional screening tests are instituted. Some effects of environmental testing are shown in Table No.1.

Techniques of opening components

When opening an electronic component for investigation it is important that the least amount of damage is done. The technique used will obviously vary with the particular packaging style. The following list shows the range of packaging which may be encountered,

resistors and capacitors - plastic encapsulation,
hermetically sealed metal cans.

Annex V (contd.)

transistors and diodes	-	plastic encapsulation, hermetically sealed metal cans, glass encapsulation.
integrated circuits	-	plastic encapsulation hermetically sealed metal cans hermetically sealed ceramic

It will be seen from the above list there are three basic types of component package, each of which presents its own opening problems, plastic, metal, and ceramic.

The hermetically sealed metal can is easily opened by cutting open with a fine metal saw or cutting open using a lathe. It may sometimes be necessary to grind it open using grinding papers. Care should always be taken to avoid the interior of the component being filled with abrasive debris. Generally speaking it is better to open a metal can by a tearing action rather than by a grinding action as less loose particles will be produced to contaminate the component. In the case of transisters and integrated circuits the cut should be made as close to the bottom flange as possible. This will enable the whole can to be removed without damage to the semiconductor chip and, more important, it enables high magnification microscope objective lenses (which normally have a very short working distance) to be brought close to the chip surface thus enabling high magnification observation to be made. To open dual-in-line (DIL) ceramic packages with metal lids the normal approach is to grind away the metal lid until it is very thin. It will be found that as the metal of the lid gets thinner it will "bow" and the outline of the chip cavity will easily be seen. This is the convenient time to puncture the lid with a sharp point (e.g. a scalpel blade) and the lid can be easily peeled away (a tearing action). The principle of this technique can be successfully adapted to a number of metal packaged component.

A similar grinding technique is used with ceramic packages. With ceramic DIL packages it is possible to open them using a quick shearing technique between top and bottom parts, this method however always result in damage to the bonds and occasionally to the chip itself. It may be useful as a quick method of opening if the only objective is to check metallisation geometry etc., but for normal failure analysis it is not recommended, careful grinding although it may be tedious is the only way.

Annex V (contd.)

Table No. 1

SOME EFFECTS OF ENVIRONMENTAL TESTING

Test	Effect
Cold	Mechanical stress due to contraction will show poor adhesion and bonding
Dry heat	Mechanical stress due to expansion will show poor adhesion and bonding. Also thermal interaction of materials.
Temperature cycling (Rapid change of heat)	Will expose package sealing defects, cracked semi-conductor chips and substutes, also poor bonding and adhesion.
Damp heat	Sealing defects in packaging will allow penetration of moisture to cause corrosion.
Shock and bump	Will expose poor mechanical design and workmanship.
Vibration	As for shock and bump, it can however be much more searching and damaging.
Acceleration	Exposes poor adhesion and weak bonds.
Mould growth	The supporting of mould growth could cause short circuiting in humid conditions between components or conductors.
Low air pressure	Outgassing of volatiles may occur.
Soldering	The heat of soldering will include rapid thermal stress.
Resistance to cleaning solvents	Will determine the effectiveness of package sealing and marking
Flammability	Will determine if a potential fire hazard exists.

Annex V (contd.)

The plastic encapsulated DIL components present the greatest challenge to the analyst. As the plastic used is usually an epoxy-novalac (very highly crosslinked for high temperature stability) or a silicone material, the choice of solvent is very limited. A number of claims are made for proprietary mixtures of solvents but in the author's experience they are not really satisfactory. Effective solvents are either hot fuming nitric acid or hot concentrated sulphuric acid, the latter being the more easily handled and just as effective. At temperatures of 220°- 230°C a brief immersion in concentrated sulphuric acid for about 20 seconds will remove approximately 0.005" to 0.008" of epoxy. It is therefore best to remove most of the plastic by dry grinding until only this thickness remains, or until the metal bonds appear in the resin. It is important to keep both the component and sulphuric acid completely free from traces of moisture otherwise corrosion of the aluminium metallisation will occur. Another technique is to oxidise the resin by heating in air at 400°C for one to two hours, the resin will be carbonised then oxidised leaving behind the inorganic filler which can be gently brushed away. The disadvantage of this method is if gold bonds and aluminium metallisation are present then Kirkendall reaction on "plague" will occur between these metals. This may mask any previous reaction which may have been the original cause of failure. A better and less harmful technique is to use a plasma etch process. It is done at normal temperature so "plague" is not induced (it only occurs over 220°C). The process is slow, it takes about two days, however it is generally accepted to be about the best method for most investigations. Its principal disadvantage is the probable effect on any contamination present on the chip surface. A recent method which allows investigation of freshly exposed surfaces is by the use of a thermal shock process. By a careful grinding preparation the point is reached where a few seconds heating of the metal lead frame on a hot plate (300°C) will result in thermal stresses causing a separation of the semiconductor chip from the adjacent plastic encapsulation. It is a good method when surface contamination of the chip is involved as there is no further contamination during the investigative process. It results in two clear surfaces ready for examination, one the semiconductor chip and the other is the moulded surface impression of the chip in the resin. The latter will resolve all the surface details of the former. It has the disadvantage that it removes the bonds so that subsequent electrical tests are not easily done.

Electronic component families

The similarities and differences of a range of components will be discussed together with typical failure modes. These will be selected from :

Resistors, fixed	-	carbon film, metal oxide, metal film wirewound, cermet.
Resistors, variable	-	as above.
Capacitors	-	mica, paper, plastic film, ceramic, tantalum.
Diodes	-	SCR's, whisker type.
Transistors	-	Small signal, power.
Integrated circuits	-	linear, digital
Hybrid circuits	-	thick and thin film hybrids

A number of previously prepared examples including sectioned specimens and photographs will be examined.

Important features of component construction will be discussed including for example, dimensional differences in the construction and subsequent thermal dissipation of power transistors, the variation in geometry of the same type of integrated circuit made by different manufacturers and the effect on their reliability. Examples of thick and thin film hybrids will be available and their manufacture described.

In this section the emphasis will be on describing failure modes and showing how a knowledge of the component materials and their properties and interactions can lead to a deduction of the failure mechanism.

Use will be made oa a metallurgical microscope for examination of specimens.

Simple electrical measurements

These will be done on a variety of components and will depend upon the availability of equipment.

"Reverse" engineering of integrated circuits

In silicon integrated circuit manufacture after the diffusion stages there are a number of steps in the process which involves the interconnection of the diffused regions by metallic tracks and the deposition of insulating and protective layers of silicon dioxide. In failure analysis of integrated circuits there are occasions when it is necessary to chemically remove these layers in order to expose the diffused regions of the integrated circuit chip. The difference between the 'n' and 'p' regions can be visually emphasized by use of a suitable chemical etch which idfferentiates between the n and p doped silicon. This process is often referred to as "reverse" engineering. If each stage is recorded photographically it is possible to superimpose a tracing of say the fully etched diffused regions on top of a photograph of the normal metallised chip using tracing paper on melinex overlays. If a circuit diagram is available it helps towards a full understanding of the arrangement of the circuit.

The use of this technique will be demonstrated, and samples of identical integrated circuits will be progressively etched so the various stages can be examined with the metallurgical microscope.

Factors affecting component reliability

The curve shown in Figure 1 is the plot of failure rate (λ) against time. It is commonly known as the "bathtub". This curve applies equally to mechanical or electronic equipment. It is self explanatory, the early life failures give a failure rate which is meaningless as it is normally decreasing rapidly. These early life failures are the ones effective screening tests will detect. The useful life from t_1 to t_2 has a constant failure rate and this is the one used in reliability calculations. It is usually expressed as percentage failures per 1000 hours. Another way of expressing it is Mean - Time - Between - Failures or MTBF, this is expressed in hours and is the reciprocal of the failure rate.

In Figure 2 we have a diagram showing a typical integrated circuit and various aspects of the component which have an effect on the reliability are shown. They will be briefly discussed

Marking : This is a feature many people take for granted. The marking should be permanent, resistant to solvents, and should withstand normal handling. It tells us a great deal about the component, who makes it, whether it is military or commercial grade, when it was made, and also if it has been subjected to special screening

tests. This is vital in formation when a faulty component in an equipment has to be changed.

Applicable tests are a visual inspection, and resistance to cleaning solvents.

Package : a ceramic or metal package will provide the best protection to a semiconductor device. A plastic package will not give a hermetic seal, and moisture will always penetrate. It will do this because of thermal mismatch between the plastic encapsulation and the metal leads will cause minute gaps to open up between the leads and the plastic.

Applicable tests are temperature cycling, and leak tests.

Seal : The efficacy of the glass seal of a ceramic package will obviously effect the hermeticity of the device. The leads are normally made from Kovar alloy, a cobalt-iron-nickel alloy which allows a close watch in expansion characteristics with glass to avoid stress.

Applicable tests are again temperature cycling and leak tests.

Leads : they should be of a metal which is compatible with the package system used, they must not corrode, and should be capable of easy soldering even after a prolonged period of storage. If not then poor soldering which gives rise to dry joints may occur, which will cause unreliability.

Applicable tests are solderability.

Die attach medium : This material has to conduct both heat and electricity well. If voids are present then the dissipation of heat is decreased and there is the danger of overheating with subsequent failure. It also has to be capable of withstanding temperature cycling, shock, vibration. Gold-silicon alloys and silver loaded epoxy resins are the main ones used although soft solders are used for some power transistors.

Applicable tests are temperature cycling and acceleration.

Annex V (contd.)

Die (Chip) faults : during processing of the waters and subsequent dice, cracks are sometimes produced. Temperature stress can propagate these cracks causing failure of the circuit.

Applicable tests are visual examination, temperature cycling and acceleration.

Die (Chip) Metallisation : faults such as narrowing of the metallised cracks through mask faults and mechanical scratching can cause high current density in the tracks and subsequent electro-migration leading to an open-circuit. Short circuiting between two adjacent metallised tracks is sometimes encountened.

Applicable tests are visual examination, electrical tests and burn-in.

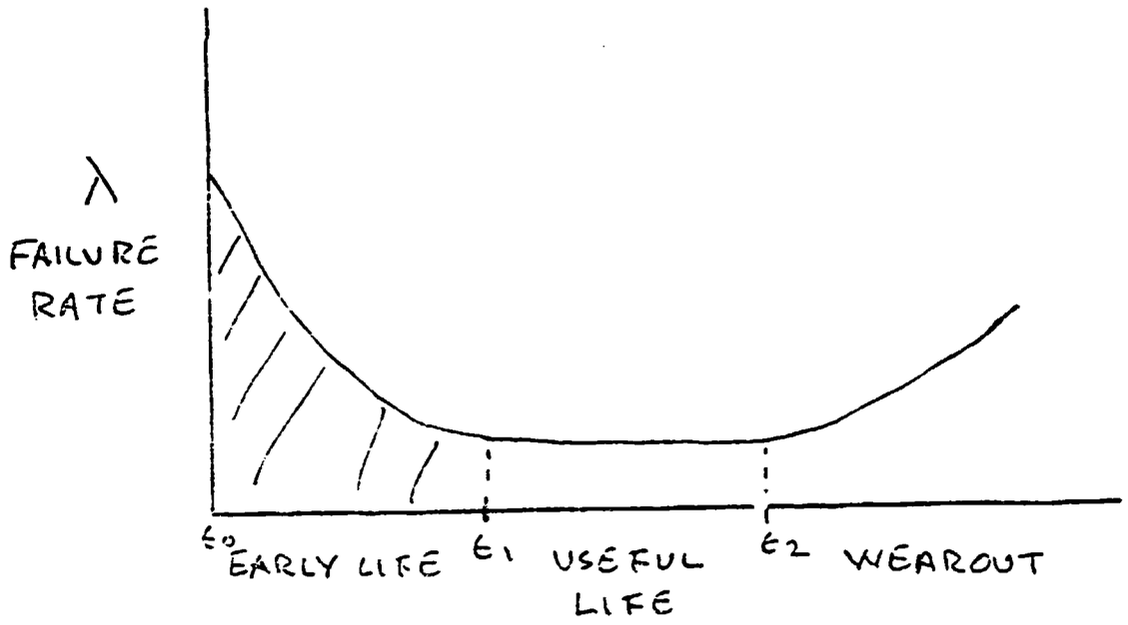
Internal cavity : any contamination present is an obvious reliability hazard, ionic contaminants give rise to surface leakage proolems, also corrosion of the metallisation. Moisture can have the same effect.

Applicable tests are electrical tests.

Bonding wires : the obvious fault is that they may be too close and may be a little too long, and under conditions of vibration two adjacent wires may actually touch. They should of course be physically robust enough for withstand all the environmental tests.

Applicable tests are visual examination, and X-ray.

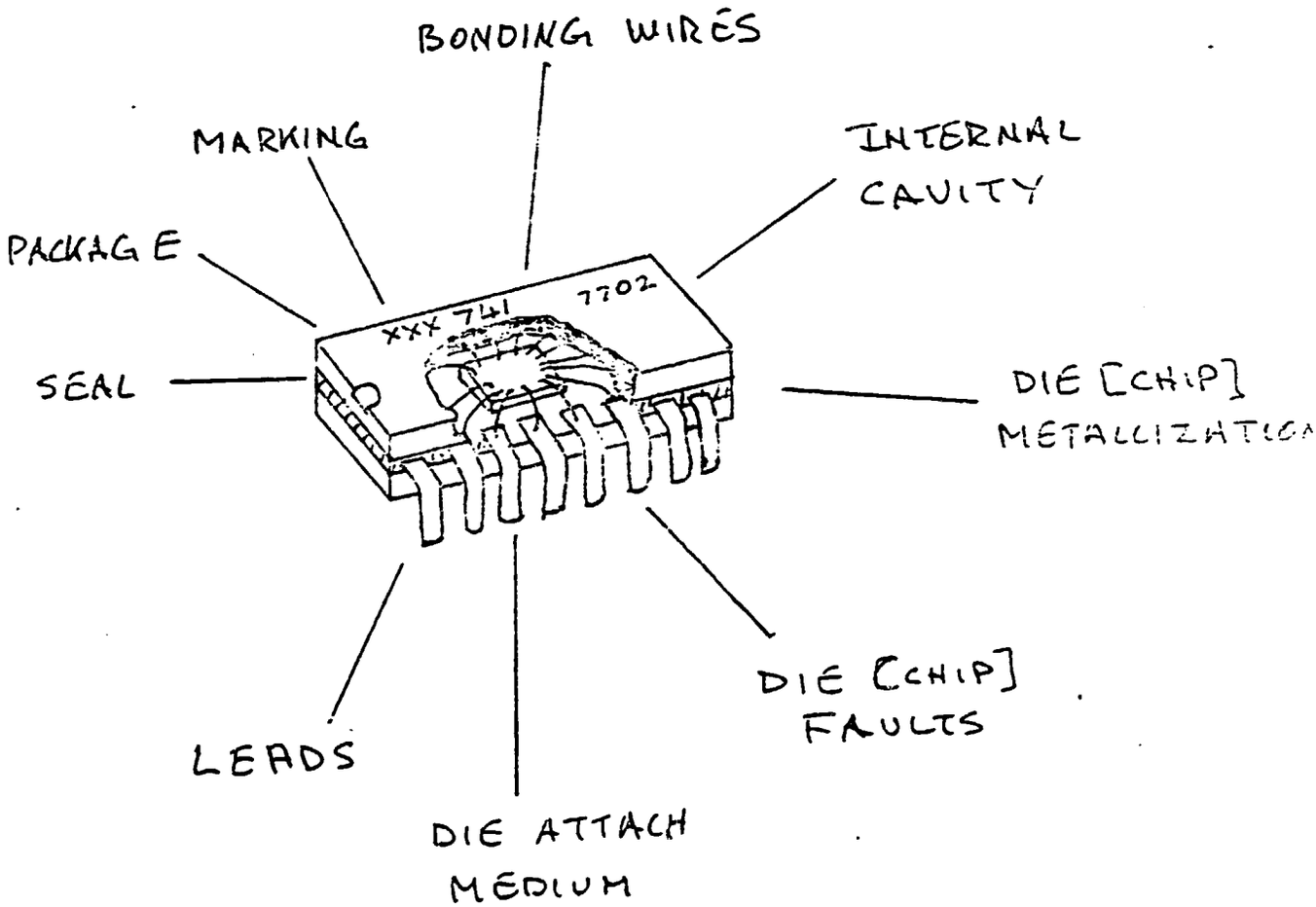
This is not a comprehensive test but it illustrates some of the many factors which can influence semiconductor reliability and shows how defective components can be screened out.



RELIABILITY LIFE CURVE

(THE "BATHTUB")

Figure 1



FACTORS AFFECTING SEMICONDUCTOR RELIABILITY

Figure 2

Annex VI

Project documentation

A Preliminary report was issued by the UNIDO expert after six weeks at National Test House, Calcutta (26th March 1982). It dealt with the general situation at NTH, and the situation in relation to the job description. Included as an Annex were the requirements for the Failure analysis laboratory at NTH in terms of space, facilities, staff and equipment.

Annex VII

SHORT SEMINAR ON RELIABILITY TESTING & FAILURE ANALYSIS WITH PARTICULAR REFERENCE TO ELECTRONIC COMPONENTS

(Convened jointly by NTH, Calcutta and AREA (E. Zone)

PROGRAMME

Venue : Lecture Hall of National Test House, Calcutta.

22nd July 1982

2.00 p.m. to 2.15 p.m.	Welcome Address by Dr. S.R. Das, Director General, National Test House, Calcutta.
2.15 p.m. to 2.30 p.m.	Address by Shri S.P. Kapur, Hon. Secretary of the All India Radio & Electronics Association (E. Zone), Calcutta (AREA)
2.30 p.m. to 3.30 p.m.	Address by the Principal Speaker, Mr. G. Bone, the U.N.D.P. Expert on the subject.
3.30 p.m. to 3.45 p.m.	T E A B R E A K
3.45 p.m. to 4.30 p.m.	Address by other speakers from NTH, AREA (E. Zone) or any other Institution and Organisations.
4.30 p.m. to 4.50 p.m.	Informal Technical Discussion
4.50 p.m. to 5.05 p.m.	Summing up of all the Technical Talks and discussions by Shri B.P. Ghosh, Jt. Director, National Test House, Calcutta.
5.05 p.m. to 5.10 p.m.	Vote of Thanks by Shri B.C. Mukherjee, Deputy Director (Electronics), National Test House, Calcutta.