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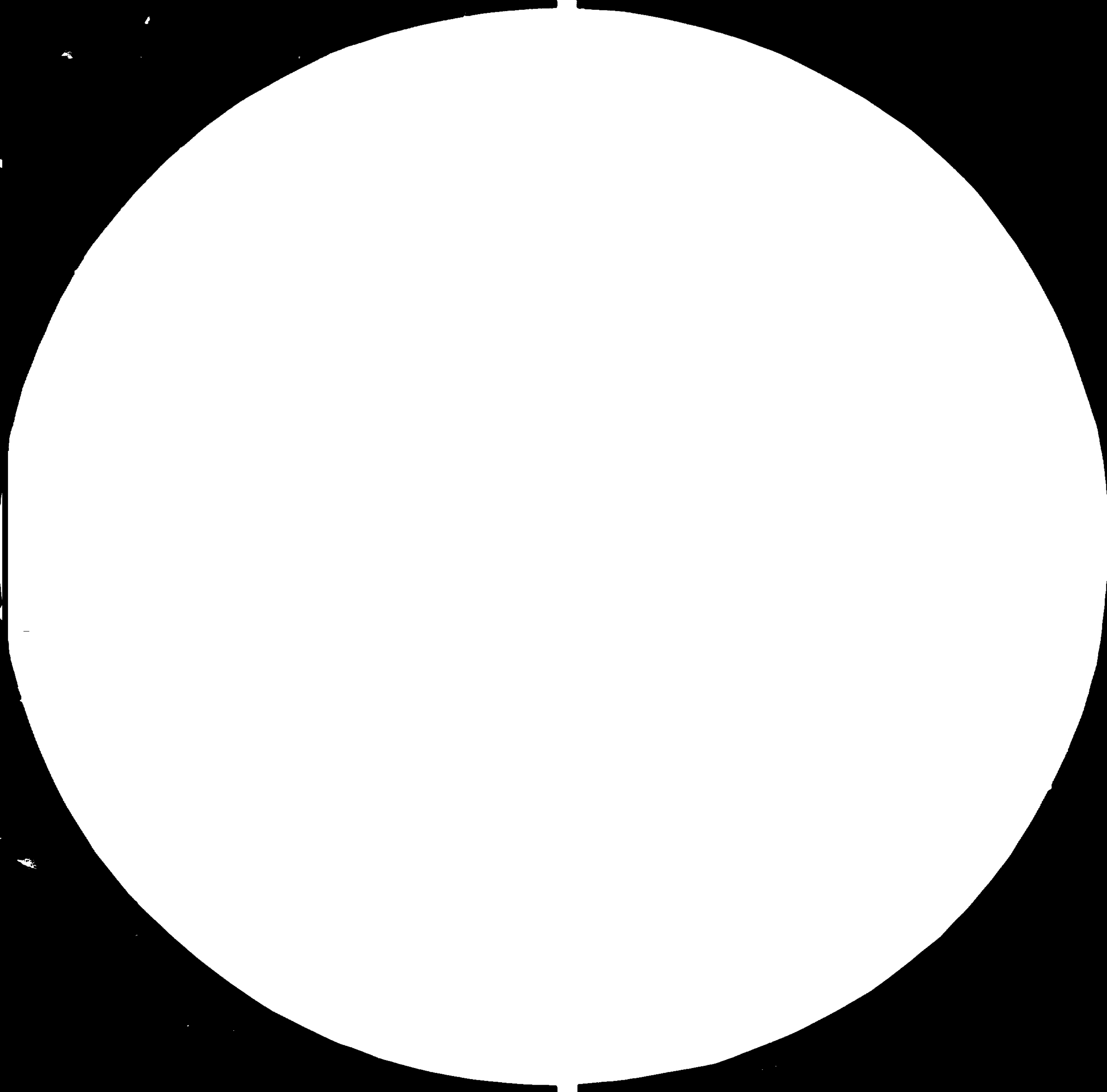

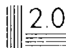

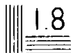
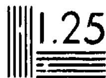

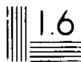

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SEMICONDUCTOR MATERIALS TECHNOLOGY

DP/ROK/75/019

REPUBLIC OF KOREA .

Terminal report *

Prepared for the Government of the Republic of Korea
by the United Nations Industrial Development Organization,
acting as executing agency for the United Nations
Development Programme

Based on the work of Yoon Soo Park,
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United Nations Industrial Development Organization

Vienna

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Abstract

Post Title: Consultant in Gallium-Arsenide Materials Technology

Duty Station: Seoul, Korea

Duration: Phase I (November 20 - December 16, 1980)
Phase II (September 15 - October 14, 1981)

Objective: To advise and assist the technical staff of the Semiconductor Materials Laboratory of the Korean Advanced Institute of Science and Technology in the growth, characterization, and processing of epitaxial and bulk crystals of GaAs and related Group III-V compounds.

Conclusions: Procedures relating to the growth, characterization, and processing of epitaxial and bulk crystals of GaAs were outlined to the technical staff of KAIST-SML. Three growth reactors for GaAs have been installed. Growth and characterization of silicon single crystals were performed, and consultation was provided on the on-going silicon-materials-technology program.

Recommendation: Although steady progress has been made toward achieving the goals set forth in the semiconductor-materials-technology program, it appears that additional and continuing support from UNDP is needed in order to bring the initial aim of the program to fruition. Establishment of adequate and competitive research efforts is urgently needed to cope with technological advances being made in other countries.

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I. INTRODUCTION

Over the past two years, the Korean Advanced Institute of Science and Technology (KAIST) initiated and carried out an ambitious program to establish a technology base for self-sufficiency in Si and GaAs semiconductor electronic materials to meet the needs of Korean industries. With technical and financial support from UNDP-UNIDO, remarkable progress has been made in this undertaking and the effort is soon to be brought to fruition.

Recently, activity related to the growth and characterization of Si and III-V semiconducting compounds, notably GaAs and InP, has increased because of the need for large-scale, high-speed digital logic and microwave circuits. The field of opto-electronics has also experienced widespread interest, primarily as a result of advances in the performance and reliability of epitaxial III-V material structures. The types of III-V materials for use in optical communication systems are constantly being developed.

In response to this increased interest and challenge and, in particular, to the critical need and demand of Korean electronics industries for materials growth and supply, the Semiconducting Materials Laboratory (SML) at KAIST is establishing the technology of growing bulk single crystals of both Si and GaAs and epitaxial layers of GaAs and related III-V compound semiconductors.

Unfortunately, the entire domestic supply of electronic materials is now dependent upon foreign sources. If these sources were severed for one reason or another, the domestic producers of electronic devices would be forced to develop their own crystal-growth technology and apparatus. Such a state of affairs, if it should occur, would be truly chaotic and detrimental to the future welfare of Korean electronic industries and the health of the Korean economy as a whole. This unfortunate and critical weak link in the electronic technology in Korea must be rectified if the Korean electronics industries are to survive.

Therefore, considerable attention and effort should be given to the development and establishment of growth and charactization capabilities of

electronic materials in Korea. The value and impact of such a technological venture need not be expounded upon.

II. ACTIVITY REPORT

A. Summary of activity

Phase I (November 20 - December 16, 1980)

In the first week of my stay at KAIST, I reviewed all equipment on order for growth and characterization of GaAs materials. Major equipment included the Model 301 Horizontal Bridgman Crystal Grower, Model 420 Research Epitaxial Reactor, Model 421 MOCVD Reactor made by Crystal Specialty, Inc., and the High Impedance Hall Effect Measurement System from Keithley Instruments, Inc. I feel that acquisition of these items is absolutely necessary for the implementation and success of the GaAs research program. Equipment was carefully selected in light of potential electronic-device requirements by Korean industries. Special emphasis was given to meeting the fabrication requirements for light sources and detectors applicable in display and fiber-optic communication and FET's for microwave-device applications.

In subsequent weeks I presented six two-hour seminars on crystal growth, characterization, and processing techniques of GaAs to the members of the Semiconductor Materials Group. In addition, seminars on "Growth and Characterization of Semi-Insulating GaAs" at Yonsei University, "Device Processing of GaAs" to the Electrical Engineering Department of the Korean Advanced Institute of Science, and "GaAs Materials Research, Present and Future" to the Solid State Physics Group of the Korean Physical Society were presented.

In addition to the GaAs consultation activities, I had the opportunity to participate in the growth of silicon single crystals and provided consultation on the on-going silicon-materials-technology program. During my visit the first test runs of the Siltec Model 860D Czochralski Silicon Puller were made. This is the crystal puller recently purchased by KAIST through the UNIDO

assistance program. Four successful test runs were made and four single crystals of the following dimensions were grown:

- 1 ea 4-in. diam., 18-in. length containing a 6-in. polycrystal region, <111> orientation
- 1 ea 4-in. diam., 26-in. length containing a 6-in. polycrystal region, <111> orientation
- 1 ea 3-in. diam., 15-in. length, <111> orientation
- 1 ea 3-in. diam., 15-in. length, <100> orientation.

Two 3-in.-diam. single crystals were free of crystalline defects, and they are the first silicon single crystals grown in Korea. It was a sheer delight to witness such fine crystals being grown in an environment that is lacking in adequate facilities.

Phase II (September 15 - October 14, 1981)

The three growth reactors--Model 301 Horizontal Bridgman Crystal Grower, Model 420 Research Epitaxial Reactor, and Model 421 MOCVD Reactor--were delivered in July by Crystal Specialty, Inc. Since then the KAIST-SML technical members have been busy with installation and repair of the damage to the reactors during shipping.

During the week of my arrival, installation of the exhaust system and the power lines for all three reactors began. Operational procedures for the HB Crystal Grower were followed step by step, but many unexpected difficulties were encountered during the test run. The Model 1040 Programmer used for total system control of the crystal grower did not function as smoothly as anticipated. For example, the motor speed control for the heater travel mechanism did not provide variable-speed control, and the temperature controller for the third zone in the furnace did not function properly. The possible causes for trouble were traced, and mechanical and electrical component parts requiring replacement were identified; the information was relayed to the manufacturer upon my return to the United States.

Because of these unexpected difficulties, unfortunately, no test run of the grower was made during my stay. However, the crystal-growth procedures were reviewed in detail, and pre-growth cleaning and baking procedures of the growth tube and boat were determined. The boat for the seed crystal was designed.

The Ga reservoir of the process tube of the Model 420 Epitaxial Reactor was broken during shipping, and the mass flow controllers for the dopant gas were missing.

Full operation of all three reactors is not expected until damaged/missing parts are repaired/replaced.

In addition to the activities at KAIST-SML, I participated in and presented an opening lecture entitled, "Electronic and Opto-Electronic Future of III-V Compound Semiconductors," at the First International Workshop on Semiconductor Physics which was held at Seoul National University, September 25-29, 1981. I gave a seminar on "Perspective of GaAs Materials Research at the Kyungbug University and on "Redistribution of Impurities in GaAs" at the Jungbuk University.

B. Current status of KAIST-SML materials research

With the support of UNDP, KAIST-SML acquired certain pieces of equipment essential for the growth, processing, and characterization of Si and GaAs. These include

- Siltec Model 860D Czochralski Silicon Puller
- Surface grinding machine
- Slicing machine
- Polishing machine
- Spreading-resistance measurement system
- Non-contact resistivity meter
- Non-contact thickness meter
- C-V plotter
- Crystal Specialty (CS) Model 301 Horizontal Bridgman GaAs Crystal Grower

- CS Model 420 Research Epitaxial GaAs Reactor
- CS Model 421 MOCVD GaAs Reactor

In addition, an automatic Hall-effect system is on order.

The Siltec Model 860D Czochralski Silicon Puller was installed and tested successfully in November of 1980; since then, the staff of SML has been routinely pulling Si boules of 3-4 in. diameter.

Single crystals, both undoped and P-doped (n-type), grown by SML are now being evaluated by various characterization techniques. All the crystals pulled appeared to be of fine quality in terms of crystal morphology, as revealed by x-ray and optical methods. Oxygen impurity concentration was found to be on the order of 5×10^{17}/CC as determined by infrared absorption, and a nearly equal amount of carbon was also detected.

Most of the crystals were free of dislocations (EPD $< 100/\text{cm}^2$), although an undoped crystal grown in the (100) direction showed a dislocation density of $10^4/\text{cm}^2$. This boule was the one which was lost structurally during the run.

Radial and axial resistivity profiles of both undoped and P-doped crystal boules were examined by the spreading-resistance meter. Resistivity of an undoped (111) crystal varied from 10 Ω-cm in the seed end to 25 Ω-cm in the tail end. Resistivity of a P-doped (111) crystal, for example, varied from 0.9 Ω-cm in the seed end to 0.7 Ω-cm in the tail end. The seed end of a P-doped (100) crystal showed a resistivity of 0.8 Ω-cm, while the resistivity of the tail end was 0.5 Ω-cm. The axial variation of resistivity was within ± 6.8%.

Several boules of Si were ground at the surface and sliced into wafers with the automatic saw. Some wafers were hand polished because the polishing pads in the new polishing machine had not arrived. Also, the edges of the wafers were not rounded because of the unavailability of the edge grinder. The wafers were not processed for device fabrication. It will be interesting to see how these wafers behave under the actual device-fabrication process.

The three growth reactors for GaAs arrived in July of 1981. Installation of the reactors was initiated immediately. However, many parts of the reactors were damaged during shipping. Repair and replacement of the damaged parts and installation of all three reactors should be completed by the end of December 1981.

III. RECOMMENDATION

In the UNDP project document, ROK/75/019, the need for establishing local semiconductor technology was justified. To develop a more sophisticated technology intensive electronics industry from the present simple assembly-type industry, it was stressed that the new materials-technology program in Si and GaAs should be initiated as quickly as possible. If the Korean electronics industry is to remain competitive in the world market, it is imperative that the domestic industry become self-sufficient in the production and processing of semiconductor materials.

The purpose of the project was to acquire and develop the technologies needed for the production and processing of semiconductor materials by domestic industry. The transfer of semiconductor materials and processing technology to industry was strongly emphasized.

Since the initiation of the program in March of 1979, the program has been steadily progressing with the cooperative efforts of UNDP and KAIST personnel. Although some difficulties in the procurement of equipment and in the training of the personnel were encountered, impressive progress has been made in the growth of Si single crystals, as demonstrated in Section II. For the first time in Korea, defect-free, good-quality silicon single crystals of 3-4 in. diameter have been grown by KAIST scientists and technicians. Although steady progress has been made toward achieving the goals set forth in the program, it now appears that additional and continuing support from UNDP is needed in order to bring the initial aim of the program to fruition.

The following work is recommended for support in the future.

A. Silicon semiconductor materials

Silicon single-crystal growth

Acquisition of an additional Czochralski puller is desirable. For fabrication of semiconductor devices, both n- and p-type single-crystal wafers are required. At present KAIST-SML is equipped with only one Czochralski puller which is capable of producing large single-crystal ingots of 3-4 in. diameter. With this puller either n- or p-type single crystals can be produced. Unless an additional puller is procured, both n- and p-type crystals must be grown in the same system. The crystals grown in this way can inevitably be cross-contaminated, and this mode of operation is very inefficient. Since growth of high-purity materials is the key to successful fabrication of solid-state devices, it is highly desirable to dedicate the system to a specific conductivity type. In view of the anticipated future demand of domestic electronic industries, it would be wise to prepare and up-grade the growth facility at KAIST-SML.

Development of silicon-wafer processing

The wafer-processing facility at KAIST-SML is currently equipped with slicing, surface-grinding, and polishing machines which were acquired with UNDP support. The facility is used to conduct research on developing techniques and procedures for preparing defect-free wafer surfaces for device fabrication which will satisfy the requirements of industry. In order to meet stringent device-fabrication requirements, the facility must be augmented by additional equipment. The additional equipment needed includes a cut-off saw, a lapping machine, an edge grinder for rounding the edges of the wafers, a wafer sorter, a wax-free polisher, and a wafer-cleaning system. Acquisition of these pieces of equipment will greatly enhance the research and development capabilities in the processing area at KAIST-SML and will facilitate the transfer of technology to domestic electronics industries.

Characterization of defects in silicon

The crystal-growth and wafer-processing activities must be closely coordinated with and influenced by an effective characterization program which will permit the identification of all types of defects--both mechanical and

electrical. These defects include physical and chemical states of wafer surfaces, residual and foreign impurities, lattice defects, and gross imperfections such as dislocations, precipitates, and agglomerates.

Emphasis should be placed upon the study and analysis of oxygen and carbon concentrations and upon minimization of their contamination during the growth process. In particular their role in the formation of striated micro-defect distributions (swirl defects) in silicon during crystal growth should be investigated. Recently it has been shown experimentally that such swirl defects play one of the most important roles in the performance, reliability, and yield of Si LSI and VLSI circuits. Therefore, it is imperative that the grown materials be characterized in a systematic way in order to provide dislocation- and swirl-free crystals for device fabrication.

KAIST-SML is presently equipment-limited in their efforts on characterization of grown materials. In addition to the growth facilities, their characterization capabilities should be strengthened and expanded. The addition of an x-ray machine, lifetime tester, ultrasonic sono tester, wafer fracture tester, scanning electron microscope, thermal and optical annealer, and cryogenic system will greatly enhance the characterization-measurement activities at KAIST. The characterization-measurement results should be correlated with growth parameters, and the information should constantly be fed into the growth process. With such well-organized coordination efforts of the characterization and growth activities, high-device-quality materials with a high degree of purity and structure perfection can be obtained.

Technology transfer

Efforts to transfer semiconductor materials and processing technology to industry should be intensified. Contacts should be made regarding utilization of the KAIST-SML-grown wafers for device processing and fabrication. Device performance should be analyzed, and device processing and material quality should be evaluated in light of device characteristics. Correlation of device performance, device processing, and material characteristics should be established.

Wafers from KAIST-SML should be made available in reasonable quantities to all interacting organizations--universities, research institutes, and industries--for evaluation and use. Flow of information among the interacting organizations should be established. Feedback of information, from materials characterization to crystal growth and from device processing and testing and, in the opposite direction, from crystal growth to materials characterization to device processing and testing should form an essential basis for future activities regarding technology transfer.

B. GaAs materials and devices

The last decade has seen a great increase in worldwide activities related to the growth and characterization of III-V semiconducting compounds--notably GaAs--because of the need for LEDs, laser diodes, and high-speed microwave device and logic circuits. However, GaAs technology can be considered a new, emerging technology in Korea. In contrast to silicon-device manufacturing industries, only a few companies are engaged in assembly-type production of LEDs. Recognizing the importance of the technology of GaAs for the future electronics industry in Korea, the research activities involving GaAs materials growth and characterization have been proposed in the UNDP project document.

It is anticipated that the demand for LEDs will continue to increase for display applications. Use of LEDs and laser diodes as potential light sources for optical communications is expected to increase considerably within a few years.

Increased use of the Field Effect Transistor (FET) for amplification at frequencies above which a silicon bipolar transistor can be utilized is also anticipated.

To meet this challenge to be faced by future Korean electronics industries, KAIST-SML has acquired growth reactors for both **epitaxial and** bulk crystals. The vapor-phase-epitaxial (VPE) and metal-organic chemical-vapor-deposition (MOCVD) reactors for epitaxial growth and the Horizontal Bridgeman Reactor

for bulk crystal growth have been procured with the support of UNDP. Installation and testing of the three reactors is expected to be completed at the end of December 1981. By the end of this project, full production of both epitaxial layers and bulk crystals is expected.

Further work for GaAs should be planned.

In-depth characterization of epitaxial and single crystals

It is well known that large concentrations of point defects can occur in GaAs and that these native defects can interact with intentional dopants to alter the electrical characteristics of the host materials. In order to understand how impurities and point defects interact and to clarify the effects of native defects and impurity-defect complexes upon the electrical-device characteristics of epitaxially and bulk-grown crystals, the following effort is proposed: (a) identification of stoichiometric defects, residual impurities, intentionally added impurities, and the interaction of impurities and defects in epitaxial and bulk materials; (b) study of how impurities and defects are incorporated into the epitaxial layer and bulk crystals during growth; (c) detailed study of growth parameters in the VPE, MOCVD, and HB systems which influence the incorporation of lattice defects and impurity-defect complexing; (d) coordination of the crystal-growth program with an expensive and detailed materials-characterization program capable of fundamental and detailed analysis of the materials; and (e) study of device feasibility and testing to permit correlation of material properties and device performance.

To implement this characterization program, several universities, research institutes, and industries should be recruited for collaboration. However, establishment of basic characterization techniques is needed to couple the growth and characterization activities.

Acquisition of the following capabilities is recommended:

1. Ellipsometry
2. Photoluminescence spectroscopy
3. Deep-level-transient spectroscopy

Device fabrication and evaluation

Since, unlike the case of Si, the domestic electronics industries are not familiar with GaAs device-fabrication and process technology, initiation of device fabrication must originate with KAIST-SML. KAIST-SML is expected to establish a basic device-fabrication facility.

Acquisition of the following items will enable KAIST-SML to begin fabrication and processing of LEDs, laser diodes, and low-power FETs:

1. D. I. water system
2. Hydrogen purifier
3. Electron-beam evaporator
4. Mask aligner
5. Photoresist spinner
6. Wire bonder
7. Die bonder
8. Micro ion milling system
9. LPE reactor
10. Alpha step profiler

It is recommended that devices be fabricated from the high-quality material produced and that these devices be tested under actual operating conditions. A complete correlation between device performance and reliability and material properties should be made. It should be the goal of the future program to control growth parameters to the degree necessary to tailor material properties for maximum device yield, performance, and reliability. This requires a complete understanding of the detailed nature of defects, impurities, and their interactions as well as uniformity of incorporation and position in the host lattice. It is felt that this is the key to reproducible, high-quality material from which high-yield, reproducible, reliable devices can be made economically.

Growth and characterization of semi-insulating crystals

Significant progress is currently being made toward developing a viable planar-ion-implantation technology, but it is widely recognized that the

variable--and often poor--quality of semi-insulating substrates is a major limitation at present. GaAs substrates of high resistivity, which retain their semi-insulating properties throughout device fabrication, are required in order to maintain both good electrical isolation and low parasitic capacitance associated with active devices. Unfortunately, at the temperatures normally employed in FET processing, the thermal stability of semi-insulating substrates has often been a severe problem. A common manifestation of the problem is the formation of a conductive surface layer following a thermal annealing process. In ion-implantation technology, these anomalous conversion and compensation phenomena which have been observed following post-implantation annealing adversely affect the implant profile and activation and can result in poor control of full-channel current and pinch-off voltage in directly implanted digital and power FET structures. It is probable that the high and variable concentrations of silicon, chromium, oxygen, and carbon impurities which are present in typical Cr-doped semi-insulating substrates contribute to the difficulties in achieving uniform implant profiles, since these impurities can modify their electrical role and redistribute as a result of implantation and thermal annealing.

KAIST-SML should attempt to grow thermally stable, high-resistivity GaAs substrates which contain very low concentrations of residual impurities and are thus suitable for direct ion-implantation device fabrication.